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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	-
Number of Cores/Bus Width	-
Speed	-
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	-
Operating Temperature	-
Security Features	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/bsc9132nxn7knkb

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
IFC_AD12/ GPIO38/ IRQ09	IFC Muxed Address,Data	G26	I/O	BVDD	—
IFC_AD13/ GPIO39/ IRQ07	IFC Muxed Address,Data	G27	I/O	BVDD	—
IFC_AD14/ GPIO40/ IRQ06	IFC Muxed Address,Data	G28	I/O	BVDD	—
IFC_AD15/ GPIO41/ TIMER02	IFC Muxed Address,Data	H28	I/O	BVDD	—
IFC_ADDR16/ GPO08	IFC Address	H26	O	BVDD	2
IFC_ADDR17/ GPO09	IFC Address	H25	O	BVDD	2
IFC_ADDR18/ GPO10	IFC Address	H24	O	BVDD	2
IFC_ADDR19/ GPO11	IFC Address	H22	O	BVDD	2
IFC_ADDR20/ GPO12	IFC Address	H21	O	BVDD	2
IFC_ADDR21/ GPO13	IFC Address	J28	O	BVDD	2
IFC_ADDR22/ GPO14	IFC Address	J27	O	BVDD	18
IFC_ADDR23/ GPO15	IFC Address	J25	O	BVDD	2
IFC_ADDR24/ GPO16	IFC Address	J24	O	BVDD	2
IFC_ADDR25/ GPO17	IFC Address	J23	O	BVDD	2
IFC_ADDR26/ GPO18	IFC Address	J22	O	BVDD	2
IFC_AVD/ GPO54	IFC Address Valid	L28	O	BVDD	2
IFC_CS_B00/ GPO55	IFC Chip Select	K21	O	BVDD	—
IFC_CS_B01/ GPO64	IFC Chip Select	K28	O	BVDD	—
IFC_CS_B02/ GPO65	IFC Chip Select	L24	O	BVDD	—
IFC_WE_B/ GPO52	IFC Write Enable/GPCM Write Byte Select0/ Generic ASIC i/f Start of Frame	L26	O	BVDD	2

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT2_DIO104/ **TDM1_RCK**/ GPIO92	TDM1 Receive Clock	K4	I/O	X2VDD	—
ANT2_DIO105/ **TDM1_RFS**/ TIMER08	TDM1 Receive Frame Sync	K7	I/O	X2VDD	—
ANT2_DIO102/ **TDM1_RXD**	TDM1 Receive Data	J7	I/O	X2VDD	—
TDM2 over RF3					
ANT3_RX_CLK/ **TDM2_TCK**/ GPIO04	TDM2 Clock	D1	I/O	X2VDD	—
ANT3_DIO007/ **TDM2_TFS**	TDM2 Transmit Frame Sync	B3	I/O	X2VDD	—
ANT3_DIO011/ **TDM2_TXD**	TDM2 Transmit Data	B1	I/O	X2VDD	—
ANT3_DIO008/ **TDM2_RCK**/ CKSTP0_OUT_B	TDM2 Receive Clock	A2	I/O	X2VDD	—
ANT3_DIO009/ **TDM2_RFS**/ CKSTP1_OUT_B	TDM2 Receive Frame Sync	C3	I/O	X2VDD	—
ANT3_DIO010/ **TDM2_RXD**	TDM2 Receive Data	D4	I/O	X2VDD	—
SerDes					
SD_TX03	Tx Data out	AE19	O	XPADVDD	—
SD_TX02	Tx Data out	AE21	O	XPADVDD	—
SD_TX01	Tx Data out	AE23	O	XPADVDD	—
SD_TX00	Tx Data out	AE25	O	XPADVDD	—
SD_TX_B03	Tx Data out, inverted	AF19	O	XPADVDD	—
SD_TX_B02	Tx Data out, inverted	AF21	O	XPADVDD	—
SD_TX_B01	Tx Data out, inverted	AF23	O	XPADVDD	—
SD_TX_B00	Tx Data out, inverted	AF25	O	XPADVDD	—
SD_RX03	Rx Data in	AG18	I	XCOREVDD	—
SD_RX02	Rx Data in	AG20	I	XCOREVDD	—
SD_RX01	Rx Data in	AG22	I	XCOREVDD	—
SD_RX00	Rx Data in	AG24	I	XCOREVDD	—
SD_RX_B03	Rx Data in, Inverted	AH18	I	XCOREVDD	—
SD_RX_B02	Rx Data in, Inverted	AH20	I	XCOREVDD	—
SD_RX_B01	Rx Data in, Inverted	AH22	I	XCOREVDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT1_DIO111/ **TIMER07**/ GPIO24	Timer 7	U3	I/O	X1VDD	—
ANT2_DIO105/ TDM1_RFS/ **TIMER08**	Timer 8	K7	I/O	X2VDD	—
OCeaN DMA					
SDHC_DATA03/ **DMA_DDONE_B00**/ CKSTP1_IN_B/ GPIO77	DMA done	E25	I/O	BVDD	
ANT2_TX_FRAME/ **DMA_DDONE_B00**	DMA done	G4	O	X2VDD	
SDHC_WP/ **DMA_DREQ_B00**/ CKSTP0_IN_B/ GPIO78	DMA request	G23	I	BVDD	—
ANT2_RX_FRAME/ **DMA_DREQ_B00**	DMA request	H3	I	X2VDD	—
SDHC_CD/ **DMA_DACK_B00**/ MCP1_B/ GPIO79/ IRQ10	DMA acknowledge	C25	O	BVDD	—
ANT2_TXNRX/ **DMA_DACK_B00**	DMA acknowledge	H2	O	X2VDD	—
System DMA					
ANT4_ENABLE/ **SYS_DMA_DONE**	System DMA done	Y2	O	X1VDD	—
UART_RTS_B01/ **SYS_DMA_DONE**/ GPO45/ ANT4_AGC	System DMA done	Y27	O	OVDD	—
UART_CTS_B01/ **SYS_DMA_REQ**/ SRESET_B/ GPIO44/ IRQ05	System DMA request	W22	I	OVDD	—
ANT4_DIO001/ **SYS_DMA_REQ**	System DMA request	U6	I	X1VDD	—
Interrupts					
USB_D04/ GPIO00/ **IRQ00**	External Interrupt	P26	I	CVDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
SDHC_WP/ DMA_DREQ_B00/ CKSTP0_IN_B/ **GPIO78**	General Purpose I/O	G23	I/O	BVDD	—
SDHC_CD/ DMA_DACK_B00/ MCP1_B/ **GPIO79**/ IRQ10	General Purpose I/O	C25	I/O	BVDD	—
ANT1_RX_FRAME/ **GPIO80**	General Purpose I/O	R2	I/O	X1VDD	—
ANT1_DIO100/ **GPIO81**	General Purpose I/O	P4	I/O	X1VDD	—
ANT1_DIO101/ **GPIO82**	General Purpose I/O	R1	I/O	X1VDD	—
ANT1_DIO102/ **GPIO83**	General Purpose I/O	R5	I/O	X1VDD	—
ANT1_DIO103/ **GPIO84**	General Purpose I/O	R7	I/O	X1VDD	—
ANT1_DIO104/ **GPIO85**	General Purpose I/O	T1	I/O	X1VDD	—
ANT1_DIO105/ **GPIO86**	General Purpose I/O	T3	I/O	X1VDD	—
ANT1_DIO106/ **GPIO87**/ IRQ10	General Purpose I/O	T5	I/O	X1VDD	—
ANT1_DIO107/ **GPIO88**/ IRQ11	General Purpose I/O	T6	I/O	X1VDD	—
ANT2_RX_CLK/ **GPIO91**	General Purpose I/O	J3	I/O	X2VDD	—
ANT2_DIO104/ TDM1_RCK/ **GPIO92**	General Purpose I/O	K4	I/O	X2VDD	—
ANT1_RX_CLK/ TSEC_1588_TRIG_IN2/ **GPIO95**	General Purpose I/O	P2	I/O	X1VDD	—
GPO					
ANT4_TX_FRAME/ **GPO06**	General Purpose Output	Y3	O	X1VDD	—
IFC_ADDR16**/** **GPO08**	General Purpose Output	H26	O	BVDD	—
IFC_ADDR17**/** **GPO09**	General Purpose Output	H25	O	BVDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
cfg_d2_dram_type/ ANT1_AGC/ GPO58	DDR2 DRAM Type	R3	I	X1VDD	2
cfg_ifc_ecc[0]/ UART_RTS_B00/ PPS_LED/GPO43	IFC ECC Enable Configuration	AB26	I	OVDD	2
cfg_ifc_ecc[1]/UART_SOUT01/ GPO56	IFC ECC Enable Configuration	W23	I	OVDD	2
cfg_host_agt/UART_RTS_B01/ SYS_DMA_DONE/ GPO45/ ANT4_AGC	Host/Agent Configuration	Y27	I	OVDD	2
cfg_ifc_adm_mode/IFC_WE_B/ GPO52	IFC Address Shift Mode Configuration	L26	I	BVDD	2
cfg_ifc_flash_mode/EE1	IFC Flash Mode Configuration	T25	I	OVDD	2
cfg_srds_io_ports[0]/READY/ ASLEEP/READY_P1	SerDes I/O Port Selection	U21	I	OVDD	2
cfg_srds_io_ports[1]/ ANT1_DIO000	SerDes I/O Port Selection	L7	I	X1VDD	2
cfg_srds_io_ports[2]/ ANT1_DIO010	SerDes I/O Port Selection	M1	I	X1VDD	2
cfg_srds_io_ports[3]/ ANT1_DIO011	SerDes I/O Port Selection	N3	I	X1VDD	2
cfg_srds_io_ports[4]/ ANT3_TX_FRAME	SerDes I/O Port Selection	E3	I	X2VDD	2
cfg_srds_io_ports[5]/ ANT4_TX_FRAME/ GPO06	SerDes I/O Port Selection	Y3	I	X1VDD	2
cfg_srds_io_ports[6]/ SPI2_MOSI	SerDes I/O Port Selection	E7	I	X2VDD	2
cfg_rom_loc[0]/ANT1_DIO006	Boot ROM Location	N6	I	X1VDD	2
cfg_rom_loc[1]/ANT1_DIO007	Boot ROM Location	M3	I	X1VDD	2
cfg_rom_loc[2]/ANT1_DIO008	Boot ROM Location	M2	I	X1VDD	2
cfg_rom_loc[3]/ANT2_AGC/ GPO89	Boot ROM Location	G1	I	X2VDD	2
cfg_srds_pll_timeout_en/ ANT1_DIO001	SerDes PLL Timeout Enable	N7	I	X1VDD	2, 4
cfg_d1_ddr_half_full_mode/ ANT1_DIO002	Power Architecture DDR Mode	P7	I	X1VDD	2
cfg_d2_ddr_half_full_mode/ ANT1_DIO003	DSP DDR Mode	N5	I	X1VDD	2
cfg_srds_refclk/ANT1_DIO009	SerDes Reference Clock Configuration	M5	I	X1VDD	2
Power Supply					

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
G1VDD	DDR Supply	E11	—	G1VDD	—
G1VDD	DDR Supply	H9	—	G1VDD	—
G1VDD	DDR Supply	H10	—	G1VDD	—
G1VDD	DDR Supply	H11	—	G1VDD	—
G1VDD	DDR Supply	H12	—	G1VDD	—
G1VDD	DDR Supply	H13	—	G1VDD	—
G1VDD	DDR Supply	H14	—	G1VDD	—
G1VDD	DDR Supply	H15	—	G1VDD	—
G1VDD	DDR Supply	H16	—	G1VDD	—
G1VDD	DDR Supply	H17	—	G1VDD	—
G1VDD	DDR Supply	H18	—	G1VDD	—
G1VDD	DDR Supply	H19	—	G1VDD	—
G1VDD	DDR Supply	H20	—	G1VDD	—
G1VDD	DDR Supply	B18	—	G1VDD	—
G1VDD	DDR Supply	B23	—	G1VDD	—
G1VDD	DDR Supply	D20	—	G1VDD	—
G1VDD	DDR Supply	E15	—	G1VDD	—
G2VDD	DDR Supply	AC3	—	G2VDD	—
G2VDD	DDR Supply	AC10	—	G2VDD	—
G2VDD	DDR Supply	AA8	—	G2VDD	—
G2VDD	DDR Supply	AA9	—	G2VDD	—
G2VDD	DDR Supply	AA10	—	G2VDD	—
G2VDD	DDR Supply	AA11	—	G2VDD	—
G2VDD	DDR Supply	AA12	—	G2VDD	—
G2VDD	DDR Supply	AA13	—	G2VDD	—
G2VDD	DDR Supply	AA14	—	G2VDD	—
G2VDD	DDR Supply	AA15	—	G2VDD	—
G2VDD	DDR Supply	AD6	—	G2VDD	—
G2VDD	DDR Supply	AD13	—	G2VDD	—
G2VDD	DDR Supply	AF2	—	G2VDD	—
G2VDD	DDR Supply	AG4	—	G2VDD	—
G2VDD	DDR Supply	AG9	—	G2VDD	—
G2VDD	DDR Supply	AG12	—	G2VDD	—
G2VDD	DDR Supply	AC15	—	G2VDD	—
LVDD	Ethernet Supply	Y23	—	LVDD	—
LVDD	Ethernet Supply	AA25	—	LVDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
VSS	Platform and Core Ground	D22	—	—	—
VSS	Platform and Core Ground	D24	—	—	—
VSS	Platform and Core Ground	E27	—	—	—
VSS	Platform and Core Ground	F18	—	—	—
VSS	Platform and Core Ground	F21	—	—	—
VSS	Platform and Core Ground	H23	—	—	—
VSS	Platform and Core Ground	H27	—	—	—
VSS	Platform and Core Ground	J15	—	—	—
VSS	Platform and Core Ground	J19	—	—	—
VSS	Platform and Core Ground	J21	—	—	—
VSS	Platform and Core Ground	K15	—	—	—
VSS	Platform and Core Ground	K17	—	—	—
VSS	Platform and Core Ground	K19	—	—	—
VSS	Platform and Core Ground	L15	—	—	—
VSS	Platform and Core Ground	L17	—	—	—
VSS	Platform and Core Ground	L19	—	—	—
VSS	Platform and Core Ground	L27	—	—	—
VSS	Platform and Core Ground	L21	—	—	—
VSS	Platform and Core Ground	L23	—	—	—
VSS	Platform and Core Ground	M15	—	—	—
VSS	Platform and Core Ground	M17	—	—	—
VSS	Platform and Core Ground	M19	—	—	—
VSS	Platform and Core Ground	M21	—	—	—
VSS	Platform and Core Ground	N15	—	—	—
VSS	Platform and Core Ground	N17	—	—	—
VSS	Platform and Core Ground	N19	—	—	—
VSS	Platform and Core Ground	N21	—	—	—
VSS	Platform and Core Ground	N24	—	—	—
VSS	Platform and Core Ground	P27	—	—	—
VSS	Platform and Core Ground	P15	—	—	—
VSS	Platform and Core Ground	P17	—	—	—
VSS	Platform and Core Ground	P19	—	—	—
VSS	Platform and Core Ground	P21	—	—	—
VSS	Platform and Core Ground	R15	—	—	—
VSS	Platform and Core Ground	R17	—	—	—
VSS	Platform and Core Ground	R19	—	—	—

Table 10. I/O Power (continued)

PS#	Primary pin name	Pin width	Voltage domain	Recommended value	Current max	Typical current (A)	Max (A)	Note
SD	SVDD	—	SerDes Core logic supply	1.0V	—	0.144	0.144	—
	XVDD	—	SerDes I/O supply	1.5V	—	0.058	0.058	—
Analog	AVDD_CORE0	—	Core 0 PLL supply	1.0V	—	0.005	0.015	—
	AVDD_CORE1	—	Core 1 PLL supply		—			—
	AVDD_DSP	—	DSP PLL supply		—			—
	AVDD_PLAT	—	Platform PLL supply		—			—
	AVDD_D1_DDR	—	DDR PLL supply		—			—
	AVDD_D2_DDR	—	DDR PLL supply		—			—
	SDAVDD1	—	SerDes PLL supply		—			—
	SDAVDD2	—	SerDes PLL supply		—			—

Note:

1 For DDR typical, it is 40% DIMM utilization.

2 For DDR max, it is 75% DIMM utilization.

3 For I/O with different possible voltages, the currents listed above are for the higher voltage.

2.7 Input Clocks

This section provides information about the system clock specifications, spread spectrum sources, real time clock specifications, TDM clock specifications, and other input sources.

2.7.1 System Clock and DDR Clock Specifications

This table provides the system clock (SYSCLK) and DDR clock (DDRCLK) 3.3 V DC specifications.

Table 11. SYSCLK/DDRCLK DC Electrical Characteristics

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter	Symbol	Min	Typical	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	—	V	1
Input low voltage	V_{IL}	—	—	0.8	V	1
Input capacitance	C_{IN}	—	7	15	pf	—
Input current (V_{IN}= 0 V or V_{IN} = V_{DDC})	I_{IN}	—	—	±50	μA	2

Note:

1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.

This table provides the system clock (SYSCLK) and DDR clock (DDRCLK) AC timing specifications.

Table 12. SYSCLK/DDRCLK AC Timing Specifications

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
SYSCLK frequency	f_{SYSCLK}	66	—	100	MHz	1, 2

Table 12. SYSCLK/DDRCLK AC Timing Specifications (continued)

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typ	Max	Unit	Note
SYSCLK cycle time	t_{SYSCLK}	7.5	—	10	ns	1, 2
DDRCLK frequency	f_{DDRCLK}	66	—	166	MHz	1
DDRCLK cycle time	t_{DDRCLK}	6.0	—	15.15	ns	—
SYSCLK/DDRCLK duty cycle	t_{KHK}/ $t_{SYSCLK/DDRCLK}$	40	—	60	%	2
SYSCLK/DDRCLK slew rate	—	1	—	4	V/ns	3
SYSCLK/DDRCLK peak period jitter	—	—	—	± 150	ps	—
SYSCLK/DDRCLK jitter phase noise at –56 dBc	—	—	—	500	kHz	4
AC Input Swing Limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Note:

1. **Caution:** The relevant clock ratio settings must be chosen such that the resulting SYSCLK frequency do not exceed their respective maximum or minimum operating frequencies.
2. Measured at the rising edge and/or the falling edge at $OV_{DD}/2$.
3. Slew rate as measured from ±0.3 ΔV_{AC} at the center of peak to peak voltage at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

2.7.2 DSP Clock (DSPCLKIN) Specifications

This table provides the DSP clock (DSPCLKIN) 3.3 V DC specifications.

Table 13. DSPCLKIN DC Electrical Characteristics

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter	Symbol	Min	Typical	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	—	V	1
Input low voltage	V_{IL}	—	—	0.8	V	1
Input capacitance	C_{IN}	—	7	15	pf	—
Input current (V_{IN}= 0 V or V_{IN} = V_{DDC})	I_{IN}	—	—	±50	μA	2

Note:

1. Note that the min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.

This table provides the DSP clock (DSPCLKIN) AC timing specifications.

Table 14. DSPCLKIN AC Timing Specifications

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
DSPCLKIN frequency	f_{SYSCLK}	66	—	133	MHz	1, 2
DSPCLKIN cycle time	t_{SYSCLK}	7.5	—	10	ns	1, 2
DSPCLKIN duty cycle	t_{KHK}/ t_{SYSCLK}	40	—	60	%	2
DSPCLKIN slew rate	—	1	—	4	V/ns	3

This figure provides the AC test load for the DDR3 and DDR3Lcontroller bus.

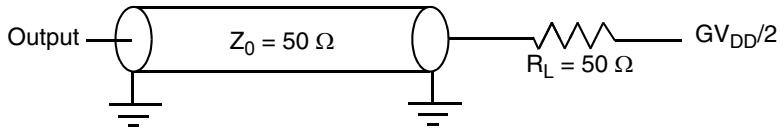

Figure 12. DDR3 and DDR3L Controller Bus AC Test Load

2.8.2.3 DDR3 and DDR3L SDRAM Differential Timing Specifications

This section describes the DC and AC differential timing specifications for the DDR3 SDRAM controller interface. Figure 13 shows the differential timing specification.

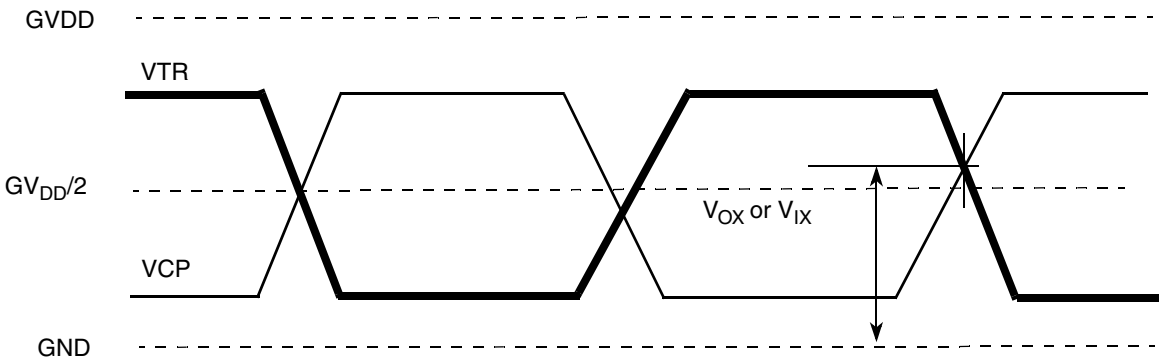

Figure 13. DDR3, and DDR3L SDRAM Differential Timing Specifications

NOTE

VTR specifies the true input signal (such as MCK or MDQS) and VCP is the complementary input signal (such as MCK_B or MDQS_B).

This table provides the DDR3 differential specifications for the differential signals MDQS/MDQS_B and MCK/MCK_B.

Table 26. DDR3 SDRAM Differential Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Note
Input AC Differential Cross-Point Voltage	V_{IXAC}	$0.5 \times GV_{DD} - 0.150$	$0.5 \times GV_{DD} + 0.150$	V	1
Output AC Differential Cross-Point Voltage	V_{OXAC}	$0.5 \times GV_{DD} - 0.115$	$0.5 \times GV_{DD} + 0.115$	V	1

Note:
1. I/O drivers are calibrated before making measurements.

This table provides the DDR3 differential specifications for the differential signals MDQS/MDQS_B and MCK/MCK_B.

Table 27. DDR3L SDRAM Differential Electrical Characteristics

Parameter	Symbol	Min	Max	Unit	Note
Input AC Differential Cross-Point Voltage	V_{IXAC}	$0.5 \times GV_{DD} - 0.135$	$0.5 \times GV_{DD} + 0.135$	V	1
Output AC Differential Cross-Point Voltage	V_{OXAC}	$0.5 \times GV_{DD} - 0.105$	$0.5 \times GV_{DD} + 0.105$	V	1

Note:
1. I/O drivers are calibrated before making measurements.

2.9 eSPI

This section describes the DC and AC electrical specifications for the SPI.

2.9.1 eSPI1 DC Electrical Characteristics

This table provides the DC electrical characteristics for the eSPI1 on the device operating on a 3.3 V power supply.

Table 28. eSPI1 DC Electrical Characteristics (CV_{DD} = 3.3 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	1
Input low voltage	V_{IL}	—	0.8	V	1
Input current (0 V ≤ V_{IN} ≤ CV_{DD})	I_{IN}	—	±10	μA	2
Output high voltage (I_{OH} = –6.0 mA)	V_{OH}	2.4	—	V	—
Output low voltage (I_{OL} = 6.0 mA)	V_{OL}	—	0.5	V	—
Output low voltage (IOL = 3.2 mA)	V_{OL}	—	0.4	V	—

Note:

1 The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.

2 The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

This table provides the DC electrical characteristics for the eSPI1 and eSPI2 on the device operating on a 1.8 V power supply.

Table 29. eSPI DC Electrical Characteristics (CV_{DD}, $X2V_{DD}$ = 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (0 V ≤ V_{IN} ≤ CV_{DD}/$X2V_{DD}$)	I_{IN}	—	±40	μA	2, 3
Output high voltage (I_{OH} = –6.0 mA)	V_{OH}	1.35	—	V	—
Output low voltage (I_{OL} = 6.0 mA)	V_{OL}	—	0.4	V	—

Note:

1 The min $V_{IL}$and max V_{IH} values are based on the respective min and max OV_{IN} values found in Table 3.

2 The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Section 2.1.2, "Recommended Operating Conditions."

3 eSPI1 is powered on CV_{DD}, SPI2 is on $X2V_{DD}$ (see Table 3).

2.9.2 eSPI1 AC Timing Specifications

This table provides the eSPI1 input and output AC timing specifications.

Table 30. eSPI1 AC Timing Specifications

For recommended operating conditions, see Table 3.

Characteristic	Symbol[1]	Min	Max	Unit	Note
eSPI outputs—Master data (internal clock) hold time	t_{NIKHOX}	0.5 + ($t_{PLATFORM\_CLK}$/2)	—	ns	2

2.10.2 DUART AC Electrical Specifications

This table provides the AC timing parameters for the DUART interface.

Table 33. DUART AC Timing Specifications

Parameter	Value	Unit	Note
Minimum baud rate	CCB clock/1,048,576	baud	1
Maximum baud rate	CCB clock/16	baud	2
Oversample rate	16	—	3

Note:

1. CCB clock refers to the platform clock.
2. Actual attainable baud rate is limited by the latency of interrupt processing.
3. The middle of a start bit is detected as the 8^{th} sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each 16^{th} sample.

2.11 Ethernet: Enhanced Three-Speed Ethernet (eTSEC)

This section provides the AC and DC electrical characteristics for enhanced three-speed Ethernet10/100/1000 controller and MII management.

2.11.1 SGMII Interface Electrical Characteristics

For SGMII interface electrical characteristics, see Section 2.20, "High-Speed Serial Interface (HSSI) DC Electrical Characteristics."

2.11.2 MII Management

2.11.2.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V and 2.5 V. The DC electrical characteristics for MDIO and MDC are provided in Table 34 and Table 35.

Table 34. MII Management DC Electrical Characteristics

At recommended operating conditions with LV_{DD} = 3.3 V.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	V	—
Input low voltage	V_{IL}	—	0.90	V	—
Input high current (LV_{DD} = Max, V_{IN} = 2.1 V)	I_{IH}	—	40	μA	1
Input low current (LV_{DD} = Max, V_{IN} = 0.5 V)	I_{IL}	–600	—	μA	1
Output high voltage (LV_{DD} = Min, I_{OH} = –1.0 mA)	V_{OH}	2.4	LV_{DD} + 0.3	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND	0.4	V	—

Note:

1. Note that the symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 2 and Table 3.

Table 35. MII Management DC Electrical Characteristics

At recommended operating conditions with LV_{DD} = 2.5 V.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.70	LV_{DD} + 0.3	V	—
Input low voltage	V_{IL}	–0.3	0.70	V	—
Input high current (V_{IN} = LV_{DD},)	I_{IH}	—	10	μA	1, 2
Input low current (V_{IN} = GND)	I_{IL}	–15	—	μA	—
Output high voltage (LV_{DD} = Min, IOH = –1.0 mA)	V_{OH}	2.00	LV_{DD} + 0.3	V	—
Output low voltage (LV_{DD} = Min, I_{OL} = 1.0 mA)	V_{OL}	GND – 0.3	0.40	V	—

Note:

1. EC1_MDC and EC1_MDIO operate on LV_{DD}.
2. Note that the symbol V_{IN}, in this case, represents the LV_{IN} and TV_{IN} symbols referenced in Table 3.

2.11.2.2 MII Management AC Electrical Specifications

This table provides the MII management AC timing specifications.

Table 36. MII Management AC Timing Specifications

Parameter	Symbol[1]	Min	Typ	Max	Unit	Note
MDC frequency	f_{MDC}	—	2.5	—	MHz	2
MDC period	t_{MDC}	—	400	—	ns	—
MDC clock pulse width high	t_{MDCH}	32	—	—	ns	—
MDC to MDIO delay	t_{MDKHDX}	$(16*t_{plb\_clk}) - 3$	—	$(16*t_{plb\_clk}) + 3$	ns	3, 4
MDIO to MDC setup time	t_{MDDVKH}	5	—	—	ns	—
MDIO to MDC hold time	t_{MDDXKH}	0	—	—	ns	—

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MDKHDX} symbolizes management data timing (MD) for the time t_{MDC} from clock reference (K) high (H) until data outputs (D) are invalid (X) or data hold time. Also, t_{MDDVKH} symbolizes management data timing (MD) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MDC} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. This parameter is dependent on the platform clock frequency (MIIMCFG [MgmtClk] field determines the clock frequency of the MgmtClk Clock EC_MDC).
3. This parameter is dependent on the platform clock frequency. The delay is equal to 16 platform clock periods ±3 ns. For example, with a platform clock of 333 MHz, the min/max delay is 48 ns ± 3 ns. Similarly, if the platform clock is 400 MHz, the min/max delay is 40 ns ± 3 ns.
4. t_{plb_clk} is the platform (CCB) clock.

Table 40. USB DC Electrical Characteristics (CV_{DD}/$X2V_{DD}$ = 3.3 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Output low voltage (CV_{DD}/$X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.3	V	—

Note:
1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN}/$X2V_{IN}$ values found in Table 3.
2. Note that the symbol CV_{IN} and $X2V_{IN}$ represent the input voltage of the power supplies. See Table 3.

This table provides the DC electrical characteristics for the ULPI interface when operating at 1.8 V.

Table 41. USB DC Electrical Characteristics (CV_{DD}/$X2V_{DD}$ = 1.8 V)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage	V_{IH}	1.25	—	V	1
Input low voltage	V_{IL}	—	0.6	V	1
Input current (CV_{IN}/$X2V_{IN}$ = 0 V or CV_{IN}/$X2V_{IN}$ = CV_{DD}/$X2V_{DD}$)	I_{IN}	—	±40	μA	2
Output high voltage (CV_{DD}/$X2V_{DD}$ = min, I_{OH} = –2 mA)	V_{OH}	1.35	—	V	—
Output low voltage (CV_{DD}/$X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:
1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max CV_{IN}/$X2V_{IN}$ values found in Table 3.
2. Note that the symbol CV_{IN}/$X2V_{IN}$ represents the input voltage of the supply. See Table 3.

2.12.2 USB AC Electrical Specifications

This table describes the general timing parameters of the USB interface of the device.

Table 42. USB General Timing Parameters (ULPI Mode)

For recommended operating conditions, see Table 3.

Parameter	Symbol[1]	Min	Max	Unit	Note
USB clock cycle time	t_{USCK}	15	—	ns	2, 3, 4, 5
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	2, 3, 4, 5
input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	2, 3, 4, 5
USB clock to output valid—all outputs	t_{USKHOV}	—	7	ns	2, 3, 4, 5
Output hold from USB clock—all outputs	t_{USKHOX}	2	—	ns	2, 3, 4, 5

2.20.1 SerDes

2.20.1.1 SerDes Signal Term Definitions

The SerDes interface uses differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals. Figure 36 shows how the signals are defined. Figure 36 shows the waveform for either a transmitter output (SD_TX[0:3] and SD_TX_B[0:3]) or a receiver input (SD_RX[0:3] and SD_RX_B[0:3]). Each signal swings between X volts and Y volts where X > Y.

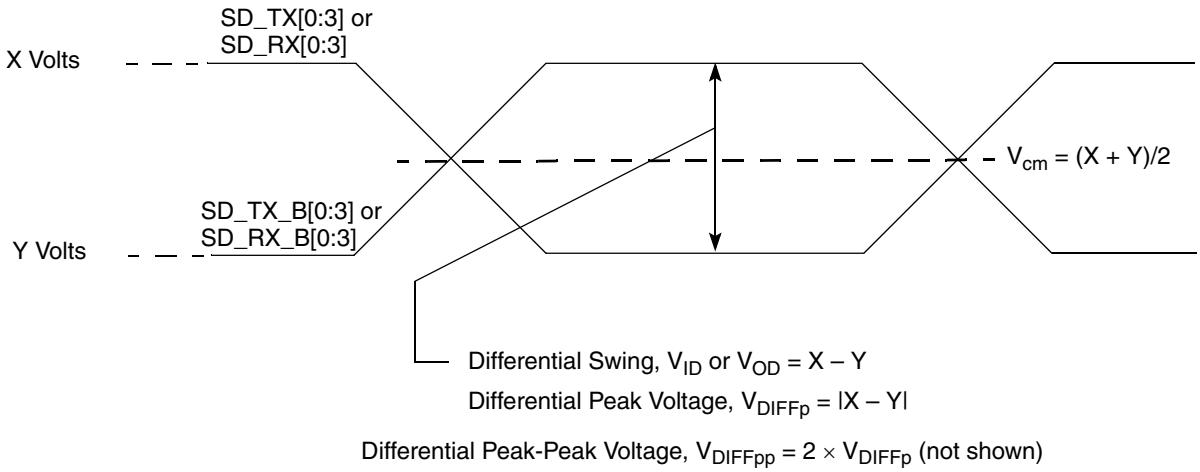

Figure 36. Differential Voltage Definitions for Transmitter/Receiver

This table lists the definitions based on this waveform. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

Table 66. Differential Signal Definitions

Term	Definition
Single-Ended Swing	The transmitter output signals and the receiver input signals SD_TX[0:3], SD_TX_B[0:3], SD_RX[0:3] and SD_RX_B[0:3] each have a peak-to-peak swing of X – Y volts. This is also referred to as each signal wire's single-ended swing.
Differential Output Voltage, VOD (or Differential Output Swing):	The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SD\_TX[0:3]} - V_{SD\_TX\_B[0:3]}$. The V_{OD} value can be either positive or negative.
Differential Input Voltage, VID (or Differential Input Swing)	The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SD\_RX[0:3]} - V_{SD\_RX\_B[0:3]}$. The V_{ID} value can be either positive or negative.
Differential Peak Voltage, V_{DIFFp}	The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, V_{DIFFp} = |X– Y| volts.
Differential Peak-to-Peak, $V_{DIFFp-p}$	Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p}$ = 2 × V_{DIFFp} = 2 × |(A – B)| volts, which is twice the differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p}$ = 2 × |V_{OD}|.

Table 74. SGMII DC Transmitter Electrical Characteristics (continued)

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Output differential voltage	$\|V_{OD}\|$	0.64 × Nom	333	1.45 × Nom	mV	• The $\|V_{OD}\|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$ = 1.0V, no common mode offset variation (V_{OS} = 500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TXn and SD_TX_Bn. • Amplitude setting: L[0:3]TECR0[AMD_RED] = 0b001100
Output differential voltage	$\|V_{OD}\|$	0.64 × Nom	292	1.45 × Nom	mV	• The $\|V_{OD}\|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$=1.0V, no common mode offset variation (V_{OS} =500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TXn and SD_TX_Bn. • Amplitude setting: L[0:3]TECR0[AMD_RED] = 0b001111
Output differential voltage	$\|V_{OD}\|$	0.64 × Nom	250	1.45 × Nom	mV	• The $\|V_{OD}\|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$=1.0V, no common mode offset variation (V_{OS} =500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TXn and SD_TX_Bn. • Amplitude setting: L[0:3]TECR0[AMD_RED] = 0b010011
Output impedance (single-ended)	R_O	40	50	60	Ω	—
Output high voltage	V_{OH}	—	—	1.5 × $\|V_{OD}$, max|	mV	—
Output low voltage	V_{OL}	$\|V_{OD}\|$, min/2	—	—	mV	—

Table 75 describes the SGMII SerDes receiver AC-coupled DC electrical characteristics.

Table 75. SGMII DC Receiver Electrical Characteristics[1,2]

Parameter	Symbol	Min	Nom	Max	Unit	Condition
Input differential voltage[3]	$V_{RX\_DIFFp\text{-}p}$	100	—	1200	mV	L[0:3]GCR1[RECTL_SIGD] = 0b001
		175	—	1200	mV	L[0:3]GCR1[RECTL_SIGD] = 0b100
Loss of signal threshold[4]	VLOS	30	—	100	mV	L[0:3]GCR1[RECTL_SIGD] = 0b001
		65	—	175	mV	L[0:3]GCR1[RECTL_SIGD] = 0b100
Receiver differential input impedance	Z_{RX_DIFF}	80	—	120	Ω	—

Note:

1. The supply voltage is 1.0 V.
2. Input must be externally AC-coupled.
3. $V_{RX\_DIFFp\text{-}p}$ is also referred to as peak-to-peak input differential voltage.
4. The concept of this parameter is equivalent to the Electrical Idle Detect Threshold parameter in the PCI Express interface. Refer to the PCI Express Differential Receiver (RX) Input Specifications section of the *PCI Express Specification* document. for details.

Table 78. PCI Express 2.0 (2.5 Gbps) Differential Receiver (Rx) Input AC Specifications (continued)

Parameter	Symbol	Min	Nom	Max	Unit	Comments

Note:

1 No test load is necessarily associated with this value.

2 Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 47 should be used as the Rx device when taking measurements. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.

3 A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.

4 It is recommended that the recovered Tx UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

Table 79. PCI Express 2.0 (5.0 Gbps) Differential Transmitter (Tx) Output AC Specifications

Parameter	Symbol	Min	Nom	Max	Unit	Comments
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See note 1.
Minimum Tx eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum Transmitter jitter can be derived as: $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. See notes 2 and 3.
Tx RMS deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	—	—	0.15	ps	—
Tx RMS deterministic jitter < 1.5 MHz	$T_{TX-LF-RMS}$	—	3.0	—	ps	Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 4.

Note:

1 No test load is necessarily associated with this value.

2 Specified at the measurement point into a timing and voltage test load as shown in Figure 47 and measured over any 250 consecutive Tx UIs.

3 A T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-MAX-JITTER}$ = 0.25 UI for the Transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

4 The DSP device SerDes transmitter does not have a built-in C_{TX}. An external AC coupling capacitor is required.

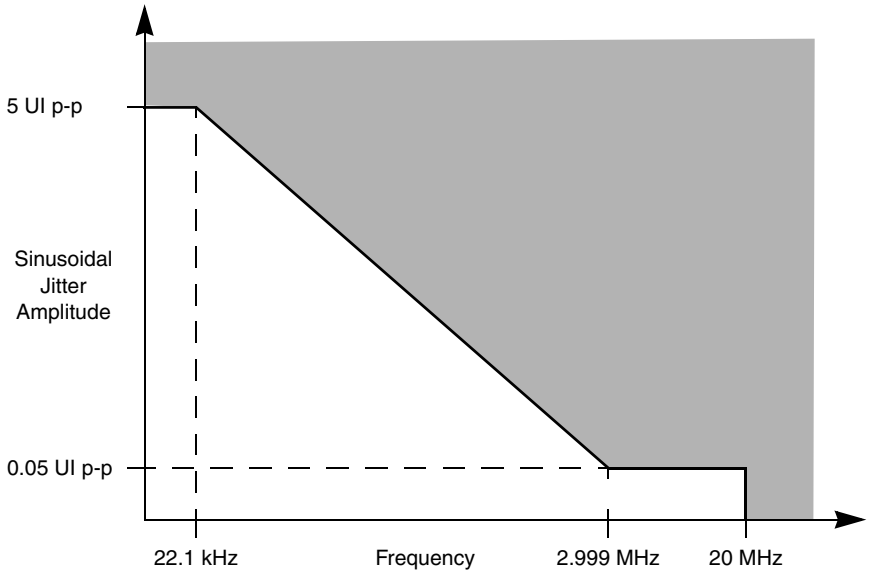

Figure 46. Single Frequency Sinusoidal Jitter Limits for Baud Rate 5.0 Gbps

2.20.3.6 Compliance Test and Measurement Load

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SD_TX*n* and SD_TX_B*n*) or at the receiver inputs (SD_RX*n* and SD_RX*n*_B). The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 47.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D– package pins.

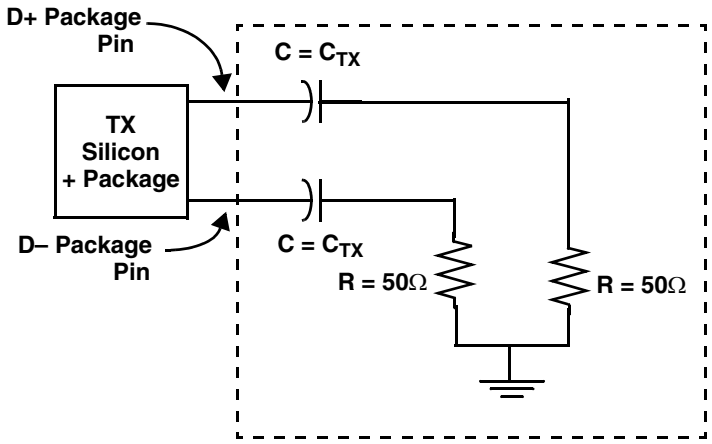

Figure 47. Compliance Test/Measurement Load

3.13.2 Temperature Diode

The chip has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461A™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment.

The following are the specifications of the chip's on-board temperature diode:

Operating range: 10 – 230μA

Ideality factor over 13.5 – 220 μA: n = 1.007 ± 0.008

3.14 Security Fuse Processor

This device implements the QorIQ platform's Trust Architecture, supporting capabilities such as secure boot. Use of the Trust Architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the Trust Architecture and SFP can be found in the *BSC9132 QorIQ Qonverge Multicore Baseband Processor Reference Manual*.

In order to program SFP fuses, the user is required to supply 1.5 V to the POV_{DD1} pin per Section 2.2, "Power Sequencing." POV_{DD1} should only be powered for the duration of the fuse programming cycle, with a per device limit of one fuse programming cycle. All other times POV_{DD1} should be connected to GND. The sequencing requirements for raising and lowering POV_{DD1} are shown in Figure 8. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

Users not implementing the QorIQ platform's Trust Architecture features are not required to program fuses and should connect POV_{DD1} to GND.

4 Package Information

The following section describes the detailed content and mechanical description of the package.

4.1 Package Parameters

The package parameters are provided in the following list. The package type is plastic ball grid array (FC-PBGA).

Package outline	23 mm × 23 mm
Interconnects	780
Pitch	0.8 mm
Ball diameter (typical)	0.4 mm

- *e500 PowerPC Core Reference Manual* (E500CORERM)

7 Revision History

Table 115. Document Revision History

Rev	Date	Substantive Change(s)
1	08/2014	Updated Table 1, “BSC9132 Pinout Listing.”
0	03/2014	Initial public release.