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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e500
Number of Cores/Bus Width	2 Core, 32-Bit
Speed	1.333GHz
Co-Processors/DSP	Signal Processing; SC3850 - Dual
RAM Controllers	DDR3, DDR3L
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	780-BFBGA, FCBGA
Supplier Device Package	780-FCBGA (23x23)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=bsc9132nxn7mnmb

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
D2_MDQ13	Data	AF9	I/O	G2VDD	—
D2_MDQ14	Data	AF8	I/O	G2VDD	—
D2_MDQ15	Data	AE9	I/O	G2VDD	—
D2_MDQ16	Data	AG13	I/O	G2VDD	—
D2_MDQ17	Data	AD11	I/O	G2VDD	—
D2_MDQ18	Data	AD10	I/O	G2VDD	—
D2_MDQ19	Data	AG10	I/O	G2VDD	—
D2_MDQ20	Data	AE12	I/O	G2VDD	—
D2_MDQ21	Data	AF12	I/O	G2VDD	—
D2_MDQ22	Data	AH13	I/O	G2VDD	—
D2_MDQ23	Data	AF11	I/O	G2VDD	—
D2_MDQ24	Data	AD14	I/O	G2VDD	—
D2_MDQ25	Data	AC12	I/O	G2VDD	—
D2_MDQ26	Data	AC14	I/O	G2VDD	—
D2_MDQ27	Data	AB14	I/O	G2VDD	—
D2_MDQ28	Data	AB12	I/O	G2VDD	—
D2_MDQ29	Data	AD15	I/O	G2VDD	—
D2_MDQ30	Data	AD12	I/O	G2VDD	—
D2_MDQ31	Data	AC13	I/O	G2VDD	—
D2_MDM00	Data Mask	AB8	O	G2VDD	—
D2_MDM01	Data Mask	AD9	O	G2VDD	—
D2_MDM02	Data Mask	AH12	O	G2VDD	—
D2_MDM03	Data Mask	AB13	O	G2VDD	—
D2_MDQS00	Data Strobe	AG8	I/O	G2VDD	—
D2_MDQS01	Data Strobe	AE10	I/O	G2VDD	—
D2_MDQS02	Data Strobe	AG11	I/O	G2VDD	—
D2_MDQS03	Data Strobe	AE13	I/O	G2VDD	—
D2_MDQS_B00	Data Strobe	AH8	I/O	G2VDD	—
D2_MDQS_B01	Data Strobe	AF10	I/O	G2VDD	—
D2_MDQS_B02	Data Strobe	AH11	I/O	G2VDD	—
D2_MDQS_B03	Data Strobe	AF13	I/O	G2VDD	—
D2_MBA00	Bank Select	AC2	O	G2VDD	—
D2_MBA01	Bank Select	AB4	O	G2VDD	—
D2_MBA02	Bank Select	AB3	O	G2VDD	—
D2_MA00	Address	AB6	O	G2VDD	—
D2_MA01	Address	AA5	O	G2VDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
D2_MA02	Address	AB2	O	G2VDD	—
D2_MA03	Address	AG2	O	G2VDD	—
D2_MA04	Address	AA3	O	G2VDD	—
D2_MA05	Address	AG1	O	G2VDD	—
D2_MA06	Address	AE3	O	G2VDD	—
D2_MA07	Address	AF1	O	G2VDD	—
D2_MA08	Address	AC1	O	G2VDD	—
D2_MA09	Address	AD2	O	G2VDD	—
D2_MA10	Address	AA4	O	G2VDD	—
D2_MA11	Address	AD3	O	G2VDD	—
D2_MA12	Address	AC4	O	G2VDD	—
D2_MA13	Address	AD5	O	G2VDD	—
D2_MA14	Address	AE2	O	G2VDD	—
D2_MA15	Address	AE1	O	G2VDD	—
D2_MWE_B	Write Enable	AC6	O	G2VDD	—
D2_MRAS_B	Row Address Strobe	AD4	O	G2VDD	—
D2_MCAS_B	Column Address Strobe	AC5	O	G2VDD	—
D2_MCS_B00	Chip Select	AA6	O	G2VDD	—
D2_MCS_B01	Chip Select	AA7	O	G2VDD	—
D2_MCS_B02	Chip Select	AF3	O	G2VDD	—
D2_MCS_B03	Chip Select	AF4	O	G2VDD	—
D2_MCKE00	Clock Enable	AH3	O	G2VDD	—
D2_MCKE01	Clock Enable	AH5	O	G2VDD	—
D2_MCK00	Clock	AE5	O	G2VDD	—
D2_MCK01	Clock	AG6	O	G2VDD	—
D2_MCK02	Clock	AE7	O	G2VDD	—
D2_MCK_B00	Clock Complements	AF5	O	G2VDD	—
D2_MCK_B01	Clock Complements	AH6	O	G2VDD	—
D2_MCK_B02	Clock Complements	AF7	O	G2VDD	—
D2_MODT00	On Die Termination	AH2	O	G2VDD	—
D2_MODT01	On Die Termination	AG3	O	G2VDD	—
D2_MDIC00	Driver Impedence Calibration	AE6	I/O	VSS	14
D2_MDIC01	Driver Impedence Calibration	AG5	I/O	G2VDD	14
D2_MECC00	ECC data	AE14	I/O	G2VDD	—
D2_MECC01	ECC data	AH14	I/O	G2VDD	—
D2_MECC02	ECC data	AB15	I/O	G2VDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT1_TX_FRAME/ GPO20	Transmit Frame	R4	O	X1VDD	4, 13
ANT1_RX_FRAME/ GPIO80	Receive Frame	R2	I	X1VDD	—
ANT1_DIO000	Data	L7	I/O	X1VDD	2
ANT1_DIO001	Data	N7	I/O	X1VDD	2, 4
ANT1_DIO002	Data	P7	I/O	X1VDD	2
ANT1_DIO003	Data	N5	I/O	X1VDD	2
ANT1_DIO004	Data	M7	I/O	X1VDD	
ANT1_DIO005	Data	M6	I/O	X1VDD	
ANT1_DIO006	Data	N6	I/O	X1VDD	2
ANT1_DIO007	Data	M3	I/O	X1VDD	2
ANT1_DIO008	Data	M2	I/O	X1VDD	2
ANT1_DIO009	Data	M5	I/O	X1VDD	2
ANT1_DIO010	Data	M1	I/O	X1VDD	2
ANT1_DIO011	Data	N3	I/O	X1VDD	2
ANT1_DIO100/ GPIO81	Data	P4	I	X1VDD	—
ANT1_DIO101/ GPIO82	Data	R1	I	X1VDD	—
ANT1_DIO102/ GPIO83	Data	R5	I	X1VDD	—
ANT1_DIO103/ GPIO84	Data	R7	I	X1VDD	—
ANT1_DIO104/ GPIO85	Data	T1	I	X1VDD	—
ANT1_DIO105/ GPIO86	Data	T3	I	X1VDD	—
ANT1_DIO106/ GPIO87/ IRQ10	Data	T5	I	X1VDD	—
ANT1_DIO107/ GPIO88/ IRQ11	Data	T6	I	X1VDD	—
ANT1_DIO108/ GPIO21/ IRQ08	Data	T7	I	X1VDD	—
ANT1_DIO109/ GPIO22/ IRQ09	Data	U1	I	X1VDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
ANT3_RX_CLK/ TDM2_TCK/ GPIO04	Receive Clock	D1	I	X2VDD	—
ANT3_TXNRX	TX_RX Control	C1	O	X2VDD	—
ANT3_ENABLE	Antenna Enable	D5	O	X2VDD	—
ANT3_TX_FRAME	Transmit Frame	E3	O	X2VDD	2
ANT3_RX_FRAME/ GPIO05	Receive Frame	C2	I	X2VDD	—
ANT3_DIO000/ CP_SYNC1	Data	B6	I/O	X2VDD	—
ANT3_DIO001/ CP_SYNC2	Data	A5	I/O	X2VDD	4, 13
ANT3_DIO002/ CP_LOS1	Data	B5	I/O	X2VDD	4, 13
ANT3_DIO003/ CP_LOS2	Data	A4	I/O	X2VDD	4, 13
ANT3_DIO004/ CP_TX_INT_B	Data	C4	I/O	X2VDD	4, 13
ANT3_DIO005/ CP_RCLK	Data	C5	I/O	X2VDD	4, 13
ANT3_DIO006/ CP_RX_INT_B	Data	A3	I/O	X2VDD	4, 13
ANT3_DIO007/ TDM2_TFS	Data	B3	I/O	X2VDD	—
ANT3_DIO008/ TDM2_RCK/ CKSTP0_OUT_B	Data	A2	I/O	X2VDD	—
ANT3_DIO009/ TDM2_RFS/ CKSTP1_OUT_B	Data	C3	I/O	X2VDD	4, 13
ANT3_DIO010/ TDM2_RXD	Data	D4	I/O	X2VDD	4, 13
ANT3_DIO011/ TDM2_TXD	Data	B1	I/O	X2VDD	—
RF Interface 4					
UART_RTS_B01/ SYS_DMA_DONE/ GPO45/ **ANT4_AGC**	AGC	Y27	O	OVDD	—
ANT4_TX_CLK	Transmit Clock	W7	O	X1VDD	—
ANT4_RX_CLK/ GPIO04/ TRIG_IN	Receive Clock	W5	I	X1VDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
IFC_ADDR18/ **GPO10**	General Purpose Output	H24	O	BVDD	—
IFC_ADDR19/ **GPO11**	General Purpose Output	H22	O	BVDD	—
IFC_ADDR20/ **GPO12**	General Purpose Output	H21	O	BVDD	—
IFC_ADDR21/ **GPO13**	General Purpose Output	J28	O	BVDD	—
IFC_ADDR22/ **GPO14**	General Purpose Output	J27	O	BVDD	—
IFC_ADDR23/ **GPO15**	General Purpose Output	J25	O	BVDD	—
IFC_ADDR24/ **GPO16**	General Purpose Output	J24	O	BVDD	—
IFC_ADDR25/ **GPO17**	General Purpose Output	J23	O	BVDD	—
IFC_ADDR26/ **GPO18**	General Purpose Output	J22	O	BVDD	—
ANT1_TXNRX/ TSEC_1588_PULSE_OUT2/ **GPO19**	General Purpose Output	P3	O	X1VDD	—
ANT1_TX_FRAME/ **GPO20**	General Purpose Output	R4	O	X1VDD	—
UART_RTS_B00/ PPS_LED/ **GPO43**	General Purpose Output	AB26	O	OVDD	—
UART_RTS_B01/ SYS_DMA_DONE/ **GPO45**/ ANT4_AGC	General Purpose Output	Y27	O	OVDD	—
IFC_CLE/ **GPO48**	General Purpose Output	L25	O	BVDD	—
IFC_OE_B/ **GPO49**	General Purpose Output	K23	O	BVDD	—
IFC_RB_B/ **GPO50**	General Purpose Output	K25	O	BVDD	—
IFC_WE_B/ **GPO52**	General Purpose Output	L26	O	BVDD	—
IFC_AVD/ **GPO54**	General Purpose Output	L28	O	BVDD	—
IFC_CS_B00/ **GPO55**	General Purpose Output	K21	O	BVDD	—
UART_SOUT01/ **GPO56**	General Purpose Output	W23	O	OVDD	—

Table 1. BSC9132 Pinout Listing (continued)

Signal	Signal Description	Pin Number	Pin Type	Power Supply	Note
X2VDD	eSPI2, USB, TDM1, TDM2, RF Parallel Interface	G2	—	X2VDD	—
X2VDD	eSPI2, USB, TDM1, TDM2, RF Parallel Interface	J4	—	X2VDD	—
X2VDD	eSPI2, USB, TDM1, TDM2, RF Parallel Interface	J8	—	X2VDD	—
X2VDD	eSPI2, USB, TDM1, TDM2, RF Parallel Interface	K6	—	X2VDD	—
X2VDD	eSPI2, USB, TDM1, TDM2, RF Parallel Interface	K8	—	X2VDD	—
X2VDD	eSPI2, USB, TDM1, TDM2, RF Parallel Interface	L8	—	X2VDD	—
X2VDD	eSPI2, USB, TDM1, TDM2, RF Parallel Interface	M8	—	X2VDD	—
XCOREVDD	SerDes Core Logic Supply	AH19	—	XCOREVDD	—
XCOREVDD	SerDes Core Logic Supply	AH23	—	XCOREVDD	—
XCOREVDD	SerDes Core Logic Supply	AH27	—	XCOREVDD	—
XCOREVDD	SerDes Core Logic Supply	AG25	—	XCOREVDD	—
XCOREVDD	SerDes Core Logic Supply	AF16	—	XCOREVDD	—
XCOREVDD	SerDes Core Logic Supply	AG17	—	XCOREVDD	—
XCOREVDD	SerDes Core Logic Supply	AG21	—	XCOREVDD	—
XPADVDD	SerDes Transceiver Supply	AA19	—	XPADVDD	—
XPADVDD	SerDes Transceiver Supply	AA20	—	XPADVDD	—
XPADVDD	SerDes Transceiver Supply	AF18	—	XPADVDD	—
XPADVDD	SerDes Transceiver Supply	AE20	—	XPADVDD	—
XPADVDD	SerDes Transceiver Supply	AF22	—	XPADVDD	—
XPADVDD	SerDes Transceiver Supply	AF26	—	XPADVDD	—
XPADVDD	SerDes Transceiver Supply	AE24	—	XPADVDD	—
Ground					
VSS	Platform and Core Ground	A9	—	—	—
VSS	Platform and Core Ground	A26	—	—	—
VSS	Platform and Core Ground	B2	—	—	—
VSS	Platform and Core Ground	B8	—	—	—
VSS	Platform and Core Ground	B11	—	—	—
VSS	Platform and Core Ground	B15	—	—	—
VSS	Platform and Core Ground	B21	—	—	—
VSS	Platform and Core Ground	C27	—	—	—
VSS	Platform and Core Ground	D17	—	—	—

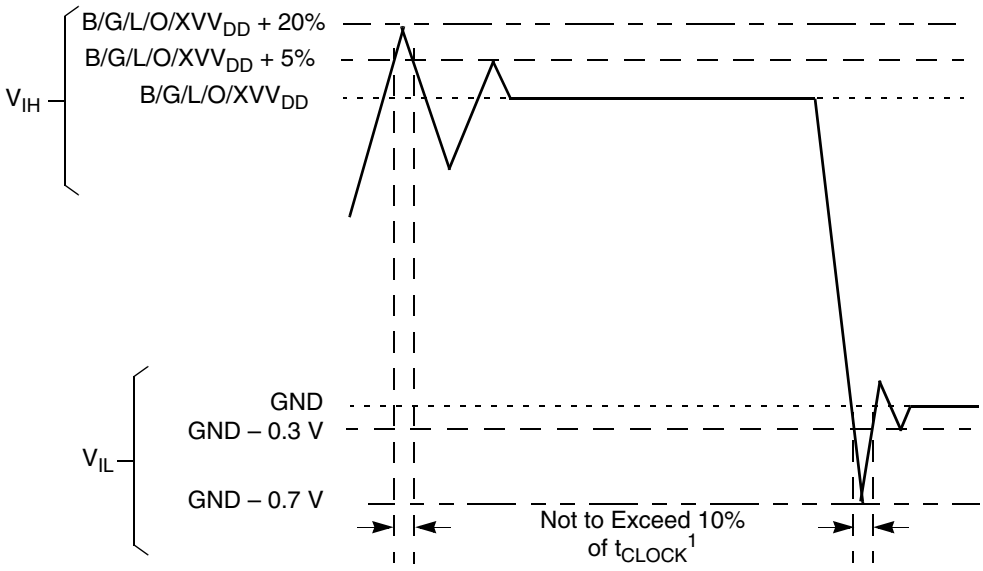
Table 3. Recommended Operating Conditions (continued)

Characteristic	Symbol	Recommended Value	Unit	Note

Note:

1. **Caution:** POV_{DD1} must be supplied 1.5 V and the device must operate in the specified fuse programming temperature range only during secure boot fuse programming. For all other operating conditions, POV_{DD1} must be tied to GND, subject to the power sequencing constraints shown in Section 2.2, "Power Sequencing."
2. USIM pins are multiplexed with the pins of other interfaces. Check Table 3 for which power supply is used (BV_{DD} or a CV_{DD}) for each particular USIM pin.
3. Unless otherwise stated in an interface's DC specifications, the maximum allowed input capacitance in this table is a general recommendation for signals.

This figure shows the undershoot and overshoot voltages at the interfaces.



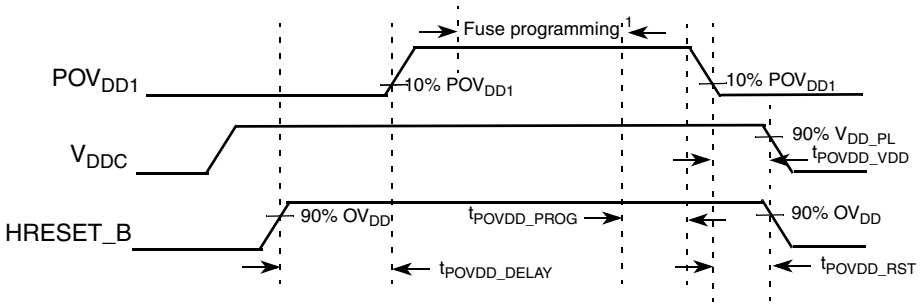
Note:

1. t_{CLOCK} refers to the clock period associated with the respective interface:
   For I^2C and JTAG, t_{CLOCK} references SYSCLK.
   For DDR, t_{CLOCK} references MCLK.
   For eTSEC, t_{CLOCK} references TSEC*n*_GTX_CLK125.
   For IFC, t_{CLOCK} references IFC_CLK.

Figure 7. Overshoot/Undershoot Voltage for $BV_{DD}/GV_{DD}/LV_{DD}/OV_{DD}/X1V_{DD}/X2V_{DD}$

The core voltage must always be provided at nominal 1 V (see Table 3 for actual recommended core voltage). Voltage to the processor interface I/Os are provided through separate sets of supply pins and must be provided at the voltages shown in Table 3. The input voltage threshold scales with respect to the associated I/O supply voltage. OV_{DD} and LV_{DD} based receivers are simple CMOS I/O circuits and satisfy appropriate LVCMOS type specifications. The DDR3 SDRAM interface uses a differential receiver referenced the externally supplied MV_{REF} signal (nominally set to $GV_{DD}/2$). The DDR DQS receivers cannot be operated in single-ended fashion. The complement signal must be properly driven and cannot be grounded.

This figure provides the POV_{DD1} timing diagram.



NOTE: POVDD must be stable at 1.5 V prior to initiating fuse programming.

Figure 8. POV_{DD1} Timing Diagram

This table provides information on the power-down and power-up sequence parameters for POV_{DD1}.

Table 5. POV_{DD1} Timing [5]

Driver Type	Min	Max	Unit	Note
t_{POVDD_DELAY}	1500	—	t_{SYSCLK}	1
t_{POVDD_PROG}	0	—	µs	2
t_{POVDD_VDD}	0	—	µs	3
t_{POVDD_RST}	0	—	µs	4

Note:

1. Delay required from the deassertion of HRESET_B to driving POV_{DD1} ramp up. Delay measured from HRESET_B deassertion at 90% OV_{DD} to 10% POV_{DD1} ramp up.
2. Delay required from fuse programming finished to POV_{DD1} ramp down start. Fuse programming must complete while POV_{DD1} is stable at 1.5 V. No activity other than that required for secure boot fuse programming is permitted while POV_{DD1} driven to any voltage above GND, including the reading of the fuse block. The reading of the fuse block may only occur while POV_{DD1} = GND. After fuse programming is completed, it is required to return POV_{DD1} = GND.
3. Delay required from POV_{DD1} ramp down complete to V_{DDC} ramp down start. POV_{DD1} must be grounded to minimum 10% POV_{DD1} before V_{DDC} is at 90% V_{DDC}.
4. Delay required from POV_{DD1} ramp down complete to HRESET_B assertion. POV_{DD1} must be grounded to minimum 10% POV_{DD1} before HRESET_B assertion reaches 90% OV_{DD}.
5. Only one secure boot fuse programming event is permitted per lifetime of a device.

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

In order to guarantee MCKE low during power-up, the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, the sequencing for GV_{DD} is not required.

2.7.5 RF Parallel Interface Clock Specifications

The following table lists the RF parallel interface clock DC electrical characteristics.

Table 16. RF Parallel Reference Clock DC Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Note
Input high voltage	V_{IH}	2.0	—	—	V	1
Input low voltage	V_{IL}	—	—	0.8	V	1
Input capacitance	C_{IN}	—	7	15	C	—
Input current (V_{IN}= 0 V or V_{IN} = V_{DDC})	I_{IN}	—	—	±50	μA	2

Note:
1. The max V_{IH}, and min V_{IL} values can be found in Table 3.
2. The symbol V_{IN}, in this case, represents the OV_{IN} symbol referenced in Table 3.

The following table lists the RF parallel interface clock AC electrical characteristics.

Table 17. RF Parallel Reference Clock AC Electrical Characteristics

At recommended operating conditions with OV_{DD} = 3.3 V ± 165 mV

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
ANT*n*_REF_CLK frequency	$f_{ANT\_REF\_CLK}$	—	19.2	—	MHz	—
ANT*n*_REF_CLK cycle time	$t_{ANT\_REF\_CLK}$	—	52	—	ns	—
ANT*n*_REF_CLK duty cycle	$t_{KHK}/t_{ANT\_REF\_CLK}$	48	50	52	%	—
ANT*n*_REF_CLK slew rate	—	1	—	4	V/ns	1
ANT*n*_REF_CLK peak period jitter	—	—	—	±100	ps	—
AC Input Swing Limits at 3.3 V OV_{DD}	ΔV_{AC}	1.9	—	—	V	—

Note:
1. Slew rate as measured from ±0.3 ΔV_{AC} at the center of peak to peak voltage at clock input.

2.7.6 Other Input Clocks

A description of the overall clocking of this device is available in the *BSC9132 QorIQ Qonverge Multicore Baseband Processor Reference Manual* in the form of a clock subsystem block diagram. For information about the input clock requirements of other functional blocks such as SerDes, Ethernet Management, eSDHC, and IFC, see the specific interface section.

2.8 DDR3 and DDR3L SDRAM Controller

This section describes the DC and AC electrical specifications for the DDR3 and DDR3L SDRAM controller interface. Note that the required GV_{DD}(typ) voltage is 1.5 V and 1.35 V when interfacing to DDR3 or DDR3L SDRAM, respectively.

2.8.2 DDR3 and DDR3L SDRAM Interface AC Timing Specifications

This section provides the AC timing specifications for the DDR SDRAM controller interface. The DDR controller supports DDR3 and DDR3L memories. Note that the required GV_{DD}(typ) voltage is 1.5 V when interfacing to DDR3 SDRAM, and the required GV_{DD}(typ) voltage is 1.35 V when interfacing to DDR3L SDRAM.

2.8.2.1 DDR3 and DDR3L SDRAM Interface Input AC Timing Specifications

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3 SDRAM.

Table 22. DDR3 SDRAM Interface Input AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage > 1200 MHz data rate ≤ 1200 MHz data rate	V_{ILAC}	—	 MVREFn – 0.150 MVREFn – 0.175	V	—
AC input high voltage > 1200 MHz data rate ≤ 1200 MHz data rate	V_{IHAC}	 MVREF*n* + 0.150 MVREF*n* + 0.175	—	V	—

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3L SDRAM.

Table 23. DDR3L SDRAM Interface Input AC Timing Specifications

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage > 1067 MHz data rate ≤ 1067 MHz data rate	V_{ILAC}	—	 MVREF*n* – 0.135 MVREF*n* – 0.160	V	—
AC input high voltage > 1067 MHz data rate ≤ 1067 MHz data rate	V_{IHAC}	 MVREF*n* + 0.135 MVREF*n* + 0.160	—	V	—

This table provides the input AC timing specifications for the DDR controller when interfacing to DDR3/3L SDRAM.

Table 24. DDR3 and DDR3L SDRAM Interface Input AC Timing Specifications

At recommended operating conditions with GV_{DD} of 1.5 V ± 5% for DDR3 or 1.35 V ± 5% for DDR3L.

Parameter	Symbol	Min	Max	Unit	Note
Controller Skew for MDQS—MDQ/MECC	t_{CISKEW}	—	—	ps	1
1333 MHz data rate		–125	125		
1200 MHz data rate		–147.5	147.5		
1066 MHz data rate		–170	170		
800 MHz data rate		–200	200		
667 MHz data rate		–240	240		

This figure shows the DDR3 and DDR3L SDRAM interface output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

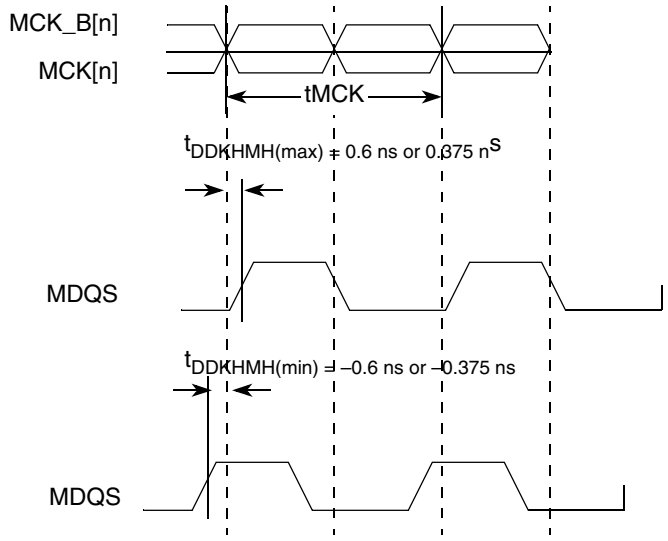


Figure 10. t_{DDKHMH} Timing Diagram

This figure shows the DDR3 and DDR3L SDRAM output timing diagram.

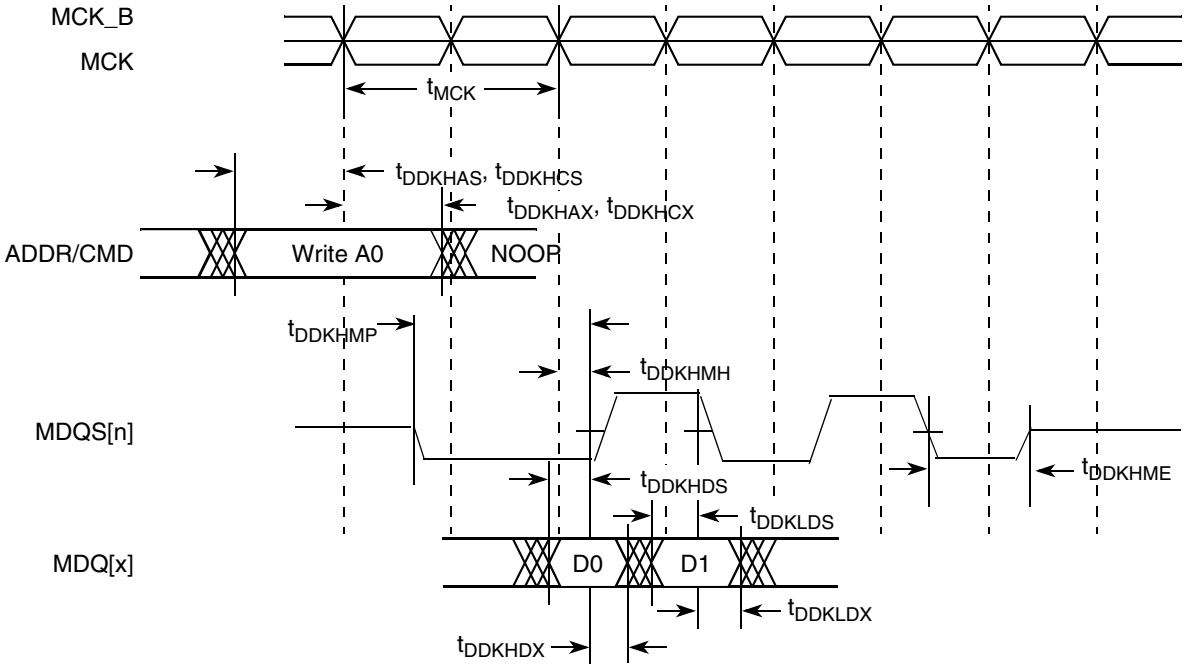


Figure 11. DDR3 and DDR3L Output Timing Diagram

Table 52. PIC DC Electrical Characteristics (1.8 V) (continued)

For recommended operating conditions, see Table 3.

Parameter	Symbol	Min	Max	Unit	Note
Output low voltage ($CV_{DD}/OV_{DD}/BV_{DD}/X1V_{DD}/X2V_{DD}$ = min, I_{OL} = 2 mA)	V_{OL}	—	0.4	V	—

Note:

1. Note that the min V_{IL} and max V_{IH} values are based on the respective min and max $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ values found in Table 3.
2. Note that the symbol $CV_{IN}/OV_{IN}/BV_{IN}/X1V_{IN}/X2V_{IN}$ represents the input voltage of the supply. See Table 3.

2.15.2 PIC AC Timing Specifications

This table provides the PIC input and output AC timing specifications.

Table 53. PIC Input AC Timing Specifications

For recommended operating conditions, see Table 3

Parameter	Symbol	Min	Max	Unit	Note
PIC inputs—minimum pulse width	t_{PIWID}	3	—	SYSCLK	1

Note:

1. PIC inputs and outputs are asynchronous to any visible clock. PIC outputs should be synchronized before use by any external synchronous logic. PIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge-triggered mode.

Table 58. I²C AC Electrical Specifications (continued)

For recommended operating conditions see Table 3. All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 56)

Parameter	Symbol[1]	Min	Max	Unit	Note

Note:

1. The symbols used for timing specifications herein follow the pattern $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the START condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the STOP condition (P) reaches the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time.
2. The requirements for I²C frequency calculation must be followed. See Freescale application note AN2919, “Determining the I2C Frequency Divider Ratio for SCL.”
3. As a transmitter, the device provides a delay time of at least 300 ns for the SDA signal (referred to as the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL to avoid unintended generation of a START or STOP condition. When the device acts as the I²C bus master while transmitting, it drives both SCL and SDA. As long as the load on SCL and SDA are balanced, the device does not generate an unintended START or STOP condition. Therefore, the 300 ns SDA output delay time is not a concern. If under some rare condition, the 300 ns SDA output delay time is required for the device as transmitter, application note AN2919 referred to in note 4 below is recommended.
4. The maximum t_{I2OVKL} has only to be met if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.

This figure provides the AC test load for the I²C.

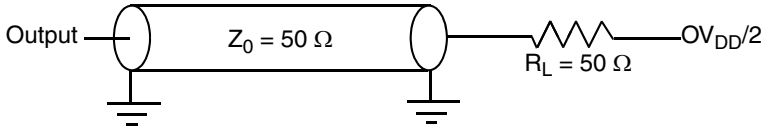


Figure 30. I²C AC Test Load

This figure shows the AC timing diagram for the I²C bus.

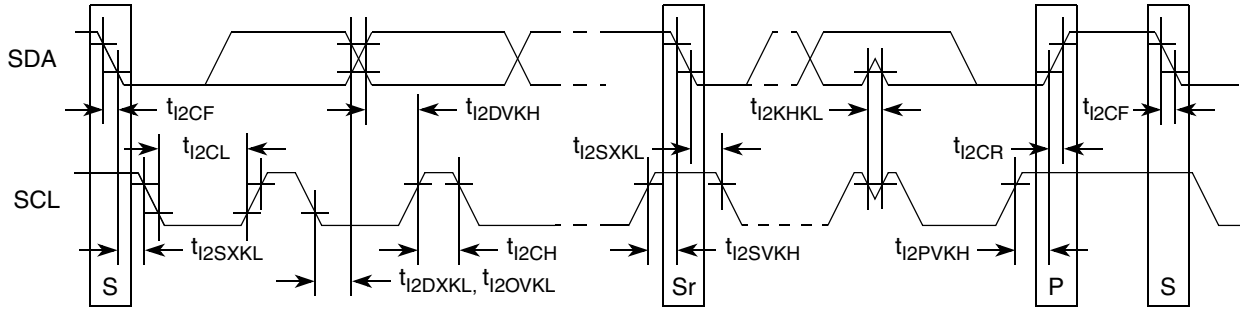


Figure 31. I²C Bus AC Timing Diagram

2.18 GPIO

This section describes the DC and AC electrical specifications for the GPIO interface.

2.20.1 SerDes

2.20.1.1 SerDes Signal Term Definitions

The SerDes interface uses differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals. Figure 36 shows how the signals are defined. Figure 36 shows the waveform for either a transmitter output (SD_TX[0:3] and SD_TX_B[0:3]) or a receiver input (SD_RX[0:3] and SD_RX_B[0:3]). Each signal swings between X volts and Y volts where X > Y.

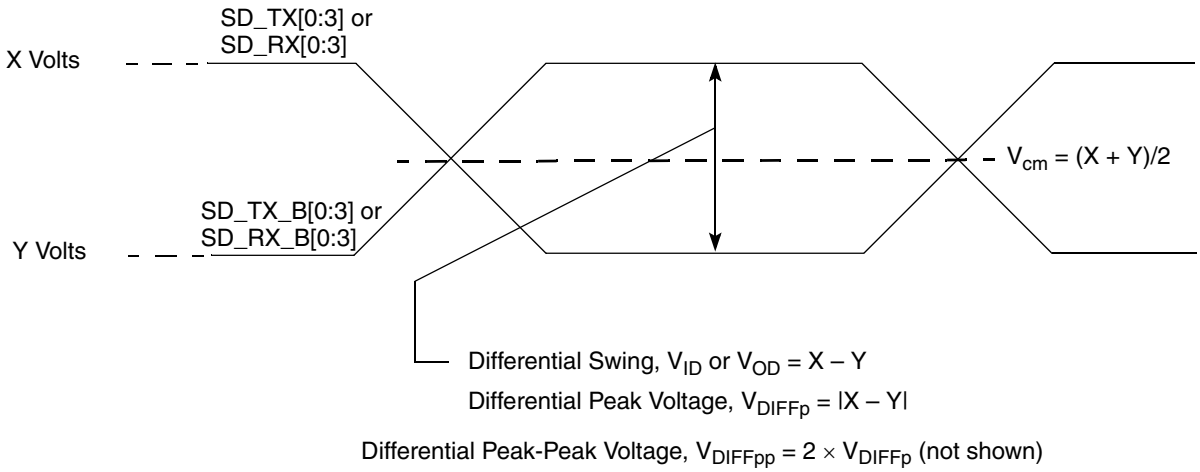


Figure 36. Differential Voltage Definitions for Transmitter/Receiver

This table lists the definitions based on this waveform. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

Table 66. Differential Signal Definitions

Term	Definition
Single-Ended Swing	The transmitter output signals and the receiver input signals SD_TX[0:3], SD_TX_B[0:3], SD_RX[0:3] and SD_RX_B[0:3] each have a peak-to-peak swing of X – Y volts. This is also referred to as each signal wire's single-ended swing.
Differential Output Voltage, VOD (or Differential Output Swing):	The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SD\_TX[0:3]} - V_{SD\_TX\_B[0:3]}$. The V_{OD} value can be either positive or negative.
Differential Input Voltage, VID (or Differential Input Swing)	The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SD\_RX[0:3]} - V_{SD\_RX\_B[0:3]}$. The V_{ID} value can be either positive or negative.
Differential Peak Voltage, V_{DIFFp}	The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, V_{DIFFp} = |X– Y| volts.
Differential Peak-to-Peak, $V_{DIFFp-p}$	Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p}$ = 2 × V_{DIFFp} = 2 × |(A – B)| volts, which is twice the differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p}$ = 2 × |V_{OD}|.

Table 74. SGMII DC Transmitter Electrical Characteristics (continued)

Parameter	Symbol	Min	Nom	Max	Unit	Conditions
Output differential voltage	$\|V_{OD}\|$	0.64 × Nom	333	1.45 × Nom	mV	• The $\|V_{OD}\|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$ = 1.0V, no common mode offset variation (V_{OS} = 500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TXn and SD_TX_Bn. • Amplitude setting: L[0:3]TECR0[AMD_RED] = 0b001100
Output differential voltage	$\|V_{OD}\|$	0.64 × Nom	292	1.45 × Nom	mV	• The $\|V_{OD}\|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$=1.0V, no common mode offset variation (V_{OS} =500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TXn and SD_TX_Bn. • Amplitude setting: L[0:3]TECR0[AMD_RED] = 0b001111
Output differential voltage	$\|V_{OD}\|$	0.64 × Nom	250	1.45 × Nom	mV	• The $\|V_{OD}\|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$=1.0V, no common mode offset variation (V_{OS} =500mV), SerDes transmitter is terminated with 100-Ω differential load between SD_TXn and SD_TX_Bn. • Amplitude setting: L[0:3]TECR0[AMD_RED] = 0b010011
Output impedance (single-ended)	R_O	40	50	60	Ω	—
Output high voltage	V_{OH}	—	—	1.5 × $\|V_{OD}$, max|	mV	—
Output low voltage	V_{OL}	$\|V_{OD}\|$, min/2	—	—	mV	—

Table 75 describes the SGMII SerDes receiver AC-coupled DC electrical characteristics.

Table 75. SGMII DC Receiver Electrical Characteristics[1,2]

Parameter	Symbol	Min	Nom	Max	Unit	Condition
Input differential voltage[3]	$V_{RX\_DIFFp\text{-}p}$	100	—	1200	mV	L[0:3]GCR1[RECTL_SIGD] = 0b001
		175	—	1200	mV	L[0:3]GCR1[RECTL_SIGD] = 0b100
Loss of signal threshold[4]	VLOS	30	—	100	mV	L[0:3]GCR1[RECTL_SIGD] = 0b001
		65	—	175	mV	L[0:3]GCR1[RECTL_SIGD] = 0b100
Receiver differential input impedance	Z_{RX_DIFF}	80	—	120	Ω	—

Note:

1. The supply voltage is 1.0 V.
2. Input must be externally AC-coupled.
3. $V_{RX\_DIFFp\text{-}p}$ is also referred to as peak-to-peak input differential voltage.
4. The concept of this parameter is equivalent to the Electrical Idle Detect Threshold parameter in the PCI Express interface. Refer to the PCI Express Differential Receiver (RX) Input Specifications section of the *PCI Express Specification* document. for details.

Table 78. PCI Express 2.0 (2.5 Gbps) Differential Receiver (Rx) Input AC Specifications (continued)

Parameter	Symbol	Min	Nom	Max	Unit	Comments

Note:

1 No test load is necessarily associated with this value.

2 Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 47 should be used as the Rx device when taking measurements. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.

3 A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the Transmitter and interconnect collected any 250 consecutive UIs. The TRX-EYE-MEDIAN-to-MAX-JITTER specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the Rx and Tx are not derived from the same reference clock, the Tx UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.

4 It is recommended that the recovered Tx UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

Table 79. PCI Express 2.0 (5.0 Gbps) Differential Transmitter (Tx) Output AC Specifications

Parameter	Symbol	Min	Nom	Max	Unit	Comments
Unit Interval	UI	199.94	200.00	200.06	ps	Each UI is 400 ps ± 300 ppm. UI does not account for spread spectrum clock dictated variations. See note 1.
Minimum Tx eye width	T_{TX-EYE}	0.75	—	—	UI	The maximum Transmitter jitter can be derived as: $T_{TX-MAX-JITTER} = 1 - T_{TX-EYE} = 0.25$ UI. See notes 2 and 3.
Tx RMS deterministic jitter > 1.5 MHz	$T_{TX-HF-DJ-DD}$	—	—	0.15	ps	—
Tx RMS deterministic jitter < 1.5 MHz	$T_{TX-LF-RMS}$	—	3.0	—	ps	Reference input clock RMS jitter (< 1.5 MHz) at pin < 1 ps
AC coupling capacitor	C_{TX}	75	—	200	nF	All transmitters must be AC coupled. The AC coupling is required either within the media or within the transmitting component itself. See note 4.

Note:

1 No test load is necessarily associated with this value.

2 Specified at the measurement point into a timing and voltage test load as shown in Figure 47 and measured over any 250 consecutive Tx UIs.

3 A T_{TX-EYE} = 0.75 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-MAX-JITTER}$ = 0.25 UI for the Transmitter collected over any 250 consecutive Tx UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total Tx jitter budget collected over any 250 consecutive Tx UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.

4 The DSP device SerDes transmitter does not have a built-in C_{TX}. An external AC coupling capacitor is required.

2.21.1.2 RF Parallel Interface AC Electrical Characteristics (eSPI2)

2.21.1.2.1 RF Parallel AC Data Interface

Table 89 provides the timing specifications for the RF parallel interface.

Table 89. RF Parallel Interface Timing Specification (3.3 V, 1.8 V)[1,2]

Parameter	Symbol	Min	Max	Unit	Note
Data_clk (MCLK) clock period	t_{PDCP}	16.276 (61.44)	—	ns (MHz)	—
Data_clk (MCLK) and fb_clk (FCLK) pulse width	t_{PDMP}	45% of t_{PDCP}	—	—	—
Delay between MCLK and FCLK at the external RFIC including trace delay	t_{PDCD}	—	7.32	ns	—
MCLK input to FCLK output delay at the BSC9132 BBIC	t_{PDMFD}	—	6.32	ns	—
Control/Data output valid time wrt FCLK during Tx from the BSC9132 BBIC	t_{PDOV}	—	6.0	ns	—
Control/Data hold from FCLK during Tx from the BSC9132 BBIC	t_{PDOX}	1.37	—	ns	3
Control/Data setup wrt MCLK	t_{PDIV}	2.5	—	ns	—
Control/Data hold wrt MCLK	t_{PDIX}	0.4	—	ns	—

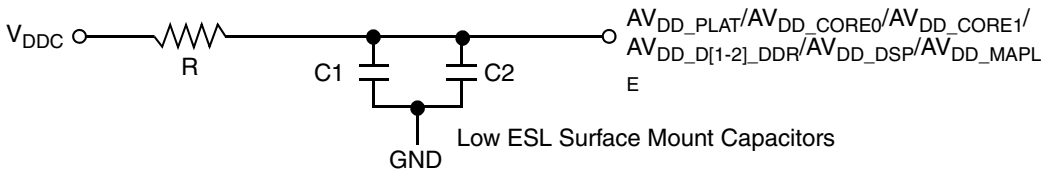
Note:

1 The max trace delay of MCLK from the external RFIC to the BSC9132 BBIC and FCK/TXNRX/ENABLE from BBIC to RFIC = 1 ns each.

2 The max allowable trace skew between MCLK/FCLK and the respective data/control is 70 ps.

3 1.37 ns includes 70 ps trace skew.

Figure 55 shows the core PLL (AV_{DD_CORE}) power supply filter circuit.



Notes:

R = 5Ω ± 5%

C1 = 10µF ± 10%, 603, X5R with ESL ≤ 0.5 nH

C2 = 1.0µF ± 10%, 402 X5R with ESL ≤ 0.5 nH

This circuit applies for system PLL, core PLL, DDR PPLL, and DSP PLL.

Figure 55. PLL Power Supply Filter Circuit

The AVDD_SRDSn signals provides power for the analog portions of the SerDes PLL. Use separate islands (that is, very wide traces) for each PLL bank's SD*n*AGND and SD*n*AVDD connections. The ground islands/wide traces of different PLL banks are to be joined to a single ground plane either with an inductor or through a 0 Ω resistance. While it is possible to connect these islands together to a single supply (possibly via a resistor or ferrite bead), it would be best for this connection to be formed by multiple single-point connections which are as close to the source (and as far away from the chip) as possible. The multiple single-point connections can be optimized as thick multiple wide connections to provide a good return path. The user should simulate the return path impedance and then take appropriate PCB layout tradeoff decisions. Additionally, one should maintain low noise and good stability of the SD*n*AVDD. The user should not place any digital or other bank traces near the PLL power and ground planes.

For maximum effectiveness, the filter circuit should be placed as closely as possible to the SDAVDD ball to ensure it filters out as much noise as possible. The ground connection should be near the SDAVDD ball. To provide effective bypass capacitance at high frequencies, these two islands/wide traces should be directly over each other and on the nearest layer (that is, layers 3 and 4 of a 6-layer PC board).

The capacitors are connected from SDAVDD to the ground plane. Only the surface mount technology (SMT) capacitors should be used to minimize inductance. Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance. The 2.2 nF capacitor is the closest to the package pin, followed by the two 2.2 µF capacitors, and finally the 1 Ω resistor to the board supply plane. The goal is to have a 2.2 nF decoupling capacitor within approximately 0.5 cm of each power pin.

3.5 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the system, and the device itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each VDD, BVDD, CVDD, OVDD, G1VDD, G2VDD, LVDD, RVDD, X1VDD, and X2VDD pin of the device. These decoupling capacitors should receive their power from separate VDD, BVDD, OVDD, G1VDD, G2VDD, LVDD, RVDD, X1VDD, X2VDD, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0201 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, BV_{DD}, OV_{DD}, GV_{DD}, and LV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

minimal signal quality or delay disruption. The default value for all configuration bits treated this way has been encoded such that a high voltage level puts the device into the default state and external resistors are needed only when non-default settings are required by the user.

Careful board layout with stubless connections to these pull-down resistors coupled with the large value of the pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

The platform PLL ratio and e500 PLL ratio configuration pins are not equipped with these default pull-up devices.

3.11 JTAG Configuration Signals

There are two JTAG ports:

- Power Architecture JTAG (TDI, TDO, TMS, TCK, and TRST_B)
- DSP JTAG (DSP_TDI, DSP_ TDO, DSP_TMS, DSP_TCK, and DSP_TRST_B)

Note that the DSP JTAG is available as dedicated I/O pins.

The Power Architecture JTAG is the primary JTAG interface of the chip. DSP JTAG is defined as optional debug interface. As seen in Table 112, the JTAG topology is selectable by static value driven on two pins—CFG_0_JTAG_MODE and CFG_1_JTAG_MODE.

Table 112. JTAG Topology

{CFG_0_JTAG_MODE, CFG_1_JTAG_MODE}	Uses Power Architecture Debug Header	Uses DSP Debug Header	JTAG Topology
00	Yes	No	Access Power Architecture domain and DSP domain using Power Architecture JTAG port
01	Yes	No	Access DSP domain using Power Architecture JTAG port
10	Yes	No	Access Power Architecture domain using Power Architecture JTAG port
11	Yes	Yes	Access Power Architecture domain using Power Architecture JTAG and DSP domain using DSP JTAG

Note: For boundary SCAN, set {CFG_0_JTAG_MODE, CFG_1_JTAG_MODE} = 10.

The TRST/DSP_TRST signal is optional in the IEEE 1149.1 specification, but is provided on the device. The device requires TRST/DSP_TRST to be asserted during reset conditions to ensure the JTAG boundary logic does not interfere with normal chip operation. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, generally systems assert TRST/DSP_TRST during the power-on reset flow. Simply tying TRST/DSP_TRST to HRESET_B is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP) function.

The COP function of the processor allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The arrangement shown in Figure 59 and Figure 60 allows the COP/ONCE port to independently assert HRESET_B or TRST, while ensuring that the target can drive HRESET_B as well.

3.13.2 Temperature Diode

The chip has a temperature diode on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461A™). These devices use the negative temperature coefficient of a diode operated at a constant current to determine the temperature of the microprocessor and its environment.

The following are the specifications of the chip's on-board temperature diode:

Operating range: 10 – 230μA

Ideality factor over 13.5 – 220 μA: n = 1.007 ± 0.008

3.14 Security Fuse Processor

This device implements the QorIQ platform's Trust Architecture, supporting capabilities such as secure boot. Use of the Trust Architecture features is dependent on programming fuses in the Security Fuse Processor (SFP). The details of the Trust Architecture and SFP can be found in the *BSC9132 QorIQ Qonverge Multicore Baseband Processor Reference Manual*.

In order to program SFP fuses, the user is required to supply 1.5 V to the POV_{DD1} pin per Section 2.2, "Power Sequencing." POV_{DD1} should only be powered for the duration of the fuse programming cycle, with a per device limit of one fuse programming cycle. All other times POV_{DD1} should be connected to GND. The sequencing requirements for raising and lowering POV_{DD1} are shown in Figure 8. To ensure device reliability, fuse programming must be performed within the recommended fuse programming temperature range per Table 3.

Users not implementing the QorIQ platform's Trust Architecture features are not required to program fuses and should connect POV_{DD1} to GND.

4 Package Information

The following section describes the detailed content and mechanical description of the package.

4.1 Package Parameters

The package parameters are provided in the following list. The package type is plastic ball grid array (FC-PBGA).

Package outline	23 mm × 23 mm
Interconnects	780
Pitch	0.8 mm
Ball diameter (typical)	0.4 mm