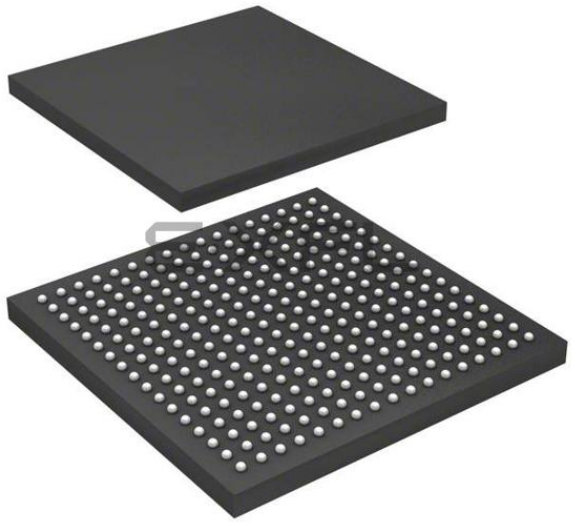

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	ARM926EJ-S
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	454MHz
Co-Processors/DSP	Data; DCP
RAM Controllers	LVDDR, LVDDR2, DDR2
Graphics Acceleration	No
Display & Interface Controllers	Keypad, LCD, Touchscreen
Ethernet	10/100Mbps (1)
SATA	-
USB	USB 2.0 + PHY (2)
Voltage - I/O	1.8V, 3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	Boot Security, Cryptography, Hardware ID
Package / Case	289-LFBGA
Supplier Device Package	289-MAPBGA (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcimx285avm4b

Table 4. i.MX28 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
LCDIF	LCD Interface	Multimedia peripherals	The LCDIF provides display data for external LCD panels from simple text-only displays to WVGA, 16/18/24 bpp color TFT panels. The LCDIF supports all of these different interfaces by providing fully programmable functionality and sharing register space, FIFOs, and ALU resources at the same time. The LCDIF supports RGB (DOTCLK) modes as well as system mode including both VSYNC and WSYNC modes.
LRADC	Low resolution ADC module	Connectivity peripherals	The sixteen-channel 12-bit low-resolution ADC (LRADC) block is used for voltage measurement. Channels 0 – 6 measure the voltage on the seven application-dependent LRADC pins. The auxiliary channels can be used for a variety of uses, including a resistor-divider-based wired remote control, external temperature sensing, touch-screen, and other measurement functions.
OCOTP Controller	On-chip OTP controller	Security	The on-chip one-time-programmable (OCOTP) ROM serves the functions of hardware and software capability bits, Freescale operations and unique-ID, the customer-programmable cryptography key, and storage of various ROM configuration bits.
PINCTRL	Pin control and GPIO	System control peripherals	Used for general purpose input/output to external ICs. Each GPIO bank supports 32 bits of I/O.
PMU	Power management Unit (DC-DC)	Power management system	The i.MX28 integrates a comprehensive power supply subsystem, including the following features: • One integrated DC-DC converter that supports Li-Ion battery. • Four linear regulators directly power the supply rails from 5-V. • Linear battery charger for Li-Ion cells. • Battery voltage and brownout detection monitoring for VDDD, VDDA, VDDIO, VDD4P2 and 5-V supplies. • Integrated current limiter from 5-V power source. • Reset controller. • System monitors for temperature and speed. • Generates USB-Host 5-V from Li-Ion battery (using PWM). • Support for on-the-fly transitioning between 5-V and battery power. • VDD4P2, a nominal 4.2-V supply, is available when the i.MX28 is connected to a 5-V source and allows the DCDC to run from a 5-V source with a depleted battery. • The 4.2-V regulated output also allows for programmable current limits: – Battery Charge current + DCDC input current < the 5-V current limit – DCDC input current (which ultimately provides current to the on-chip and off-chip loads) as the priority and battery charge current is automatically reduced if the 5-V current limit is reached
PWM(8)	Pulse width modulation	Connectivity peripherals	There are eight PWM output controllers that can be used in place of GPIO pins. Applications include HSADC driving signals and LED & backlight brightness control. Independent output control of each phase allows 0, 1, or high-impedance to be independently selected for the active and inactive phases. Individual outputs can be run in lock step with guaranteed non-overlapping portions for differential drive applications.
PXP	Pixel Pipeline	Multimedia	The pixel pipeline (PXP) is used to perform alpha blending of graphic or video buffers with graphics data before sending to an LCD display. The PXP also supports image rotation for hand-held devices that require both portrait and landscape image support.

Table 4. i.MX28 Digital and Analog Modules (continued)

Block Mnemonic	Block Name	Subsystem	Brief Description
RTC	Real-time clock, alarm, watchdog	Clocks	The real-time clock (RTC) and alarm share a one-second pulse time domain. The watchdog reset and millisecond counter run on a one-millisecond time domain. The RTC, alarm, and persistent bits reside in a special power domain (crystal domain) that remains powered up even when the rest of the chip is in its powered-down state.
SAIF(2)	Serial audio interface	Connectivity peripherals	SAIF provides a half-duplex serial port for communication with a variety of serial devices, including industry-standard codecs and DSPs. It supports a continuous range of sample rates from 8 kHz–192 kHz using a high-resolution fractional divider driven by the PLL. Samples are transferred to/from the FIFO through the APBX DMA interface, a FIFO service interrupt, or software polling.
SPDIF	SPDIF	Connectivity peripherals	The Sony-Philips Digital Interface Format (SPDIF) transmitter module transmits data according to the SPDIF digital audio interface standard (IEC-60958).
SSP(4)	Synchronous serial port	Connectivity peripherals	The synchronous serial port is a flexible interface for inter-IC and removable media control and communication. The SSP supports master operation of SPI, Texas Instruments SSI; 1-bit, 4-bit, and 8-bit SD/SDIO/MMC and 1-bit and 4-bit MS modes. The SPI mode has enhancements to support 1-bit legacy MMC cards. SPI master dual (2-bit) and quad (4-bit) mode reads are also supported. The SSP also supports slave operation for the SPI and SSI modes. The SSP has a dedicated DMA channel in the bridge and can also be controlled directly by the CPU through PIO registers. Each of the four SSP modules is independent of the other and can have separate SSPCLK frequencies.
TIMROT	Timers and Rotary Decoder	Timer peripherals	This module implements four timers and a rotary decoder. The timers and decoder can take their inputs from any of the pins defined for PWM, rotary encoders, or certain divisions from the 32-kHz clock input. Thus, the PWM pins can be inputs or outputs, depending on the application.
USBOTG USBHOST	High-speed USB on-the-go	Connectivity peripherals	The USB module provides high-performance USB On-The-Go (OTG) and host functionality (up to 480 Mbps), compliant with the USB 2.0 specification and the OTG supplement. The module has DMA capabilities for handling data transfer between internal buffers and system memory. When the OTG controller works in device mode, it can only work in FS or HS mode. Two USB2.0 PHYs are also integrated (one for the OTG port, another for the host port.)
USBPHY	Integrated USB PHY	Connectivity peripherals	The integrated USB 2.0 PHY macrocells are capable of connecting to USB host/device systems at the USB low-speed (LS) rate of 1.5 Mbps, full-speed (FS) rate of 12 Mbps or at the USB 2.0 high-speed (HS) rate of 480 Mbps. The integrated PHYs provide a standard UTM interface. The USB_DP and USB_DN pins connect directly to a USB connector.

- Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- Table 6 gives stress ratings only—functional operation of the device is not implied beyond the conditions indicated in Table 8.

Table 6. DC Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Battery Pin	BATT, V_{DD4P2V}	–0.3	4.242	V
5-Volt Source Pin - transient, t<30ms, duty cycle <0.05%	V_{DD5V}	–0.3	7.00	V
5 Volt Source Pin - static	V_{DD5V}	–0.3	6.00	V
Analog Supply Voltage	V_{DDA}	–0.3	2.10	V
Digital Core Supply Voltage	V_{DDD}	–0.3	1.575	V
Non-EMI Digital I/O Supply	V_{DDIO}	–0.3	3.63	V
EMI Digital I/O Supply	$V_{DDIO.EMI}$	–0.3	3.63	V
DC-DC Converter[1]	DCDC_BATT	–0.3	BATT	V
Input Voltage on Any Digital I/O Pin Relative to Ground	—	–0.3	VDDIO+0.3	V
Input Voltage on USB_DP and USB_DN Pins Relative to Ground[2]	—	–0.3	3.63	V
Analog I/O absolute maximum ratings (exceptions: XTALI, XTALO, RTC_XTALI, RTC_XTALO)	—	–0.3	VDDIO+0.3	V
Storage Temperature	—	–40	125	°C

1 Application should include a Schottky diode between BATT and VDD4P2.

2 USB_DN and USB_DP can tolerate 5V for up to 24 hours. Note that while 5V is applied to USB_DN or USB_DP, LRADC readings can be corrupted.

Table 7 shows the electrostatic discharge immunity.

Table 7. Electrostatic Discharge Immunity

289-Pin BGA Package	Tested Level
Human Body Model (HBM)[1]	2 kV
Charge Device Model (CDM)[1]	500 V

1 HBM and CDM pass ESD testing per AEC-Q100.

3.1.2 DC Operating Conditions

Table 8 provides the DC recommended operating conditions.

Table 8. Recommended Power Supply Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Analog Core Supply Voltage	V_{DDA}	1.62	—	2.10	V
Digital Core Supply Voltage *Specification dependent on frequency.*[1, 2]	V_{DDD}	1.35	—	1.55	V
Digital Supply Voltages: • VDDIO33/VDDIO33_EMI • VDDIO18	V_{DDIO33}/V_{DDIO33_EMI}/V_{DDIO18}	 3.0 1.7	 — —	 3.6 1.9	V
EMI Digital I/O Supply Voltage: • DDR2/mDDR • LVDDR2	$V_{DDIO.EMI}$/V_{DDIO_EMIQ}	 1.7 1.425	 1.8 1.5	 1.9 1.625	V
Battery / DCDC Input Voltage—BATT, DCDC_BATT	BATT DCDC_BATT	3.10[3]	—	4.242	V
VDD5V Supply Voltage	—	4.75	5.00	5.25	V
Offstate Current:[4] • 32-kHz RTC off, BATT = 4.2 V • 32-kHz RTC on, BATT = 4.2 V	 — —	 — —	 21 23	 47 51	 µA µA

1 For optimum USB jitter performance, V_{DDD} = 1.35 V or greater.

2 V_{DDD} supply minimum voltage includes 75 mV guardband.

3 Tested with only the i.MX28 processor loading the MX28 PMU output rails during start up. With external loadings (for example, one DDR2 device and SD Card/NAND Flash), MX28 PMU was tested at BATT/DCDC_BATT > 3.30 V.

4 When the real-time clock is enabled, the chip consumes additional current in the OFF state to keep the crystal oscillator and the real-time clock running.

Table 9 provides the DC operating temperature conditions.

Table 9. Operating Temperature Conditions

Parameter[1, 2, 3]	Symbol	Min	Typ	Max	Unit
Automotive/Industrial Ambient Operating Temperature Range	T_A	–40	—	85	°C
Automotive/Industrial Junction Temperature Range	T_J	–40	—	105	°C

1 In most portable systems designs, battery and display specifications limits the operating range to well within these specifications. Most battery manufacturers recommend enabling battery charge only when the ambient temperature is between 0°C and 40°C. To ensure that battery charging does not occur outside the recommended temperature range, the system ambient temperature may be monitored by connecting a thermistor to the LRADC0 or LRADC6 pin on the i.MX28.

2 For applications powered by external 5V only, the Maximum Ambient Operating Temperature specified in Table 9 may not be achieved. Application developers need to do the worst-case power consumption estimation, and then calculate the Total On-chip Power Dissipation based on the equations specified in note 3 below.

Table 17. Frequency vs. Voltage for EMICLK—289-Pin BGA Package

VDDD (V)	$VDDD_{Brownout}$ (V)	EMICLK Fmax (MHz)	
		DDR2	mDDR
1.550	1.450	205.71	205.71
1.450	1.350	196.36	196.36
1.350	1.250	196.36	196.36

3.1.3 Fusebox Supply Current Parameters

Table 18 lists the fusebox supply current parameters.

Table 18. Fusebox Supply Current Parameters

Parameter	Symbol	Min	Typ	Max	Unit
eFuse Program Current[1] Current to program one eFuse bit efuse_vddq=2.5V	$I_{program}$	21.39	25.05	33.54	mA
eFuse Read Current[2] Current to read an 8-bit eFuse word vdd_fusebox = 3.3 V	I_{read}	—	—	4.07	mA

1 The current $I_{program}$ is during program time.

2 The current I_{read} is present for approximately 10 ns of the read access to the 8-bit word.

3.1.4 Interface Frequency Limits

Table 19 provides information for interface frequency limits.

Table 19. Interface Frequency Limits

Parameter	Min.	Typ.	Max.	Unit
JTAG: TCK Frequency of Operation	—	—	10	MHz
OSC24M_XTAL Oscillator	—	24.000	—	MHz
OSC32K_XTAL Oscillator	—	32.768/32.0	—	kHz

3.1.5 Power Modes

Table 20 describes the core, clock, and module settings for the different power modes of the processor.

Table 20. Power Mode Settings

Core/Clock/Module	Offstate	Standby	Run
ARM Core	Off	Off	On
USB0 PLL (System PLL)	Off	Off	On
OSC24M	Off	On	On

- Core via I.D: 0.068 mm, Core via plating 0.016 mm
- Flag: trace style with ground balls under the die connected to the flag
- Die Attach: 0.033 mm non-conductive die attach, k = 0.3 W/m K
- Mold Compound: generic mold compound, k = 0.9 W/m K

Table 21. Thermal Resistance Data

Rating			Value	Unit
Junction to ambient[1] natural convection	Single layer board (1s)	$R_{\theta JA}$	62	°C/W
Junction to ambient[1] natural convection	Four layer board (2s2p)	$R_{\theta JA}$	36	°C/W
Junction to ambient[1] (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	53	°C/W
Junction to ambient[1] (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	33	°C/W
Junction to boards[2]		$R_{\theta JB}$	24	°C/W
Junction to case (top)[3]		$R_{\theta JCtop}$	15	°C/W
Junction to package top[4]	Natural Convection	Ψ_{JT}	3	°C/W

1 Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-2 and JESD51-6. Thermal test board meets JEDEC specification for this package.

2 Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.

3 Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.

4 Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.3 I/O DC Parameters

This section includes the DC parameters of the following I/O types:

- DDR I/O: Mobile DDR (LPDDR1), standard 1.8 V DDR2, and low-voltage 1.5 V DDR2 (LVDDR2)
- General purpose I/O (GPIO)

3.3.1 DDR I/O DC Parameters

Table 22 shows the EMI digital pin DC characteristics.

NOTE

The current values and the I-V curves of the I/O DC characteristics are estimated based on an overly conservative device model. They are updated upon the measurement results of the first silicon.

Table 25. Digital Pin DC Characteristics for GPIO in 3.3-V Mode (continued)

Parameter	Symbol	Min	Max	Unit
10-K pull-up resistance[2]	Rpu10k	8	12	kΩ
47-K pull-up resistance	Rpu47k	39	56	kΩ

1 The conditions of the current measurements for all different drives are as follows:
IOL: at 0.4 V
IOH: at VDDIO * 0.8 V
Maximum corner for 3.3 V mode: 3.6 V, -40°C, fast process.
Minimum corner for 3.3 V mode: 3.0 V, 105°C, slow process.
8 gpio pins (LCD_D0-D7) and 2 gpio_clk pins (LCD_DOTCLK and LCD_WR_RWN) simultaneously loaded.

2 See the i.MX28 reference manual for detailed pull-up configuration of each I/O.

Table 26 shows the digital pin DC characteristics for GPIO in 1.8 V mode.

Table 26. Digital Pin DC Characteristics for GPIO in 1.8 V Mode

	Symbol	Min	Max	Unit
Input voltage high (DC)	VIH	0.7 × VDDIO18	VDDIO18	V
Input voltage low (DC)	VIL	—	0.3 × VDDIO18	V
Output voltage high (DC)	VOH	0.8 * VDDIO18	—	V
Output voltage low (DC)	VOL	—	0.2 × VDDIO18	V
Output source current[1] (DC) *gpio*	IOH – low	-2.2	—	mA
	IOH – medium	-3.5	—	mA
	IOH – high	-4.0	—	mA
Output sink current (DC) *gpio*	IOL – low	3.3	—	mA
	IOL – medium	7.0	—	mA
	IOL – high	7.5	—	mA
Output source current (DC) *gpio_clk*	IOH – low	-4.2	—	mA
	IOH – high	-6.0	—	mA
Output sink current (DC) *gpio_clk*	IOL – low	6.8	—	mA
	IOL – high	11.5	—	mA
10-K pull-up resistance[2]	Rpu10k	8	12	kΩ
47-K pull-up resistance	Rpu47k	39	56	kΩ

1 The condition of the current measurements for all different drives are as follows:
Maximum corner for 1.8 V mode: 1.9 V, -40°C, Fast process.
Minimum corner for 1.8 V mode: 1.7 V, 105°C, Slow process.
1 gpio pin (GPMI_D0) and 1 gpio_clk pin (GPMI_WRN) simultaneously loaded.

2 See the i.MX28 reference manual for detailed pull-up configuration of each I/O.

Table 28 shows the F-type GPIO AC timing and parameters.

Table 28. F-type GPIO

Parameters	Symbol	Test Voltage	Test Capacitance	Min Rise/Fall		Max Rise/Fall		Unit	Notes
Duty cycle	Fduty	—	—	—		—		%	—
Output pad transition times (maximum drive)	tpr	1.7~1.9V	10 pF	0.58	0.61	1.29	1.33	ns	—
		1.7~1.9V	20 pF	0.89	0.88	1.94	1.88		—
		1.7~1.9V	50 pF	1.83	1.59	3.88	3.39		—
		3.0~3.6V	10 pF	0.71	0.68	1.47	1.34		—
		3.0~3.6V	20 pF	1.02	1.04	2.11	1.99		—
		3.0~3.6V	50 pF	1.98	2.09	3.97	3.96		—
Output pad transition times (medium drive)	tpr	1.7~1.9V	10 pF	0.76	0.76	1.68	1.61	ns	—
		1.7~1.9V	20 pF	1.23	1.13	2.63	2.38		—
		1.7~1.9V	50 pF	2.66	2.18	5.61	4.6		—
		3.0~3.6V	10 pF	0.9	0.88	1.84	1.7		—
		3.0~3.6V	20 pF	1.36	1.4	2.76	2.67		—
		3.0~3.6V	50 pF	2.85	3.02	5.59	5.67		—
Output pad transition times (low drive)	tpr	1.7~1.9V	10 pF	1.32	1.26	2.88	2.72	ns	—
		1.7~1.9V	20 pF	2.27	1.98	4.84	4.23		—
		1.7~1.9V	50 pF	5.23	4.13	10.95	8.8		—
		3.0~3.6V	10 pF	1.46	1.55	3.05	3		—
		3.0~3.6V	20 pF	2.46	2.62	4.92	5.02		—
		3.0~3.6V	50 pF	5.56	5.96	10.78	11.22		—
Output pad slew rate (maximum drive)	tps	1.7~1.9V	10 pF	1.97	1.87	0.79	0.77	ns	—
		1.7~1.9V	20 pF	1.28	1.30	0.53	0.54		—
		1.7~1.9V	50 pF	0.62	0.72	0.26	0.30		—
		3.0~3.6V	10 pF	3.04	3.18	1.22	1.34		—
		3.0~3.6V	20 pF	2.12	2.08	0.85	0.90		—
		3.0~3.6V	50 pF	1.09	1.03	0.45	0.45		—
Output pad slew rate (medium drive)	tps	1.7~1.9V	10 pF	1.50	1.50	0.61	0.63	ns	—
		1.7~1.9V	20 pF	0.93	1.01	0.39	0.43		—
		1.7~1.9V	50 pF	0.43	0.52	0.18	0.22		—
		3.0~3.6V	10 pF	2.40	2.45	0.98	1.06		—
		3.0~3.6V	20 pF	1.59	1.54	0.65	0.67		—
		3.0~3.6V	50 pF	0.76	0.72	0.32	0.32		—

Table 28. F-type GPIO (continued)

Parameters	Symbol	Test Voltage	Test Capacitance	Min Rise/Fall		Max Rise/Fall		Unit	Notes
Output pad slew rate (low drive)	tps	1.7~1.9V	10 pF	1.44	1.51	0.59	0.63	ns	—
		1.7~1.9V	20 pF	0.84	0.96	0.35	0.40		—
		1.7~1.9V	50 pF	0.36	0.46	0.16	0.19		—
		3.0~3.6V	10 pF	1.48	1.39	0.59	0.60		—
		3.0~3.6V	20 pF	0.88	0.82	0.37	0.36		—
		3.0~3.6V	50 pF	0.39	0.36	0.17	0.16		—
Input pad average hysteresis	tih	1.7 V–1.9 V	—	100		75		mV	—
		3.0 V–3.6 V	—	100		50			—

Table 29 shows the CLK-type GPIO AC timing and parameters.

Table 29. CLK-Type GPIO

Parameters	Symbol	Test Voltage	Test Capacitance	Min Rise/Fall		Max Rise/Fall		units	Notes
Duty cycle	Fduty	—	—	—		—		%	—
Output pad transition times (maximum drive)	tpr	1.7~1.9V	10 pF	0.48	0.52	1.08	1.12	ns	—
		1.7~1.9V	20 pF	0.72	0.74	1.56	1.56		—
		1.7~1.9V	50 pF	1.41	1.28	3.04	2.7		—
		3.0~3.6V	10 pF	0.61	0.57	1.25	1.12		—
		3.0~3.6V	20 pF	0.85	0.85	1.73	1.63		—
		3.0~3.6V	50 pF	1.56	1.63	3.13	3.08		—
Output pad transition times (medium drive)	tpr	1.7~1.9V	10 pF	0.76	0.76	1.67	1.62	ns	—
		1.7~1.9V	20 pF	1.22	1.14	2.64	2.41		—
		1.7~1.9V	50 pF	2.66	2.2	5.61	4.62		—
		3.0~3.6V	10 pF	0.9	0.89	1.83	1.72		—
		3.0~3.6V	20 pF	1.37	1.41	2.77	2.69		—
		3.0~3.6V	50 pF	2.85	3.03	5.59	5.72		—
Output pad slew rate (maximum drive)	tps	1.7~1.9V	10 pF	2.38	2.19	0.94	0.91	ns	—
		1.7~1.9V	20 pF	1.58	1.54	0.65	0.65		—
		1.7~1.9V	50 pF	0.81	0.89	0.34	0.38		—
		3.0~3.6V	10 pF	3.54	3.79	1.44	1.61		—
		3.0~3.6V	20 pF	2.54	2.54	1.04	1.10		—
		3.0~3.6V	50 pF	1.38	1.33	0.58	0.58		—

3.5.6 FlexCAN AC Timing

Table 45 and Table 46 show voltage requirements for the FlexCAN transceiver Tx and Rx pins.

Table 45. Tx Pin Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
High-level output voltage	V_{OH}	2	—	Vcc[1] + 0.3	V
Low-level output voltage	V_{OL}	—	0.8	—	V

1 Vcc = +3.3 V ± 5%

Table 46. Rx Pin Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
High-level input voltage	V_{IH}	0.8 × Vcc[1]	—	Vcc[1]	V
Low-level input voltage	V_{IL}	—	0.4	—	V

1 Vcc = +3.3 V ± 5%

Figure 16 through Figure 19 show the FlexCAN timing, including timing of the standby and shutdown signals.

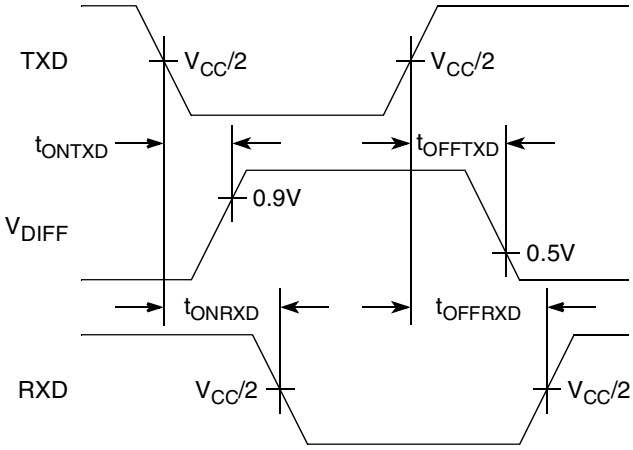


Figure 16. FlexCAN Timing Diagram

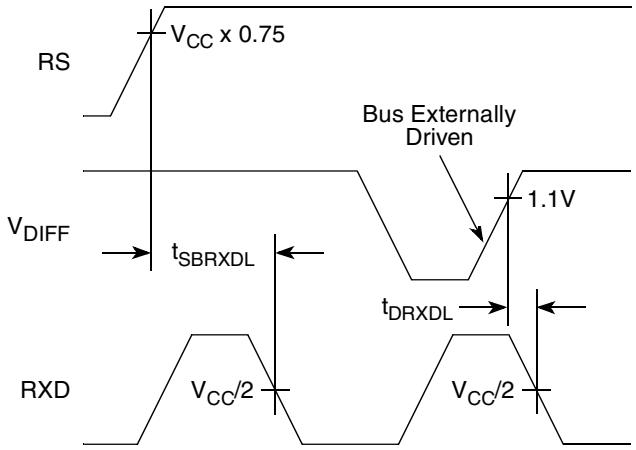


Figure 17. Timing Diagram for FlexCAN Standby Signal

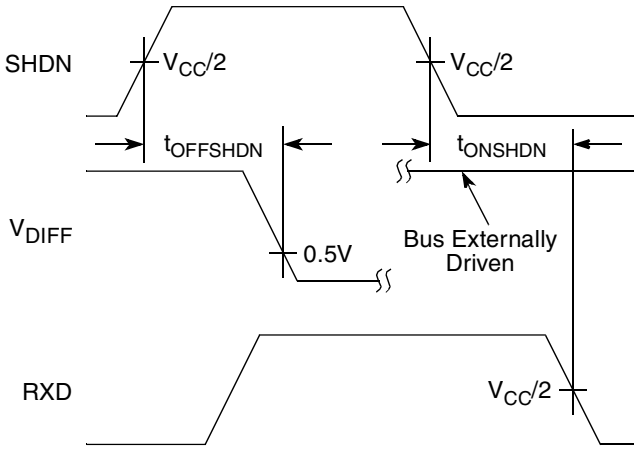


Figure 18. Timing Diagram for FlexCAN Shutdown Signal

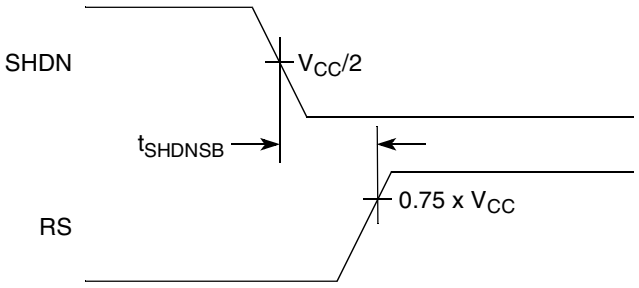


Figure 19. Timing Diagram for FlexCAN Shutdown-to-Standby Signal

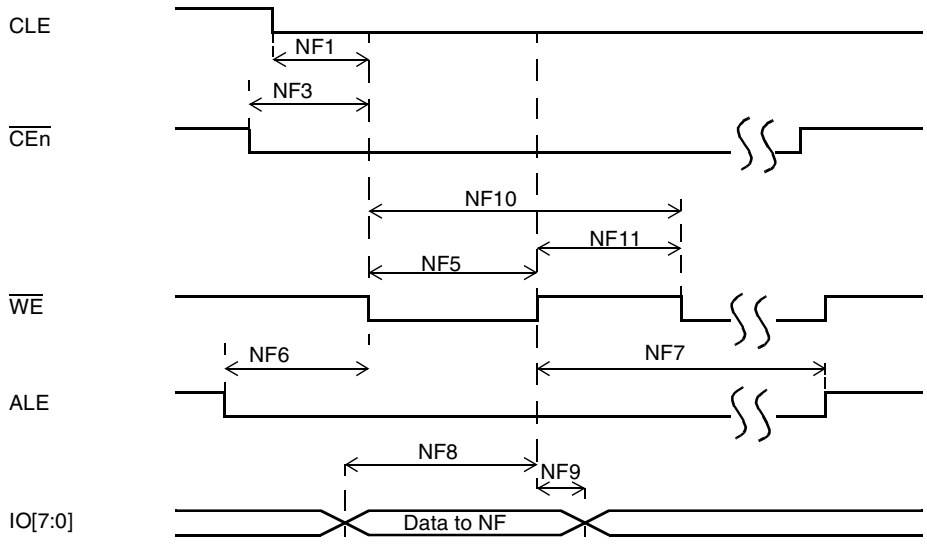


Figure 22. Write Data Latch Cycle Timing Diagram

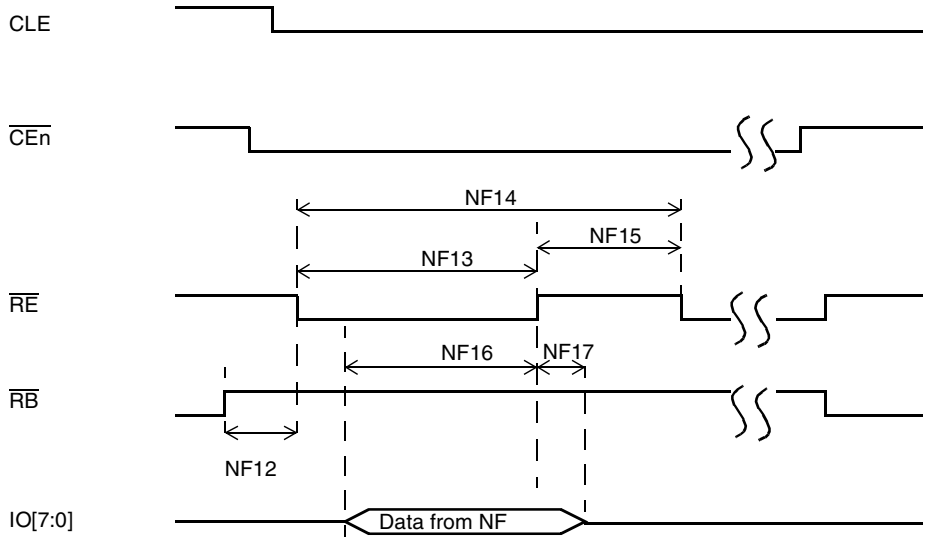
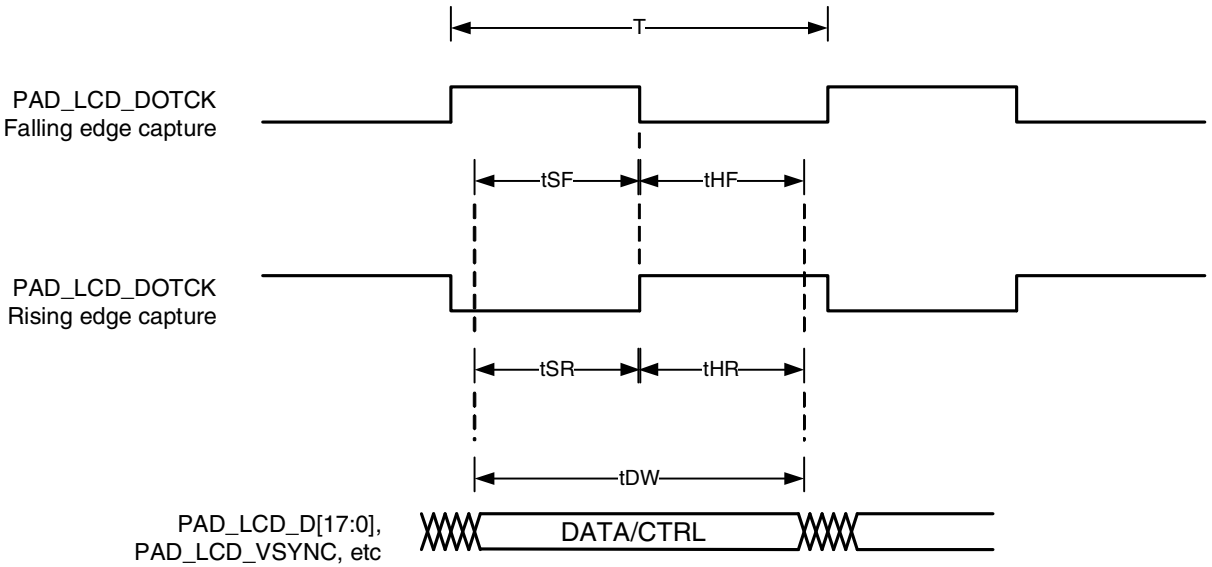


Figure 23. Read Data Latch Cycle Timing Diagram

3.5.8 LCD AC Output Electrical Specifications

Figure 24 depicts the AC output timing for the LCD module. Table 48 lists the LCD module timing parameters.



Notes:
T = LCD interface clock period
I/O Drive Strength = 4mA
I/O Voltage = 3.3V
Cck = Capacitance load on DOTCK pad
Cd = Capacitance load on DATA/CTRL pad

Figure 24. LCD AC Output Timing Diagram

Table 48. LCD AC Output Timing Parameters

ID	Parameter	Description
tSF	Data setup for falling edge	DOTCK = T/2 – 1.97ns + 0.15*Cck – 0.19*Cd
tHF	Data hold for falling edge	DOTCK = T/2 + 0.29ns + 0.09*Cd – 0.10*Cck
tSR	Data setup for rising edge	DOTCK = T/2 – 2.09ns + 0.18*Cck – 0.19*Cd
tHR	Data hold for rising edge	DOTCK = T/2 + 0.40ns + 0.09*Cd – 0.10*Cck
tDW	Data valid window	tDW = T – 1.45ns

3.5.10 JTAG Interface Timing

Figure 26 through Figure 29 show respectively the test clock input, boundary scan, test access port, and $\overline{\text{TRST}}$ timings for the SJC. Table 50 describes the SJC timing parameters (SJ1–SJ13) indicated in the figures.

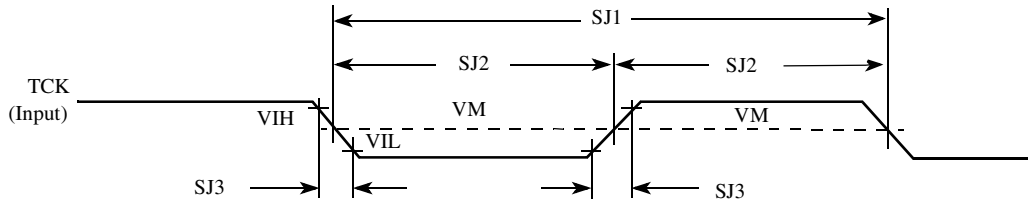


Figure 26. Test Clock Input Timing Diagram

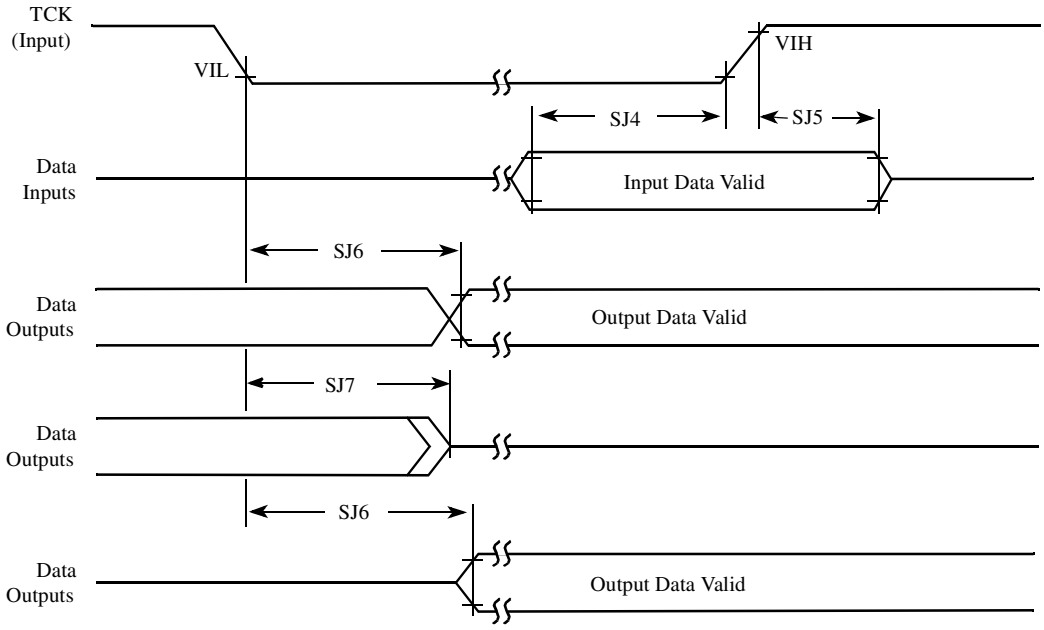


Figure 27. Boundary Scan (JTAG) Timing Diagram

Table 55. SAIF Receiver Timing with Internal Clock

ID	Parameter	Min.	Max.	Unit
SS1	BITCLK period	81.4	—	ns
SS2	BITCLK high period	36.0	—	ns
SS3	BITCLK rise time	—	6.0	ns
SS4	BITCLK low period	36.0	—	ns
SS5	BITCLK fall time	—	6.0	ns
SS14	BITCLK high to LRCLK high	—	15.0	ns
SS15	BITCLK high to LRCLK low	—	15.0	ns
SS16	SDATA setup time before BITCLK high	10.0	—	ns
SS17	SDATA hold time after BITCLK high	0.0	—	ns

3.5.13 SPDIF AC Timing

SPDIF data is sent using bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

The following Table 56 shows SPDIF timing parameters, including the timing of the modulating Tx clock (spdif_clk) in SPDIF transmitter as shown in the Figure 35.

Table 56. SPDIF Timing

Characteristics	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIFOUT output (Load = 30pf) • Skew • Transition Rising • Transition Falling	 — — —	 — — —	 1.5 13.6 18.0	ns
Modulating Tx clock (spdif_clk) period	spclkp	81.4	—	ns
spdif_clk high period	spclkph	65.1	—	ns
spdif_clk low period	spclkpl	65.1	—	ns

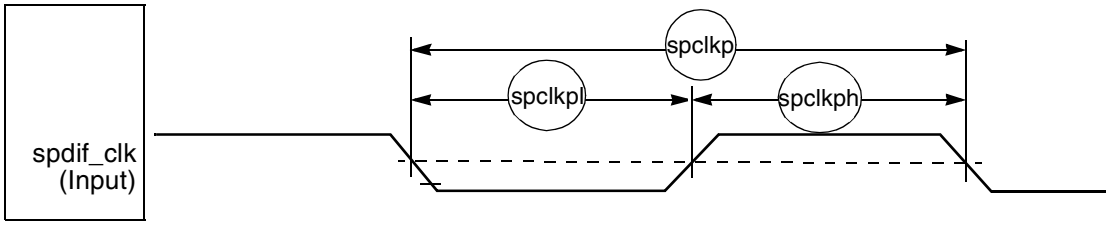


Figure 35. spdif_clk Timing

Figure 44 shows the i.MX28 production package.

Figure 44. i.MX28 Production Package

4.2 Ground, Power, Sense, and Reference Contact Assignments

Table 64 shows power and ground contact assignments for the MAPBGA package.

Table 64. MAPBGA Power and Ground Contact Assignments

Contact Name	Contact Assignment
VDDA1	C13
VDDD	G12,G11,F10,F11,K12,F12,G10
VDDIO18	G8,F9,F8,G9
VDDIO33	H8,J8,N3,G3,E6,J9,J10,A7,E16
VDDIO33_EMI	N17
VDDIO_EMI	P11,R13,N13,N15,G17,M12,M10,G13,M11,L13,G15

Table 66. 289-Pin i.MX281 MAPBGA Ball Map (continued)

K	J	H	G	F	E	D	C
ETM_TCLK	ENET0_RXD2	ENET0_RXD0	ENET0_TXD2	ENET0_TXD0	NC	NC	NC
ETM_DA0	ENET0_RXD3	ENET0_RXD1	ENET0_TXD3	ENET0_TXD1	ENET_CLK	NC	NC
ETM_DA1	ENET0_CRS	VSS	VDDIO33	ENET0_RX_CLK	ENET0_TX_CLK	SSP2_SS1	SSP2_MOSI
AUART1_TX	ENET0_COL	ENET0_MDIO	ENET0_MDC	ENET0_TX_EN	ENET0_RX_EN	SSP2_SS2	SSP2_SS0
NC	NC	AUART0_TX	AUART0_RX	NC	VSS	SSP0_DATA6	SSP0_DATA5
NC	AUART0_CTS	NC	SAIF0_LRCLK	NC	VDDIO33	SSP0_DATA2	SSP0_DATA1
PWM0	AUART0_RTS	NC	SAIF0_MCLK	SAIF0_BITCLK	SAIF0_SDATA0	SPDIF	I2C0_SCL
PWM2	VDDIO33	VDDIO33	VDDIO18	VDDIO18	SAIF1_SDATA0	I2C0_SDA	LRADC2
VSS	VDDIO33	VSS	VDDIO18	VDDIO18	PWM3	LRADC3	LRADC1
VSS	VDDIO33	VSS	VDDD	VDDD	PWM4	SSP0_DETECT	TESTMODE
VSS	VSS	VSS	VDDD	VDDD	JTAG_TCK	RTC_XTALI	RTC_XTALO
VDDD	VSS	VSS	VDDD	VDDD	JTAG_TDI	JTAG_TMS	VDDXTAL
EMI_VREF1	VDDIO_EMIQ	EMI_D12	VDDIO_EMI	EMI_D14	JTAG_TDO	LRADC4	VDDA1
EMI_DDR_OPEN	EMI_D11	VSSIO_EMI	EMI_D10	VSSIO_EMI	JTAG_RTCK	JTAG_TRST	LRADC6
VDDIO_EMIQ	VSS	EMI_D09	VDDIO_EMI	EMI_DQM1	VSS	LRADC5	LRADC0
EMI_DQS0N	EMI_DQS1N	VSS	EMI_D08	VSSIO_EMI	VDDIO33	VDD1P5	VSS
EMI_DQS0	EMI_DQS1	EMI_D13	VDDIO_EMI	EMI_D15	VDD5V	DCDC_VDDD	DCDC_VDDIO
K	J	H	G	F	E	D	C

Table 67. 289-Pin i.MX285 MAPBGA Ball Map (continued)

K	J	H	G	F	E	D	C	B
LCD_WR_RWN	ENET0_RXD2	ENET0_RXD0	ENET0_TXD2	ENET0_TXD0	NC	NC	NC	NC
LCD_D00	ENET0_RXD3	ENET0_RXD1	ENET0_TXD3	ENET0_TXD1	ENET_CLK	NC	NC	NC
LCD_D01	ENET0_CRS	VSS	VDDIO33	ENET0_RX_CLK	ENET0_TX_CLK	SSP2_SS1	SSP2_MOSI	SSP2_MISO
AUART1_TX	ENET0_COL	ENET0_MDIO	ENET0_MDC	ENET0_TX_EN	ENET0_RX_EN	SSP2_SS2	SSP2_SS0	SSP0_DATA7
NC	NC	AUART0_TX	AUART0_RX	NC	VSS	SSP0_DATA6	SSP0_DATA5	SSP0_DATA4
NC	AUART0_CTS	NC	SAIF0_LRCLK	NC	VDDIO33	SSP0_DATA2	SSP0_DATA1	SSP0_DATA0
PWM0	AUART0_RTS	NC	SAIF0_MCLK	SAIF0_BITCLK	SAIF0_SDATA0	SPDIF	I2C0_SCL	VSS
PWM2	VDDIO33	VDDIO33	VDDIO18	VDDIO18	SAIF1_SDATA0	I2C0_SDA	LRADC2	USB1DM
VSS	VDDIO33	VSS	VDDIO18	VDDIO18	PWM3	LRADC3	LRADC1	DEBUG
VSS	VDDIO33	VSS	VDDD	VDDD	PWM4	SSP0_DETECT	TESTMODE	USB0DP
VSS	VSS	VSS	VDDD	VDDD	JTAG_TCK	RTC_XTALI	RTC_XTALO	VSSA2
VDDD	VSS	VSS	VDDD	VDDD	JTAG_TDI	JTAG_TMS	VDDXTAL	XTALO
EMI_VREF1	VDDIO_EMIQ	EMI_D12	VDDIO_EMI	EMI_D14	JTAG_TDO	LRADC4	VDDA1	VSSA1
EMI_DDR_OPEN	EMI_D11	VSSIO_EMI	EMI_D10	VSSIO_EMI	JTAG_RTCK	JTAG_TRST	LRADC6	HSADC0
VDDIO_EMIQ	VSS	EMI_D09	VDDIO_EMI	EMI_DQM1	VSS	LRADC5	LRADC0	DCDC_BATT
EMI_DQS0N	EMI_DQS1N	VSS	EMI_D08	VSSIO_EMI	VDDIO33	VDD1P5	VSS	DCDC_VDDA
EMI_DQS0	EMI_DQS1	EMI_D13	VDDIO_EMI	EMI_D15	VDD5V	DCDC_VDDD	DCDC_VDDIO	DCDC_LN1
K	J	H	G	F	E	D	C	B

Table 67. 289-Pin i.MX285 MAPBGA Ball Map (continued)

	U	T	R	P	N	M	L
1	VSS	LCD_D12	LCD_D10	LCD_D07	NC	NC	NC
2	LCD_D14	LCD_D13	LCD_D11	LCD_D08	LCD_D06	LCD_D04	LCD_D02
3	LCD_D15	LCD_D16	LCD_D17	LCD_D09	VDDIO33	LCD_D05	LCD_D03
4	LCD_D18	LCD_D19	LCD_D20	LCD_RD_E	VSS	LCD_RS	AUART1_RX
5	LCD_D21	LCD_D22	LCD_D23	LCD_CS	NC	NC	NC
6	GPMI_D06	GPMI_D07	GPMI_RDN	GPMI_ALE	GPMI_RDY0	LCD_RESET	NC
7	GPMI_D03	GPMI_D04	GPMI_D05	GPMI_CLE	GPMI_CE0N	GPMI_CE2N	PWM1
8	GPMI_D00	GPMI_D01	GPMI_D02	GPMI_WRN	GPMI_RDY1	GPMI_RDY2	GPMI_RDY3
9	EMI_A08	EMI_A13	EMI_A06	EMI_CE1N	GPMI_CE1N	GPMI_CE3N	GPMI_RESETN
10	EMI_A04	EMI_A11	VSSIO_EMI	EMI_A09	EMI_A14	VDDIO_EMI	VSS
11	EMI_A12	EMI_A03	EMI_A05	VDDIO_EMI	EMI_A07	VDDIO_EMI	VSS
12	EMI_A01	EMI_BA1	VSSIO_EMI	EMI_CE0N	EMI_BA2	VDDIO_EMI	VSSIO_EMI
13	EMI_A10	EMI_CKE	VDDIO_EMI	EMI_D04	VDDIO_EMI	EMI_D01	VDDIO_EMI
14	EMI_A02	VSSIO_EMI	EMI_VREF0	VSSIO_EMI	EMI_D03	VSS	EMI_D06
15	EMI_A00	EMI_WEN	VDDIO_EMIQ	EMI_D02	VDDIO_EMI	EMI_DQM0	EMI_DDR_OPEN_FB
16	EMI_CASN	EMI_BA0	EMI_RASN	VSSIO_EMI	EMI_D00	VSSIO_EMI	EMI_CLKN
17	VSSIO_EMI	EMI_ODT1	EMI_ODT0	EMI_D05	VDDIO33_EMI	EMI_D07	EMI_CLK
	U	T	R	P	N	M	L

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Freescale Semiconductor China Ltd.
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