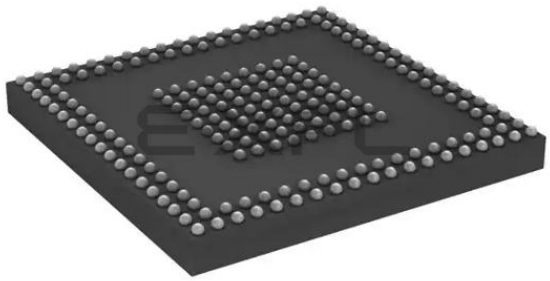

Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	XCore
Core Size	32-Bit 10-Core
Speed	1000MIPS
Connectivity	Configurable
Peripherals	-
Number of I/O	90
Program Memory Size	128KB (32K x 32)
Program Memory Type	SRAM
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	0.90V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	217-LFBGA
Supplier Device Package	217-FBGA (16x16)
Purchase URL	https://www.e-xfl.com/product-detail/xmos/xs1-a10a-128-fb217-c10

TO OUR VALUED CUSTOMERS

It is our intention to provide you with accurate and comprehensive documentation for the hardware and software components used in this product. To subscribe to receive updates, visit http://www.xmos.com/.

XMOS Ltd. is the owner or licensee of the information in this document and is providing it to you “AS IS” with no warranty of any kind, express or implied and shall have no liability in relation to its use. XMOS Ltd. makes no representation that the information, or any particular implementation thereof, is or will be free from any claims of infringement and again, shall have no liability in relation to any such claims.

3 Pin Configuration

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A	1A X0D00	1B X0D02	1C X0D04	1D X0D06	1E X0D08	1F X0D10	1G X0D12	1H X0D14	1J X0D16	1K X0D18	1L X0D20	1M X0D22	1N X0D24	1P X0D25	1R X0D26	1T X0D28	1U X0D30	1V X0D32	VDDIO_OUT
B	1W X0D01	1A X0D03	1B X0D05	1C X0D07	1D X0D09	1E X0D11	1F X0D13	1G X0D15	1H X0D17	1J X0D19	1K X0D21	1L X0D23	1M X0D70	ADC_SAMPLE	1N X0D27	1P X0D29	1R X0D31	1T X0D33	1W X0D36
C	TDO	DEBUG_N																1U X0D38	1N X0D37
D	TCK	RST_N																2C X0D40	1P X0D39
E	TMS	TDI																2D X0D42	2C X0D41
F	MODE[2]	MODE[3]				GND	GND	GND	GND	GND	GND	GND	GND	GND				2A X0D34	X0D43/WAKE
G	AVDD	ADC7				GND	GND	GND	GND	GND	GND	GND	GND	GND				1A X1D00	1A X0D35
H	ADC5	ADC6				GND	GND	GND	GND	GND	GND	GND	GND	GND				4A X1D02	1B X1D01
J	ADC3	ADC4				AVSS	GND	GND	GND	GND	GND	GND	GND	GND				4B X1D04	4A X1D03
K	ADC1	ADC2				MODE[0]	MODE[1]	GND	GND	GND	GND	GND	GND	GND				2L X1D06	1B X1D05
L	NC	ADC0				OSC_EXT_N	MODE[4]	GND	GND	GND	GND	GND	GND	GND				2A X1D08	1C X1D07
M	XI/CLK	NC				NC	NC	GND	GND	GND	GND	GND	GND	GND				1C X1D10	2A X1D09
N	XO	NC				NC	NC	GND	GND	GND	GND	GND	GND	GND				1E X1D12	1D X1D11
P	NC	VSUP				GND	GND	GND	GND	GND	GND	GND	GND	GND				4C X1D14	1F X1D13
R	SW1	SW1																1D X1D16	1G X1D15
T	SW1	VDDCORE																2B X1D18	1J X1D17
U	VDDCORE	VDDCORE																4C X1D20	4D X1D19
V	PGND	PGND	VDDIO	PGND	VDD1V8	SW2	NC	1L X1D35	8D X1D43	8D X1D41	1P X1D39	1N X1D37	4E X1D33	4F X1D31	4F X1D29	4E X1D27	1J X1D25	1G X1D22	4C X1D21
W	VSUP	VSUP	VDDIO	PGND	VDD1V8	SW2	NC	1K X1D34	8D X1D42	8D X1D40	1O X1D38	1M X1D36	4E X1D32	4F X1D30	4F X1D28	4E X1D26	1I X1D24	32A X1D70	1H X1D23

4 Signal Description

This section lists the signals and I/O pins available on the XS1-A10A-128-FB217. The device provides a combination of 1bit, 4bit, 8bit and 16bit ports, as well as wider ports that are fully or partially (gray) bonded out. All pins of a port provide either output or input, but signals in different directions cannot be mapped onto the same port.

Pins may have one or more of the following properties:

- PD/PU: The IO pin a weak pull-down or pull-up resistor. On GPIO pins this resistor can be enabled.
- ST: The IO pin has a Schmitt Trigger on its input.

Power pins (10)			
Signal	**Function**	**Type**	**Properties**
AVSS	Digital ground	GND	
GND	Digital ground	GND	
PGND	Power ground	GND	
SW1	DCDC1 switched output voltage	PWR	
SW2	DCDC2 switched output voltage	PWR	
VDD1V8	1v8 voltage supply	PWR	
VDDCORE	Core voltage supply	PWR	
VDDIO	Digital I/O power	PWR	
VDDIO_OUT	Digital I/O power out	PWR	
VSUP	Power supply (3V3/5V0)	PWR	

Analog pins (10)			
Signal	**Function**	**Type**	**Properties**
ADC0	Analog input	Input	
ADC1	Analog input	Input	
ADC2	Analog input	Input	
ADC3	Analog input	Input	
ADC4	Analog input	Input	
ADC5	Analog input	Input	
ADC6	Analog input	Input	
ADC7	Analog input	Input	
ADC_SAMPLE	Sample Analog input	I/O	
AVDD	Supply and reference voltage	PWR	

(continued)

Signal	Function					Type	Properties
X1D15	XLB^2_{out}	$4C^1$	$8B^1$	$16A^9$	$32A^{29}$	I/O	PD_S, R_U
X1D16	XLB^1_{out}	$4D^0$	$8B^2$	$16A^{10}$		I/O	PD_S, R_U
X1D17	XLB^0_{out}	$4D^1$	$8B^3$	$16A^{11}$		I/O	PD_S, R_U
X1D18	XLB^0_{in}	$4D^2$	$8B^4$	$16A^{12}$		I/O	PD_S, R_U
X1D19	XLB^1_{in}	$4D^3$	$8B^5$	$16A^{13}$		I/O	PD_S, R_U
X1D20	XLB^2_{in}	$4C^2$	$8B^6$	$16A^{14}$	$32A^{30}$	I/O	PD_S, R_U
X1D21	XLB^3_{in}	$4C^3$	$8B^7$	$16A^{15}$	$32A^{31}$	I/O	PD_S, R_U
X1D22	XLB^4_{in}	$1G^0$				I/O	PD_S, R_U
X1D23		$1H^0$				I/O	PD_S, R_U
X1D24		$1I^0$				I/O	PD_S
X1D25		$1J^0$				I/O	PD_S
X1D26		$4E^0$	$8C^0$	$16B^0$		I/O	PD_S, R_U
X1D27		$4E^1$	$8C^1$	$16B^1$		I/O	PD_S, R_U
X1D28		$4F^0$	$8C^2$	$16B^2$		I/O	PD_S, R_U
X1D29		$4F^1$	$8C^3$	$16B^3$		I/O	PD_S, R_U
X1D30		$4F^2$	$8C^4$	$16B^4$		I/O	PD_S, R_U
X1D31		$4F^3$	$8C^5$	$16B^5$		I/O	PD_S, R_U
X1D32		$4E^2$	$8C^6$	$16B^6$		I/O	PD_S, R_U
X1D33		$4E^3$	$8C^7$	$16B^7$		I/O	PD_S, R_U
X1D34		$1K^0$				I/O	PD_S
X1D35		$1L^0$				I/O	PD_S
X1D36		$1M^0$	$8D^0$	$16B^8$		I/O	PD_S
X1D37		$1N^0$	$8D^1$	$16B^9$		I/O	PD_S, R_U
X1D38		$1O^0$	$8D^2$	$16B^{10}$		I/O	PD_S, R_U
X1D39		$1P^0$	$8D^3$	$16B^{11}$		I/O	PD_S, R_U
X1D40			$8D^4$	$16B^{12}$		I/O	PD_S, R_U
X1D41			$8D^5$	$16B^{13}$		I/O	PD_S, R_U
X1D42			$8D^6$	$16B^{14}$		I/O	PD_S, R_U
X1D43			$8D^7$	$16B^{15}$		I/O	PU_S, R_U
X1D70					$32A^{19}$	I/O	PD_S

Feature	Bit	Description
Disable JTAG	0	The JTAG interface is disabled, making it impossible for the tile state or memory content to be accessed via the JTAG interface.
Disable Link access	1	Other tiles are forbidden access to the processor state via the system switch. Disabling both JTAG and Link access transforms an xCORE Tile into a “secure island” with other tiles free for non-secure user application code.
Secure Boot	5	The processor is forced to boot from address 0 of the OTP, allowing the processor boot ROM to be bypassed (*see* §9).
Redundant rows	7	Enables redundant rows in OTP.
Sector Lock 0	8	Disable programming of OTP sector 0.
Sector Lock 1	9	Disable programming of OTP sector 1.
Sector Lock 2	10	Disable programming of OTP sector 2.
Sector Lock 3	11	Disable programming of OTP sector 3.
OTP Master Lock	12	Disable OTP programming completely: disables updates to all sectors and security register.
Disable JTAG-OTP	13	Disable all (read & write) access from the JTAG interface to this OTP.
Disable Global Debug	14	Disables access to the DEBUG_N pin.
	21..15	General purpose software accessable security register available to end-users.
	31..22	General purpose user programmable JTAG UserID code extension.

Figure 12: Security register features

32-bit. Byte (8-bit), half-word (16-bit) or word (32-bit) accesses are supported and are executed within one tile clock cycle. There is no dedicated external memory interface, although data memory can be expanded through appropriate use of the ports.

10.3 Deep Sleep Memory

The XS1-A10A-128-FB217 device includes 128 bytes of deep sleep memory for state storage during sleep mode. Deep sleep memory is volatile and if device input power is remove, the data will be lost.

11 Analog-to-Digital Converter

The device has a 12-bit 1MSample/second Successive Approximation Register (SAR) Analogue to Digital Converter (ADC). It has 8 input pins which are multiplexed into the ADC. The sampling of the ADC is controlled using the ADC_SAMPLE pin that should be wired to a GPIO pin, for example X0D24 (port 1I). The sampling is triggered either by writing to the port, or by driving the pin externally. On each

13.3 Deep Sleep Modes and Real-Time Counter

The normal mode in which the XS1-A10A-128-FB217 operates is the AWAKE mode. In this mode, all cores, memory, and peripherals operate as normal. To save power, the XS1-A10A-128-FB217 can be put into a deep sleep mode, called ASLEEP, where the digital node is powered down, and most peripherals are powered down. The XS1-A10A-128-FB217 will stay in the ASLEEP mode until one of two conditions:

1. An external pin is asserted or deasserted (set by the program);

2. The 64-bit real-time counter reaches a value set by the program; or

When the chip is awake, the real-time counter counts the number of clock ticks on the oscillator. As such, the real-time counter will run at a fixed ratio, but synchronously with the 100 MHz timers on the xCORE Tile. When asleep, the real-time counter can be automatically switched to the 31,250 Hz silicon oscillator to save power (see Appendix H). To ensure that the real-time counter increases linearly over time, a programmable value is added to the counter on every 31,250 Hz clock-tick. This means that the clock will run at a granularity of 31,250 Hz but still maintain real-time in terms of the frequency of the main oscillator. If an accurate clock is required, even whilst asleep, then an external crystal or oscillator shall be provided that is used in both AWAKE and ASLEEP state.

The designer has to make a trade-off between accuracy of clocks when asleep and awake, costs, and deep-sleep power consumption. Four example designs are shown in Figure 15.

Figure 15: Example trade-offs in oscillator selection

Clocks used		Power	BOM	Accuracy	
Awake	Asleep	Asleep	costs	Awake	Asleep
20 Mhz SiOsc	31,250 SiOsc	lowest	lowest	lowest	lowest
24 MHz Crystal	31,250 SiOsc	lowest	medium	highest	lowest
5 MHz ext osc	5 MHz ext osc	medium	highest	highest	highest
24 MHz Crystal	24 MHz crystal	highest	medium	highest	highest

During deep-sleep, the program can store some state in 128 bytes of Deep Sleep Memory.

13.4 Requirements during sleep mode

Whilst in sleep mode, the device must still be powered as normal over 3V3 or 5V0 on VSUP, and 3V3 on VDDIO; however it will draw less power on both VSUP and VDDIO.

For best results (lowest power):

- The XTAL bias and XTAL oscillators should be switched off.
- The sleep register should be configured to

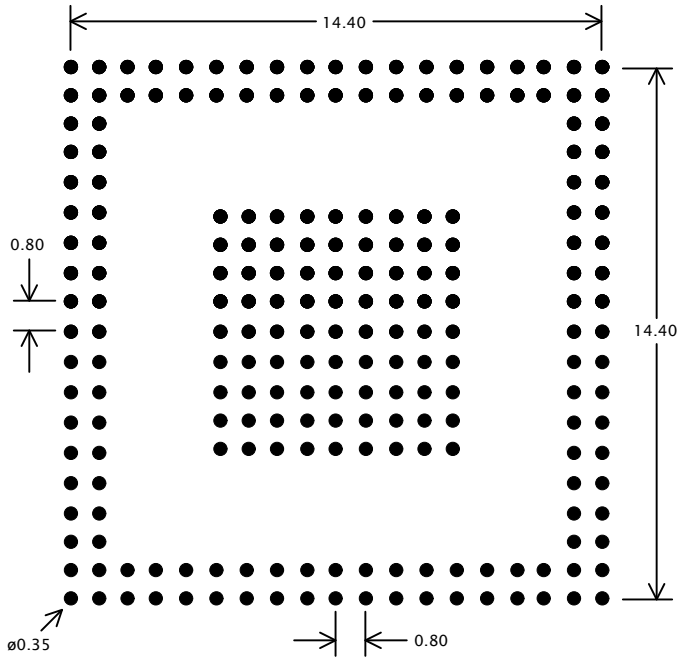

Figure 20: Example land pattern

15.2 Ground and Thermal Vias

Vias next to every other ground ball into the ground plane of the PCB are recommended for a low inductance ground connection and good thermal performance. Vias with with a 0.6mm diameter annular ring and a 0.3mm drill would be suitable.

15.3 Moisture Sensitivity

XMOS devices are, like all semiconductor devices, susceptible to moisture absorption. When removed from the sealed packaging, the devices slowly absorb moisture from the surrounding environment. If the level of moisture present in the device is too high during reflow, damage can occur due to the increased internal vapour pressure of moisture. Example damage can include bond wire damage, die lifting, internal or external package cracks and/or delamination.

All XMOS devices are Moisture Sensitivity Level (MSL) 3 - devices have a shelf life of 168 hours between removal from the packaging and reflow, provided they are stored below 30C and 60% RH. If devices have exceeded these values or an included moisture indicator card shows excessive levels of moisture, then the parts should be baked as appropriate before use. This is based on information from *Joint IPC/JEDEC Standard For Moisture/Reflow Sensitivity Classification For Nonhermetic Solid State Surface-Mount Devices* J-STD-020 Revision D.

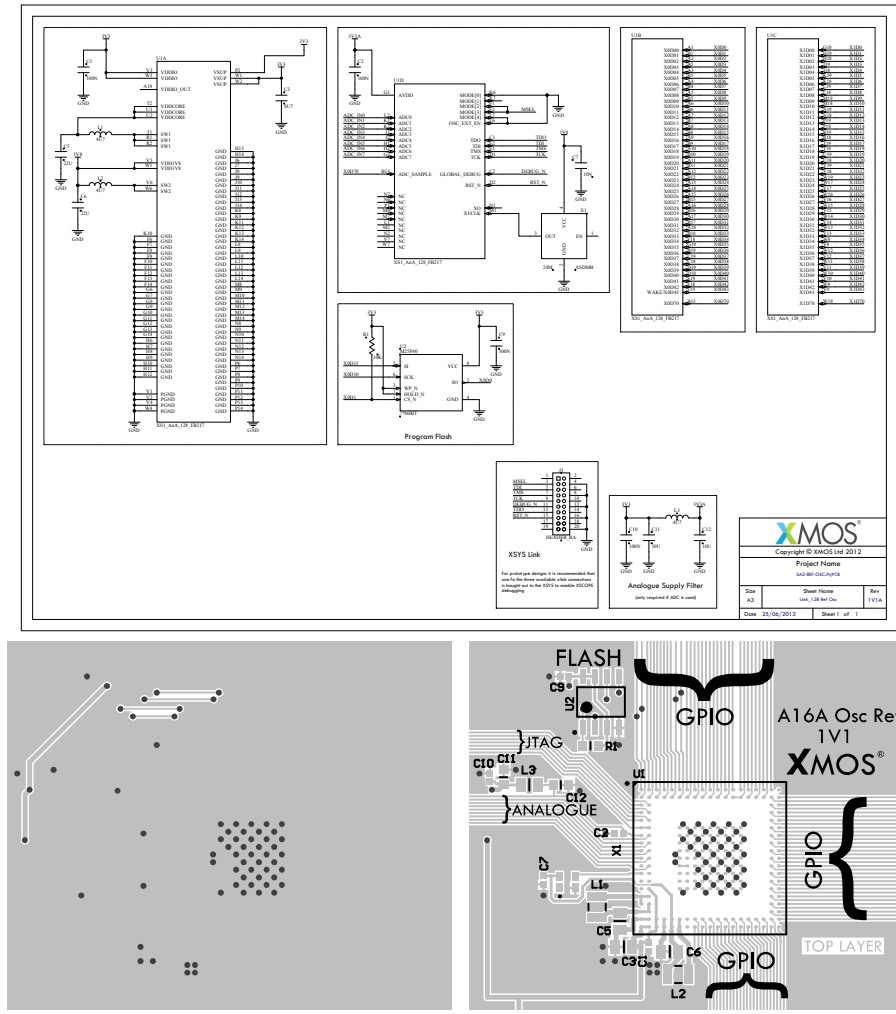

Figure 22: Example Oscillator schematic, with top and bottom layout of a 2-layer PCB

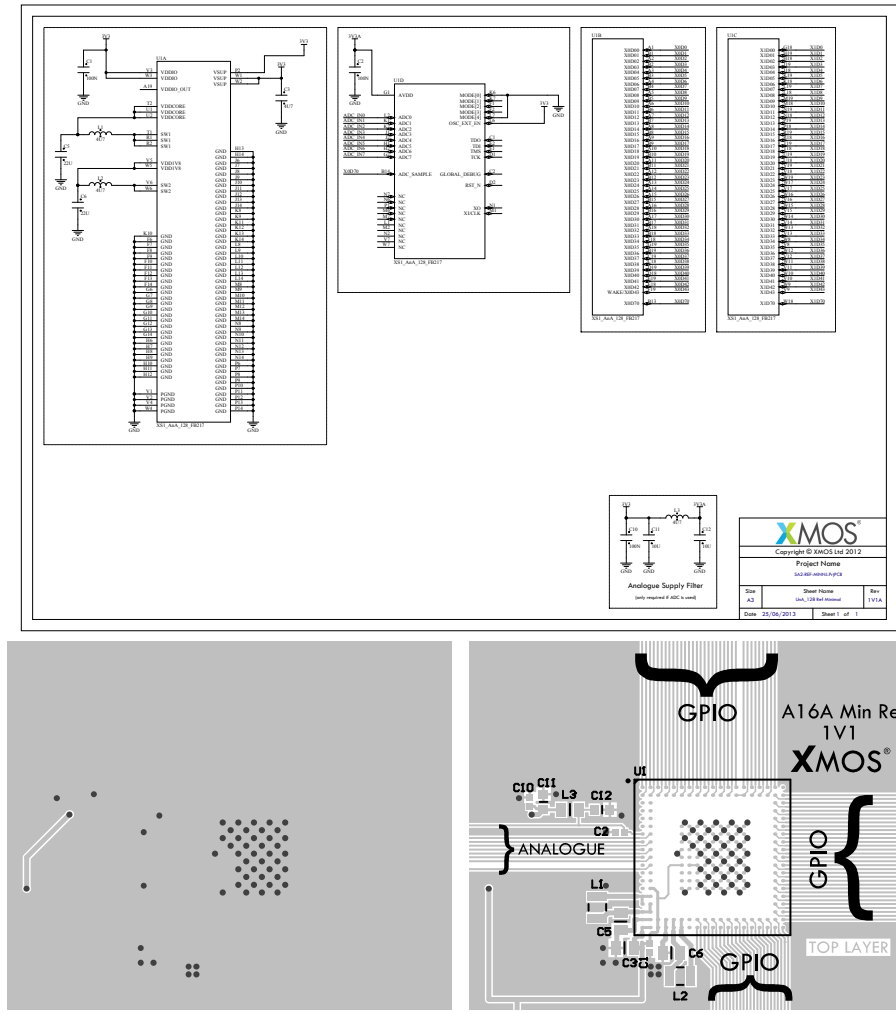

Figure 23: Example minimal system schematic, with top and bottom layout of a 2-layer PCB

0x03: xCORE Tile boot status

Bits	Perm	Init	Description
31:24	RO	-	Reserved
23:16	RO		xCORE tile number on the switch.
15:9	RO	-	Reserved
8	RO		Set to 1 if boot from OTP is enabled.
7:0	RO		The boot mode pins MODE0, MODE1, ..., specifying the boot frequency, boot source, etc.

B.5 Security configuration: 0x05

Copy of the security register as read from OTP.

0x05: Security configuration

Bits	Perm	Init	Description
31:0	RO		Value.

B.6 Ring Oscillator Control: 0x06

There are four free-running oscillators that clock four counters. The oscillators can be started and stopped using this register. The counters should only be read when the ring oscillator is stopped. The counter values can be read using four subsequent registers. The ring oscillators are asynchronous to the xCORE tile clock and can be used as a source of random bits.

0x06: Ring Oscillator Control

Bits	Perm	Init	Description
31:2	RO	-	Reserved
1	RW	0	Set to 1 to enable the xCORE tile ring oscillators
0	RW	0	Set to 1 to enable the peripheral ring oscillators

B.7 Ring Oscillator Value: 0x07

This register contains the current count of the xCORE Tile Cell ring oscillator. This value is not reset on a system reset.

0x07: Ring Oscillator Value

Bits	Perm	Init	Description
31:16	RO	-	Reserved
15:0	RO	-	Ring oscillator counter data.

0x11: Debug SPC

Bits	Perm	Init	Description
31:0	DRW		Value.

B.13 Debug SSP: 0x12

This register contains the value of the SSP register when the debugger was called.

0x12: Debug SSP

Bits	Perm	Init	Description
31:0	DRW		Value.

B.14 DGETREG operand 1: 0x13

The resource ID of the logical core whose state is to be read.

0x13: DGETREG operand 1

Bits	Perm	Init	Description
31:8	RO	-	Reserved
7:0	DRW		Thread number to be read

B.15 DGETREG operand 2: 0x14

Register number to be read by DGETREG

0x14: DGETREG operand 2

Bits	Perm	Init	Description
31:5	RO	-	Reserved
4:0	DRW		Register number to be read

B.16 Debug interrupt type: 0x15

Register that specifies what activated the debug interrupt.

0x80 .. 0x83: Resources breakpoint mask

Bits	Perm	Init	Description
31:0	DRW		Value.

B.26 Resources breakpoint value: 0x90 .. 0x93

This set of registers contains the value for the four resource watchpoints.

0x90 .. 0x93: Resources breakpoint value

Bits	Perm	Init	Description
31:0	DRW		Value.

B.27 Resources breakpoint control register: 0x9C .. 0x9F

This set of registers controls each of the four resource watchpoints.

0x9C .. 0x9F: Resources breakpoint control register

Bits	Perm	Init	Description
31:24	RO	-	Reserved
23:16	DRW	0	A bit for each logical core in the tile allowing the breakpoint to be enabled individually for each logical core.
15:2	RO	-	Reserved
1	DRW	0	By default, resource watchpoints trigger when the resource id masked with the set Mask equals the Value. If set to 1, resource watchpoints trigger when the resource id masked with the set Mask is not equal to the Value.
0	DRW	0	When 1 the instruction breakpoint is enabled.

0x05: Cause debug interrupts

Bits	Perm	Init	Description
31:2	RO	-	Reserved
1	RO	0	Set to 1 when the processor is in debug mode.
0	CRW	0	Set to 1 to request a debug interrupt on the processor.

C.6 xCORE Tile clock divider: 0x06

This register contains the value used to divide the PLL clock to create the xCORE tile clock. The divider is enabled under control of the tile control register

0x06: xCORE Tile clock divider

Bits	Perm	Init	Description
31:8	RO	-	Reserved
7:0	RW		Value of the clock divider minus one.

C.7 Security configuration: 0x07

Copy of the security register as read from OTP.

0x07: Security configuration

Bits	Perm	Init	Description
31:0	RO		Value.

C.8 PLink status: 0x10 .. 0x13

Status of each of the four processor links; connecting the xCORE tile to the switch.

C.11 PC of logical core 1: 0x41

0x41: PC of logical core 1

Bits	Perm	Init	Description
31:0	RO		Value.

C.12 PC of logical core 2: 0x42

0x42: PC of logical core 2

Bits	Perm	Init	Description
31:0	RO		Value.

C.13 PC of logical core 3: 0x43

0x43: PC of logical core 3

Bits	Perm	Init	Description
31:0	RO		Value.

C.14 PC of logical core 4: 0x44

0x44: PC of logical core 4

Bits	Perm	Init	Description
31:0	RO		Value.

C.15 SR of logical core 0: 0x60

Value of the SR of logical core 0

0x60: SR of logical core 0

Bits	Perm	Init	Description
31:0	RO		Value.

D.11 Debug source: 0x1F

Contains the source of the most recent debug event.

0x1F: Debug source

Bits	Perm	Init	Description
31:5	RO	-	Reserved
4	RW		If set, the external DEBUG_N pin is the source of the most recent debug interrupt.
3:1	RO	-	Reserved
0	RW		If set, the xCORE Tile is the source of the most recent debug interrupt.

D.12 Link status, direction, and network: 0x20 .. 0x27

These registers contain status information for low level debugging (read-only), the network number that each link belongs to, and the direction that each link is part of. The registers control links C, D, A, B, G, H, E, and F in that order.

0x20 .. 0x27: Link status, direction, and network

Bits	Perm	Init	Description
31:26	RO	-	Reserved
25:24	RO		If this link is currently routing data into the switch, this field specifies the type of link that the data is routed to: 0: plink 1: external link 2: internal control link
23:16	RO	0	If the link is routing data into the switch, this field specifies the destination link number to which all tokens are sent.
15:12	RO	-	Reserved
11:8	RW	0	The direction that this this link is associated with; set for routing.
7:6	RO	-	Reserved
5:4	RW	0	Determines the network to which this link belongs, set for quality of service.
3	RO	-	Reserved
2	RO	0	Set to 1 if the current packet is junk and being thrown away. A packet is considered junk if, for example, it is not routable.
1	RO	0	Set to 1 if the switch is routing data into the link, and if a route exists from another link.
0	RO	0	Set to 1 if the link is routing data into the switch, and if a route is created to another link on the switch.

Figure 46: Summary

Number	Perm	Description
0x00 .. 0x7F	RW	Deep sleep memory
0xFF	RW	Deep sleep memory valid

G.1 Deep sleep memory: 0x00 .. 0x7F

128 bytes of memory that can be used to hold data when the xCORE Tile is powered down.

0x00 .. 0x7F: Deep sleep memory

Bits	Perm	Init	Description
7:0	RW		User defined data

G.2 Deep sleep memory valid: 0xFF

One byte of memory that is reset to 0. The program can write a non zero value in this register to indicate that the data in deep sleep memory is valid.

0xFF: Deep sleep memory valid

Bits	Perm	Init	Description
7:0	RW	0	User defined data, reset to 0.

H Oscillator Configuration

The *Oscillator* is peripheral 4. The control registers are accessed using 8-bit reads and writes (use `write_periph_8(device, 4, ...)` and `read_periph_8(device, 4, ...)` for reads and writes).

Figure 47: Summary

Number	Perm	Description
0x00	RW	General oscillator control
0x01	RW	On-silicon-oscillator control
0x02	RW	Crystal-oscillator control

0x00: General control

Bits	Perm	Init	Description
31:8	RO	-	Reserved
7	RW	0	By default, when waking up, the voltage levels stored in the LEVEL CONTROL registers are used. Set to 1 to use the power-on voltage levels.
6	WO		Set to 1 to re-apply the current contents of the AWAKE state. Use this when the program has changed the contents of the AWAKE state register. Self clearing.
5	RW	0	Set to 1 to use a 64-bit timer.
4	RW	0	Set to 1 to wake-up on the timer.
3	RW	1	If waking on the WAKE pin is enabled (see above), then by default the device wakes up when the WAKE pin is pulled high. Set to 0 to wake-up when the WAKE pin is pulled low.
2	RW	0	Set to 1 to wake-up when the WAKE pin is at the right level.
1	RW	0	Set to 1 to initiate sleep sequence - self clearing. Only set this bit when in AWAKE state.
0	RW	0	Sleep clock select. Set to 1 to use the default clock rather than the internal 31.25 kHz oscillator. Note: this bit is only effective in the ASLEEP state.

J.2 Time to wake-up, least significant 32 bits: 0x04

This register stores the time to wake-up. The value is only used if wake-up from the real-time clock is enabled, and the device is asleep.

0x04: Time to wake-up, least significant 32 bits

Bits	Perm	Init	Description
31:0	RW	0	Least significant 32 bits of time to wake-up.

J.3 Time to wake-up, most significant 32 bits: 0x08

This register stores the time to wake-up. The value is only used if wake-up from the real-time clock is enabled, if 64-bit comparisons are enabled, and the device is asleep. In most cases, 32-bit comparisons suffice.

0x08: Time to wake-up, most significant 32 bits

Bits	Perm	Init	Description
31:0	RW	0	Most significant 32 bits of time to wake-up (ignored unless 64-bit timer comparison is enabled).

J.4 Power supply states whilst ASLEEP: 0x0C

This register controls the state the power control block should be in when in the ASLEEP state. It also defines the minimum time that the system shall stay in this state. When the minimum time is expired, the next state may be entered if either of the wake conditions (real-time counter or WAKE pin) happens. Note that the minimum number of cycles is counted in according to the currently enabled clock, which may be the slow 31 KHz clock.

0x0C: Power supply states whilst ASLEEP

Bits	Perm	Init	Description
31:21	RO	-	Reserved
20:16	RW	16	Log2 number of cycles to stay in this state: 0: 1 clock cycles 1: 2 clock cycles 2: 4 clock cycles ... 31: 2147483648 clock cycles
15	RO	-	Reserved
14	RW	0	Set to 1 to disable clock to the xCORE Tile.
13:10	RO	-	Reserved
9	RW	0	Sets modulation used by DCDC2: 0: PWM modulation (max 475 mA) 1: PFM modulation (max 50 mA)
8	RW	0	Sets modulation used by DCDC1: 0: PWM modulation (max 700 mA) 1: PFM modulation (max 50 mA)
7:6	RO	-	Reserved
5	RW	0	Set to 1 to enable VOUT6 (IO supply).
4	RW	0	Set to 1 to enable LDO5 (core PLL supply).
3:2	RO	-	Reserved
1	RO	0	Set to 1 to enable DCDC2 (analogue supply).
0	RW	0	Set to 1 to enable DCDC1 (core supply).

Bits	Perm	Init	Description
31:21	RO	-	Reserved
20:16	RW	16	Log2 number of cycles to stay in this state: 0: 1 clock cycles 1: 2 clock cycles 2: 4 clock cycles ... 31: 2147483648 clock cycles
15	RO	-	Reserved
14	RW	0	Set to 1 to disable clock to the xCORE Tile.
13:10	RO	-	Reserved
9	RW	0	Sets modulation used by DCDC2: 0: PWM modulation (max 475 mA) 1: PFM modulation (max 50 mA)
8	RW	0	Sets modulation used by DCDC1: 0: PWM modulation (max 700 mA) 1: PFM modulation (max 50 mA)
7:6	RO	-	Reserved
5	RW	1	Set to 1 to enable VOUT6 (IO supply).
4	RW	0	Set to 1 to enable LDO5 (core PLL supply).
3:2	RO	-	Reserved
1	RO	1	Set to 1 to enable DCDC2 (analogue supply).
0	RW	0	Set to 1 to enable DCDC1 (core supply).

0x1C: Power supply states whilst SLEEPING1

J.9 Power supply states whilst SLEEPING2: 0x20

This register controls what state the power control block should be in when in the SLEEPING2 state. It also defines the time that the system shall stay in this state.

0x40: LDO5 level control

Bits	Perm	Init	Description
31:3	RO	-	Reserved
2:0	RW	pin	The required voltage in 100 mV steps: 0: 0.6V 1: 0.7V 2: 0.8V ... 6: 1.2V 7: 1.3V