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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8/300H
Core Size	16-Bit
Speed	25MHz
Connectivity	SCI, SmartCard
Peripherals	PWM, WDT
Number of I/O	35
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BFQFP
Supplier Device Package	100-QFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/d13008vfbl25v

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5.3 Interrupt Sources

The interrupt sources include external interrupts (NMI, IRQ_5 to IRQ_0) and 27 internal interrupts.

5.3.1 External Interrupts

There are seven external interrupts: NMI, and IRQ_5 to IRQ_0. Of these, NMI, IRQ_2, IRQ_1, and IRQ_0 can be used to exit software standby mode.

NMI: NMI is the highest-priority interrupt and is always accepted, regardless of the states of the I and UI bits in CCR. The NMIEG bit in SYSCR selects whether an interrupt is requested by the rising or falling edge of the input at the NMI pin. NMI interrupt exception handling has vector number 7.

IRQ_5 to IRQ_0 Interrupts: These interrupts are requested by input signals at pins $\overline{IRQ_5}$ to $\overline{IRQ_0}$. The IRQ_5 to IRQ_0 interrupts have the following features.

- ISCR settings can select whether an interrupt is requested by the low level of the input at pins $\overline{IRQ_5}$ to $\overline{IRQ_0}$, or by the falling edge.
- IER settings can enable or disable the IRQ_5 to IRQ_0 interrupts. Interrupt priority levels can be assigned by four bits in IPRA (IPRA7 to IPRA4).
- The status of IRQ_5 to IRQ_0 interrupt requests is indicated in ISR. The ISR flags can be cleared to 0 by software.

Figure 5.2 shows a block diagram of interrupts IRQ_5 to IRQ_0.

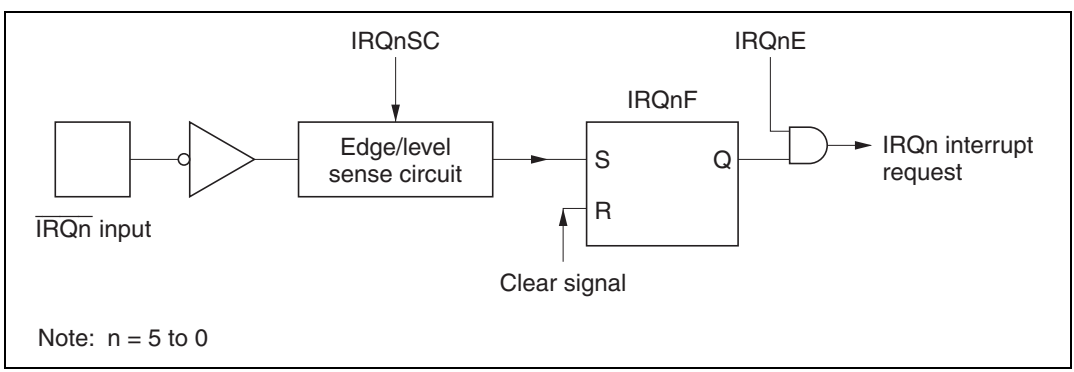


Figure 5.2 Block Diagram of Interrupts IRQ_5 to IRQ_0

In byte access, whether the upper or lower data bus is used is determined by whether the address is even or odd. The upper data bus is used for an even address, and the lower data bus for an odd address.

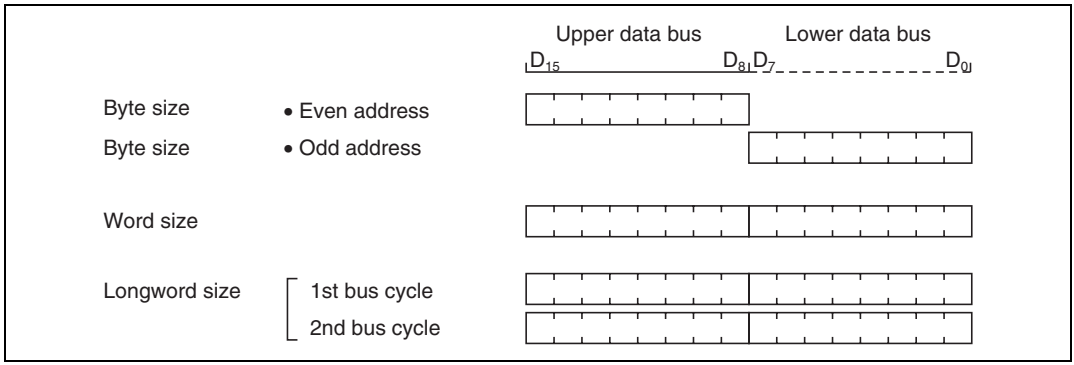


Figure 6.8 Access Sizes and Data Alignment Control (16-Bit Access Area)

6.4.3 Valid Strobes

Table 6.4 shows the data buses used, and the valid strobes, for the access spaces.

In a read, the $\overline{RD}$ signal is valid for both the upper and the lower half of the data bus.

In a write, the $\overline{HWR}$ signal is valid for the upper half of the data bus, and the $\overline{LWR}$ signal for the lower half.

Table 7.5 Port 6 Pin Functions in Modes 1 to 4

Pin	Pin Functions and Selection Method
$P6_7/\phi$	Bit PSTOP in MSTCRH selects the pin function.

PSTOP	0	1
Pin function	ϕ output	$P6_7$ input

$\overline{LWR}$	Functions as $\overline{LWR}$ regardless of the setting of bit $P6_6DDR$	
$P6_6DDR$	0	1
Pin function	$\overline{LWR}$ output	

$\overline{HWR}$	Functions as $\overline{HWR}$ regardless of the setting of bit $P6_5DDR$	
$P6_5DDR$	0	1
Pin function	$\overline{HWR}$ output	

$\overline{RD}$	Functions as $\overline{RD}$ regardless of the setting of bit $P6_4DDR$	
$P6_4DDR$	0	1
Pin function	$\overline{RD}$ output	

$\overline{AS}$	Functions as $\overline{AS}$ regardless of the setting of bit $P6_3DDR$	
$P6_3DDR$	0	1
Pin function	$\overline{AS}$ output	

$P6_2/\overline{BACK}$ Bit BRLE in BRCR and bit $P6_2DDR$ select the pin function as follows.

BRLE	0		1
$P6_2DDR$	0	1	—
Pin function	$P6_2$ input	$P6_2$ output	$\overline{BACK}$ output

$P6_1/\overline{BREQ}$ Bit BRLE in BRCR and bit $P6_1DDR$ select the pin function as follows.

BRLE	0		1
$P6_1DDR$	0	1	—
Pin function	$P6_1$ input	$P6_1$ output	$\overline{BREQ}$ input

$P6_0/\overline{WAIT}$ Bit WAITE in BCR and bit $P6_0DDR$ select the pin function as follows.

WAITE	0		1
$P6_0DDR$	0	1	0*
Pin function	$P6_0$ input	$P6_0$ output	$\overline{WAIT}$ input

Note: * Do not set bit $P6_0DDR$ to 1.

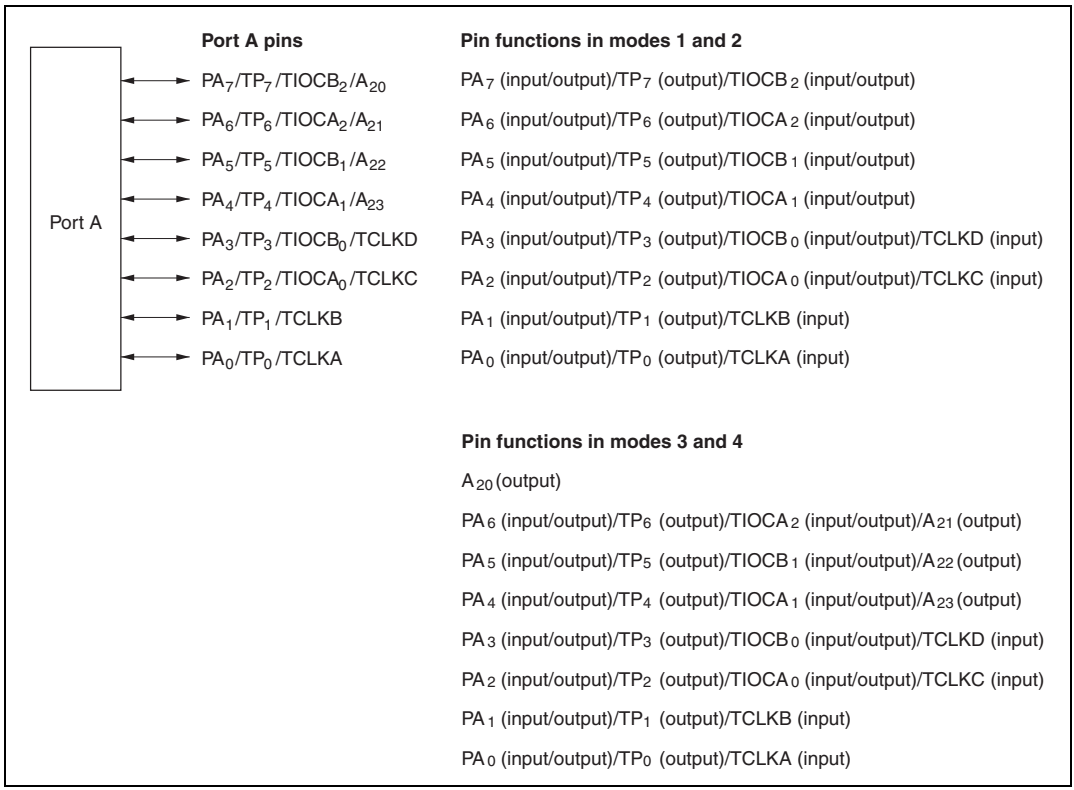


Figure 7.6 Port A Pin Configuration

7.7.2 Register Descriptions

Table 7.11 summarizes the registers of port A.

Table 7.11 Port A Registers

				Initial Value	
Address*	**Name**		**R/W**	**Modes 1 and 2**	**Modes 3 and 4**
H'EE009	Port A data direction register	PADDR	W	H'00	H'80
H'FFFD9	Port A data register	PADR	R/W	H'00	H'00

Note: * Lower 20 bits of the address in advanced mode.

Example of Phase Counting Mode: Figure 8.30 shows an example of operations in phase counting mode. Table 8.5 lists the up-counting and down-counting conditions for 16TCNT2.

In phase counting mode both the rising and falling edges of TCLKA and TCLKB are counted. The phase difference between TCLKA and TCLKB must be at least 1.5 states, the phase overlap must also be at least 1.5 states, and the pulse width must be at least 2.5 states.

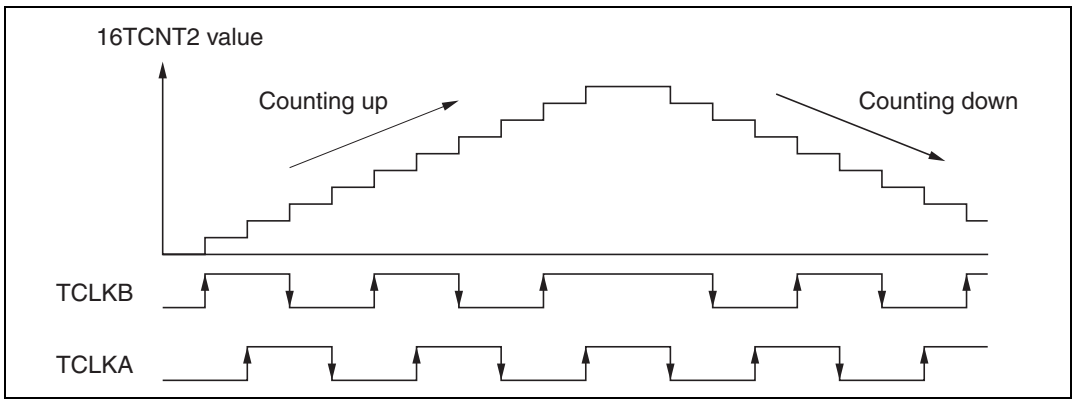


Figure 8.30 Operation in Phase Counting Mode (Example)

Table 8.5 Up/Down Counting Conditions

Counting Direction	Up-Counting				Down-Counting			
TCLKB pin	↑	High	↓	Low	High	↓	Low	↑
TCLKA pin	Low	↑	High	↓	↓	Low	↑	High

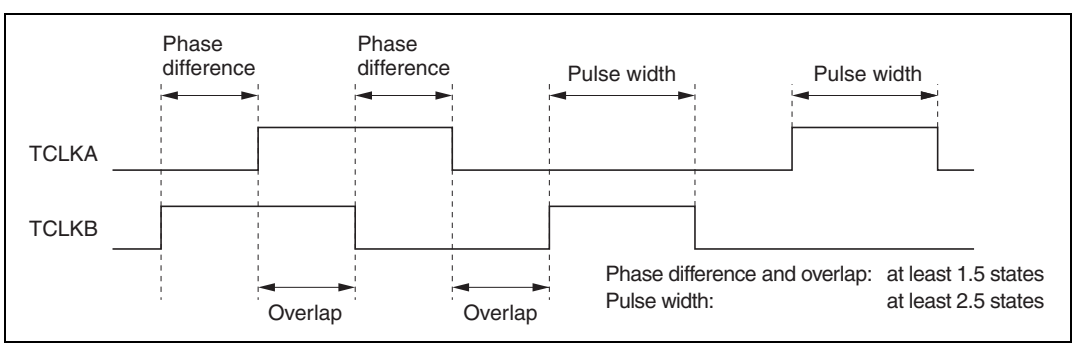


Figure 8.31 Phase Difference, Overlap, and Pulse Width in Phase Counting Mode

Bit 7—Compare Match/Input Capture Flag B (CMFB): Status flag that indicates the occurrence of a TCORB compare match or input capture.

Bit 7 CMFB	Description	
0	[Clearing condition] Read CMFB when CMFB = 1, then write 0 in CMFB	(Initial value)
1	[Setting conditions] • 8TCNT = TCORB* • The 8TCNT value is transferred to TCORB by an input capture signal when TCORB functions as an input capture register	

Note: * When bit ICE is set to 1 in 8TCSR1 and 8TCSR3, the CMFB flag is not set when 8TCNT0 = TCORB0 or 8TCNT2 = TCORB2.

Bit 6—Compare Match Flag A (CMFA): Status flag that indicates the occurrence of a TCORA compare match.

Bit 6 CMFA	Description	
0	[Clearing condition] Read CMFA when CMFA = 1, then write 0 in CMFA	(Initial value)
1	[Setting condition] 8TCNT = TCORA	

Bit 5—Timer Overflow Flag (OVF): Status flag that indicates that the 8TCNT has overflowed from H'FF to H'00.

Bit 5 OVF	Description	
0	[Clearing condition] Read OVF when OVF = 1, then write 0 in OVF	(Initial value)
1	[Setting condition] 8TCNT overflows from H'FF to H'00	

12.5 Usage Notes

12.5.1 Notes on Use of SCI

Note the following points when using the SCI.

TDR Write and TDRE Flag: The TDRE flag in SSR is a status flag indicating the loading of transmit data from TDR to TSR. The SCI sets the TDRE flag to 1 when it transfers data from TDR to TSR.

Data can be written into TDR regardless of the state of the TDRE flag. If new data is written in TDR when the TDRE flag is 0, the old data stored in TDR will be lost because this data has not yet been transferred to TSR. Before writing transmit data in TDR, be sure to check that the TDRE flag is set to 1.

Simultaneous Multiple Receive Errors: Table 12.13 shows the state of the SSR status flags when multiple receive errors occur simultaneously. When an overrun error occurs the RSR contents are not transferred to RDR, so receive data is lost.

Table 12.13 SSR Status Flags and Transfer of Receive Data

SSR Status Flags				Receive Data Transfer	
RDRF	**ORER**	**FER**	**PER**	**RSR → RDR**	**Receive Errors**
1	1	0	0	×	Overrun error
0	0	1	0	○	Framing error
0	0	0	1	○	Parity error
1	1	1	0	×	Overrun error + framing error
1	1	0	1	×	Overrun error + parity error
0	0	1	1	○	Framing error + parity error
1	1	1	1	×	Overrun error + framing error + parity error

Legend:

○: Receive data is transferred from RSR to RDR.

×: Receive data is not transferred from RSR to RDR.

If reception ends and the RDRF flag is set to 1 while the RIE bit is set to 1 and interrupt requests are enabled, a receive-data-full interrupt (RXI) will be requested. If an error occurs in reception and either the ORER flag or the PER flag is set to 1, a transmit/receive-error interrupt (ERI) will be requested.

For details, see Interrupt Operations in this section.

If a parity error occurs during reception and the PER flag is set to 1, the received data is transferred to RDR, so the erroneous data can be read.

Switching Modes: When switching from receive mode to transmit mode, first confirm that the receive operation has been completed, then start from initialization, clearing RE to 0 and setting TE to 1. The RDRF, PER, or ORER flag can be used to check that the receive operation has been completed.

When switching from transmit mode to receive mode, first confirm that the transmit operation has been completed, then start from initialization, clearing TE to 0 and setting RE to 1. The TEND flag can be used to check that the transmit operation has been completed.

Fixing Clock Output: When the GM bit is set to 1 in SMR, clock output can be fixed by means of the CKE1 and CKE0 bits in SCR. The minimum clock pulse width can be set to the specified width in this case.

Figure 13.9 shows the timing for fixing clock output. In this example, GM = 1, CKE1 = 0, and the CKE0 bit is controlled.

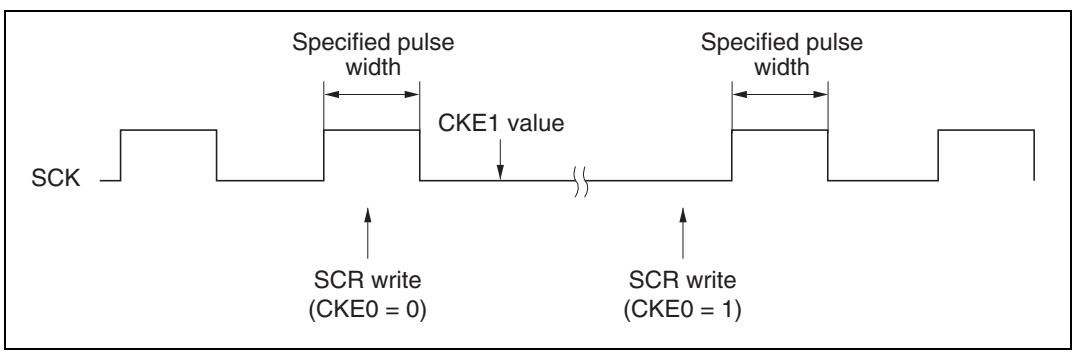


Figure 13.9 Timing for Fixing Cock Output

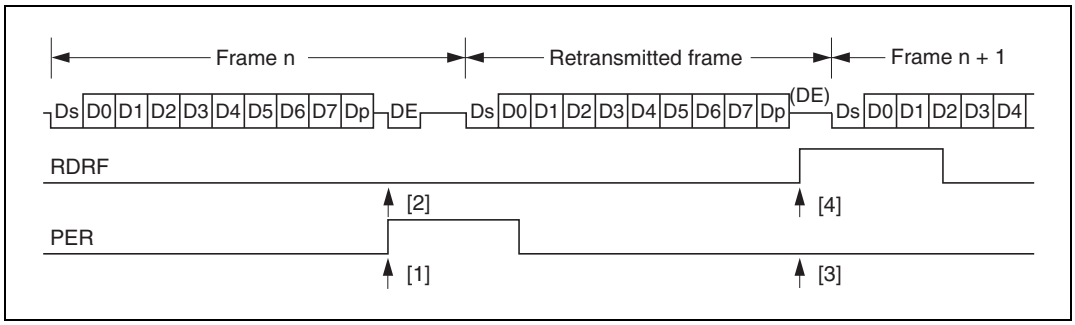


Figure 13.12 Retransmission in SCI Receive Mode

- Retransmission when SCI is in Transmit Mode

  Figure 13.13 illustrates retransmission when the SCI is in transmit mode.

6. If an error signal is sent back from the receiving device after transmission of one frame is completed, the ERS bit is set to 1 in SSR. If the RIE bit in SCR is set to the enable state, an ERI interrupt is requested. The ERS bit should be cleared to 0 in SSR before the next parity bit sampling timing.
7. The TEND bit in SSR is not set for the frame for which the error signal was received.
8. If an error signal is not sent back from the receiving device, the ERS flag is not set in SSR.
9. If an error signal is not sent back from the receiving device, transmission of one frame, including retransmission, is assumed to have been completed, and the TEND bit is set to 1 in SSR. If the TIE bit in SCR is set to the enable state, a TXI interrupt is requested.

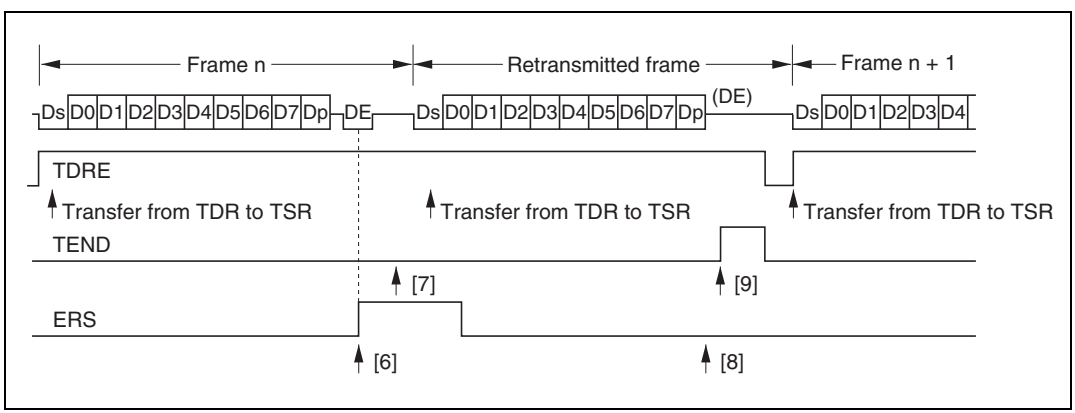


Figure 13.13 Retransmission in SCI Transmit Mode

14.1.4 Register Configuration

Table 14.2 summarizes the A/D converter's registers.

Table 14.2 A/D Converter Registers

Address*[1]	Name	Abbreviation	R/W	Initial Value
H'FFFE0	A/D data register A H	ADDRAH	R	H'00
H'FFFE1	A/D data register A L	ADDRAL	R	H'00
H'FFFE2	A/D data register B H	ADDRBH	R	H'00
H'FFFE3	A/D data register B L	ADDRBL	R	H'00
H'FFFE4	A/D data register C H	ADDRCH	R	H'00
H'FFFE5	A/D data register C L	ADDRCL	R	H'00
H'FFFE6	A/D data register D H	ADDRDH	R	H'00
H'FFFE7	A/D data register D L	ADDRDL	R	H'00
H'FFFE8	A/D control/status register	ADCSR	R/(W)*[2]	H'00
H'FFFE9	A/D control register	ADCR	R/W	H'7E

Notes: 1. Lower 20 bits of the address in advanced mode.
2. Only 0 can be written in bit 7, to clear the flag.

14.4.2 Scan Mode (SCAN = 1)

Scan mode is useful for monitoring analog inputs in a group of one or more channels. When the ADST bit is set to 1 by software or external trigger input, A/D conversion starts on the first channel in the group (AN_0 when CH2 = 0, AN_4 when CH2 = 1). When two or more channels are selected, after conversion of the first channel ends, conversion of the second channel (AN_1 or AN_5) starts immediately. A/D conversion continues cyclically on the selected channels until the ADST bit is cleared to 0. The conversion results are transferred for storage into the A/D data registers corresponding to the channels.

When the mode or analog input channel selection must be changed during analog conversion, to prevent incorrect operation, first clear the ADST bit to 0 in ADCSR to halt A/D conversion. After making the necessary changes, set the ADST bit to 1. A/D conversion will start again from the first channel in the group. The ADST bit can be set at the same time as the mode or channel selection is changed.

Typical operations when three channels in group 0 (AN_0 to AN_2) are selected in scan mode are described next. Figure 14.4 shows a timing diagram for this example.

1. Scan mode is selected (SCAN = 1), scan group 0 is selected (CH2 = 0), analog input channels AN_0 to AN_2 are selected (CH1 = 1, CH0 = 0), and A/D conversion is started (ADST = 1).
2. When A/D conversion of the first channel (AN_0) is completed, the result is transferred into ADDRA. Next, conversion of the second channel (AN_1) starts automatically.
3. Conversion proceeds in the same way through the third channel (AN_2).
4. When conversion of all selected channels (AN_0 to AN_2) is completed, the ADF flag is set to 1 and conversion of the first channel (AN_0) starts again. If the ADIE bit is set to 1, an ADI interrupt is requested when A/D conversion ends.
5. Steps 2 to 4 are repeated as long as the ADST bit remains set to 1. When the ADST bit is cleared to 0, A/D conversion stops. After that, if the ADST bit is set to 1, A/D conversion starts again from the first channel (AN_0).

18.2 Register Configuration

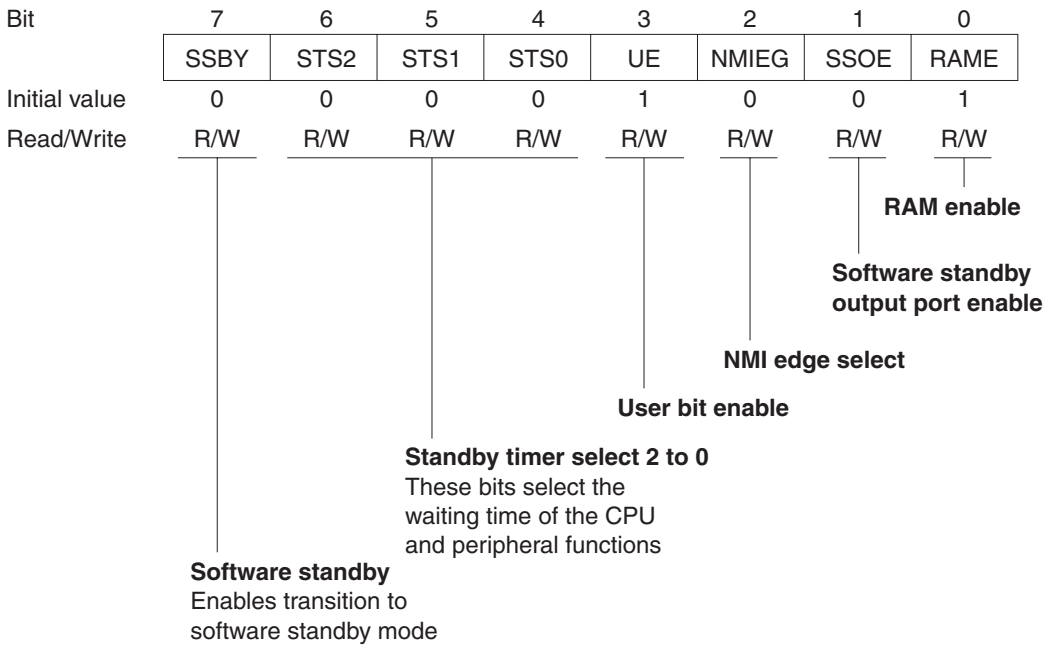
The H8/3008 has a system control register (SYSCR) that controls the power-down state, and module standby control registers H (MSTCRH) and L (MSTCRL) that control the module standby function. Table 18.2 summarizes these registers.

Table 18.2 Control Register

Address*	Name	Abbreviation	R/W	Initial Value
H'EE012	System control register	SYSCR	R/W	H'09
H'EE01C	Module standby control register H	MSTCRH	R/W	H'78
H'EE01D	Module standby control register L	MSTCRL	R/W	H'00

Note: * Lower 20 bits of the address in advanced mode.

18.2.1 System Control Register (SYSCR)



SYSCR is an 8-bit readable/writable register. Bit 7 (SSBY), bits 6 to 4 (STS2 to STS0), and bit 1 (SSOE) control the power-down state. For information on the other SYSCR bits, see section 3.3, System Control Register (SYSCR).

Item		Symbol	Min	Typ	Max	Unit	Test Conditions
Three-state leakage current	Ports 4 to 6, A_0 to A_{19}, Ports 8 to B	$\|I_{TSI}\|$	—	—	1.0	µA	V_{in} = 0.5 V to V_{CC} –0.5 V
	$\overline{RESO}$		—	—	10.0	µA	V_{in} = 0 V
Input pull-up MOS current	Ports 4 and 5	$-I_p$	50	—	300	µA	V_{in} = 0 V
Input capacitance	NMI	C_{in}	—	—	50	pF	Vin = 0 V f = fmin Ta = 25°C
	All input pins except NMI		—	—	15	pF	
Current dissipation*2	Normal operation	I_{CC}*3	—	32 (5.0 V)	47	mA	f = 20 MHz
			—	37 (5.0 V)	58	mA	f = 25 MHz
	Sleep mode		—	24 (5.0 V)	38	mA	f = 20 MHz
			—	29 (5.0 V)	47	mA	f = 25 MHz
	Module standby mode		—	19 (5.0 V)	31	mA	f = 20 MHz
			—	21 (5.0 V)	37	mA	f = 25 MHz
	Standby mode		—	1.0	10	µA	$T_a \leq 50°C$
			—	—	80	µA	$50°C < T_a$
Analog power supply current	During A/D conversion	AI_{CC}	—	0.6	1.5	mA	
	During A/D and D/A conversion		—	0.6	1.5	mA	
	Idle		—	0.01	5.0	µA	DASTE = 0
Reference current	During A/D conversion	AI_{CC}	—	0.45	0.8	mA	
	During A/D and D/A conversion		—	2.0	3.0	mA	
	Idle		—	0.01	5.0	µA	DASTE = 0
RAM standby voltage		V_{RAM}	2.0	—	—	V	

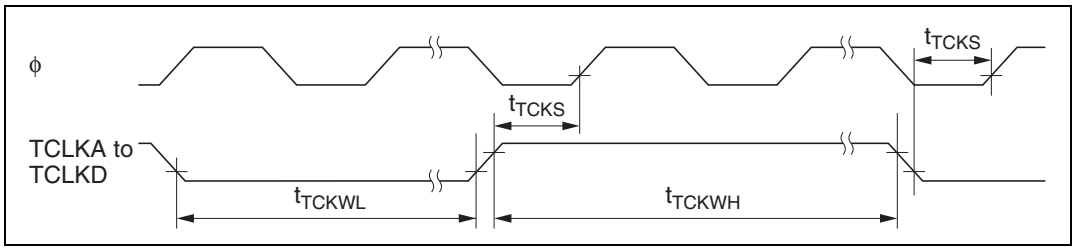


Figure 19.13 Timer External Clock Input Timing

19.6.6 SCI Input/Output Timing

SCI timing is shown as follows:

- SCI input clock timing
  Figure 19.14 shows the SCI input clock timing.
- SCI input/output timing (synchronous mode)
  Figure 19.15 shows the SCI input/output timing in synchronous mode.

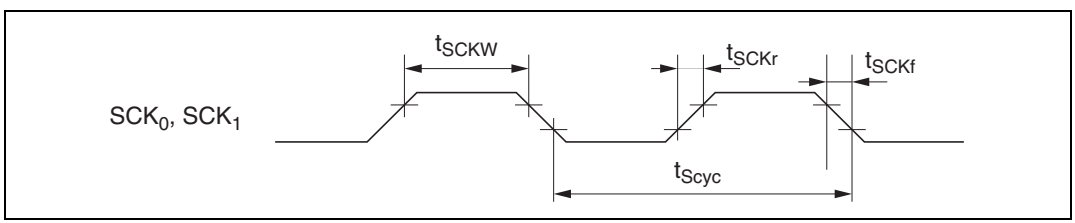


Figure 19.14 SCI Input Clock Timing

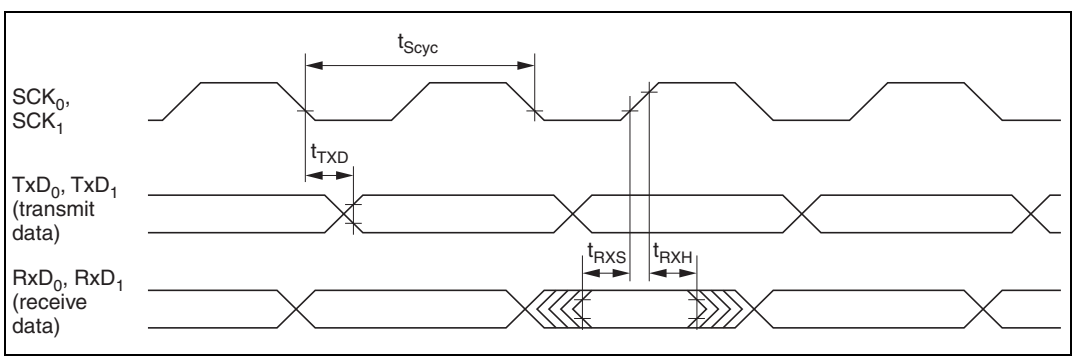


Figure 19.15 SCI Input/Output Timing in Synchronous Mode

Table A.3 Number of States per Cycle

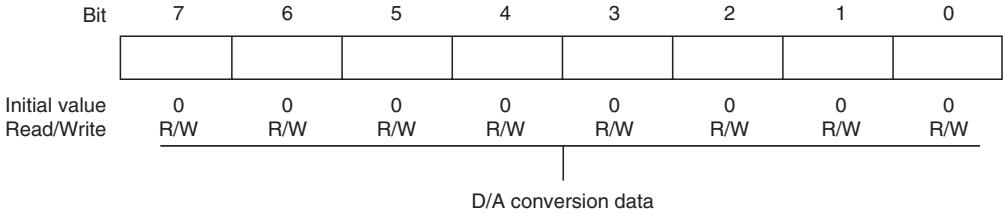
		Access Conditions						
			On-Chip Supporting Module		External Device			
					8-Bit Bus		16-Bit Bus	
Cycle		On-Chip Memory	8-Bit Bus	16-Bit Bus	2-State Access	3-State Access	2-State Access	3-State Access
Instruction fetch	S_I	2	6	3	4	6 + 2m	2	3 + m
Branch address read	S_J							
Stack operation	S_K							
Byte data access	S_L		3		2	3 + m		
Word data access	S_M		6		4	6 + 2m		
Internal operation	S_N	1						

Legend:

m: Number of wait states inserted into external device access

Address (Low)	Register Name	Data Bus Width	Bit Names								Module Name
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFF60	TSTR	8	—	—	—	—	—	STR2	STR1	STR0	16-bit timer, (all channels)
H'FFF61	TSNC	8	—	—	—	—	—	SYNC2	SYNC1	SYNC0	
H'FFF62	TMDR	8	—	MDF	FDIR	—	—	PWM2	PWM1	PWM0	
H'FFF63	TOLR	8	—	—	TOB2	TOA2	TOB1	TOA1	TOB0	TOA0	
H'FFF64	TISRA	8	—	IMIEA2	IMIEA1	IMIEA0	—	IMFA2	IMFA1	IMFA0	
H'FFF65	TISRB	8	—	IMIEB2	IMIEB1	IMIEB0	—	IMFB2	IMFB1	IMFB0	
H'FFF66	TISRC	8	—	OVIE2	OVIE1	OVIE0	—	OVF2	OVF1	OVF0	
H'FFF67	—		—	—	—	—	—	—	—	—	
H'FFF68	16TCR0	8	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	16-bit timer channel 0
H'FFF69	TIOR0	8	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0	
H'FFF6A	16TCNT0H	16									
H'FFF6B	16TCNT0L										
H'FFF6C	GRA0H	16									
H'FFF6D	GRA0L										
H'FFF6E	GRB0H	16									
H'FFF6F	GRB0L										
H'FFF70	16TCR1	8	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	16-bit timer channel 1
H'FFF71	TIOR1	8	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0	
H'FFF72	16TCNT1H	16									
H'FFF73	16TCNT1L										
H'FFF74	GRA1H	16									
H'FFF75	GRA1L										
H'FFF76	GRB1H	16									
H'FFF77	GRB1L										
H'FFF78	16TCR2	8	—	CCLR1	CCLR0	CKEG1	CKEG0	TPSC2	TPSC1	TPSC0	16-bit timer channel 2
H'FFF79	TIOR2	8	—	IOB2	IOB1	IOB0	—	IOA2	IOA1	IOA0	
H'FFF7A	16TCNT2H	16									
H'FFF7B	16TCNT2L										
H'FFF7C	GRA2H	16									
H'FFF7D	GRA2L										
H'FFF7E	GRB2H	16									
H'FFF7F	GRB2L										

DADR1—D/A Data Register 1 **H'FFF9D** **D/A**



C.4 Port 8 Block Diagrams

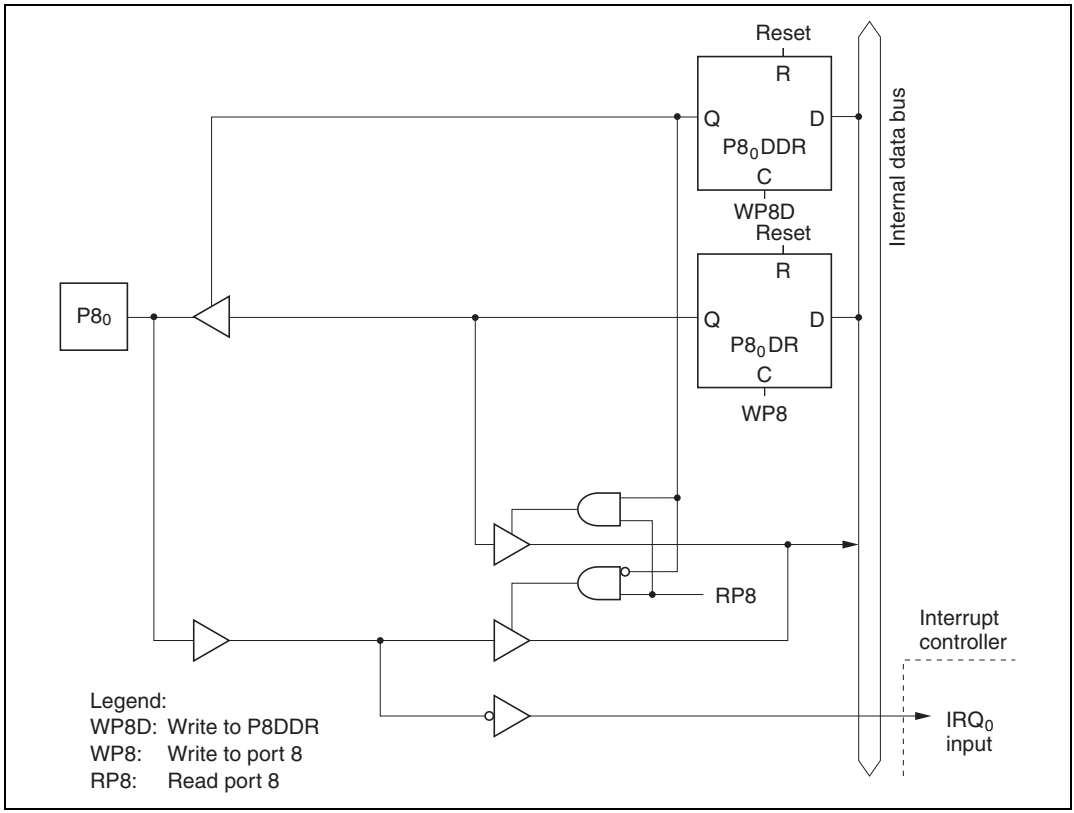


Figure C.4 (a) Port 8 Block Diagram (Pin P8$_0$)

C.5 Port 9 Block Diagrams

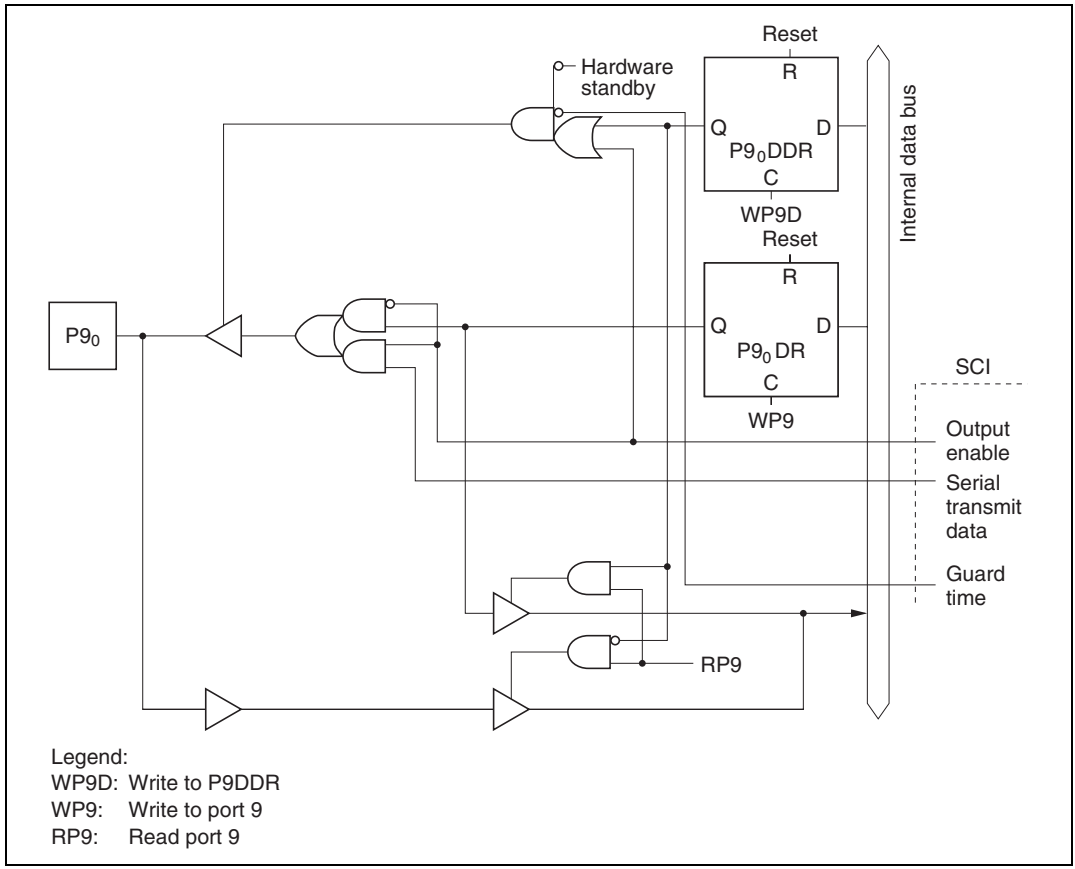


Figure C.5 (a) Port 9 Block Diagram (Pin P9$_0$)