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What Are Embedded - Microcontrollers - Application Specific?

Application specific microcontrollers are engineered to

Details

Product Status	Active
Applications	USB Microcontroller
Core Processor	8051
Program Memory Type	ROMless
Controller Series	CY7C680xx
RAM Size	16K x 8
Interface	I ² C, USB, USART
Number of I/O	40
Voltage - Supply	3V ~ 3.6V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-TQFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c68013a-100axi

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the application note [AN65209 - Getting Started with FX2LP](#).

- Overview: [USB Portfolio](#), [USB Roadmap](#)
- USB 2.0 Product Selectors: [FX2LP](#), [AT2LP](#), [NX2LP-Flex](#), [SX2](#)
- Application notes: Cypress offers a large number of USB application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with FX2LP are:
 - [AN65209](#) - Getting Started with FX2LP
 - [AN15456](#) - Guide to Successful EZ-USB® FX2LP™ and EZ-USB FX1™ Hardware Design and Debug
 - [AN50963](#) - EZ-USB® FX1™/FX2LP™ Boot Options
 - [AN66806](#) - EZ-USB® FX2LP™ GPIF Design Guide
 - [AN61345](#) - Implementing an FX2LP™- FPGA Interface
 - [AN57322](#) - Interfacing SRAM with FX2LP over GPIF
 - [AN4053](#) - Streaming Data through Isochronous/Bulk Endpoints on EZ-USB® FX2 and EZUSB FX2LP
 - [AN63787](#) - EZ-USB® FX2LP™ GPIF and Slave FIFO Configuration Examples using 8-bit Asynchronous Interface

For complete list of Application notes, [click here](#).

- Code Examples:
 - [USB Hi-Speed](#)
- Technical Reference Manual (TRM):
 - [EZ-USB FX2LP Technical Reference Manual](#)
- Reference Designs:
 - [CY4661 - External USB Hard Disk Drives \(HDD\) with Fingerprint Authentication Security](#)
 - [FX2LP DMB-T/H TV Dongle reference design](#)
- Models: [IBIS](#)

EZ-USB FX2LP Development Kit

The [CY3684 EZ-USB FX2LP Development Kit](#) is a complete development resource for FX2LP. It provides a platform to develop and test custom projects using FX2LP. The development kit contains collateral materials for the firmware, hardware, and software aspects of a design using FX2LP.

GPIF™ Designer

FX2LP™ General Programmable Interface (GPIF) provides an independent hardware unit, which creates the data and control signals required by an external interface. FX2LP GPIF Designer allows users to create and modify GPIF waveform descriptors for EZ-USB FX2/ FX2LP family of chips using a graphical user interface. Extensive discussion of general GPIF discussion and programming using GPIF Designer is included in [FX2LP Technical Reference Manual](#) and [GPIF Designer User Guide](#), distributed with GPIF Designer. [AN66806 - Getting Started with EZ-USB® FX2LP™ GPIF](#) can be a good starting point.

The FX2LP jump instruction is encoded as follows:

Table 3. INT2 USB Interrupts

USB INTERRUPT TABLE FOR INT2			
Priority	INT2VEC Value	Source	Notes
1	00	SUDAV	Setup data available
2	04	SOF	Start of frame (or microframe)
3	08	SUTOK	Setup token received
4	0C	SUSPEND	USB suspend request
5	10	USB RESET	Bus reset
6	14	HISPEED	Entered high speed operation
7	18	EP0ACK	FX2LP ACK'd the CONTROL Handshake
8	1C		reserved
9	20	EP0-IN	EP0-IN ready to be loaded with data
10	24	EP0-OUT	EP0-OUT has USB data
11	28	EP1-IN	EP1-IN ready to be loaded with data
12	2C	EP1-OUT	EP1-OUT has USB data
13	30	EP2	IN: buffer available. OUT: buffer has data
14	34	EP4	IN: buffer available. OUT: buffer has data
15	38	EP6	IN: buffer available. OUT: buffer has data
16	3C	EP8	IN: buffer available. OUT: buffer has data
17	40	IBN	IN-Bulk-NAK (any IN endpoint)
18	44		reserved
19	48	EP0PING	EP0 OUT was pinged and it NAK'd
20	4C	EP1PING	EP1 OUT was pinged and it NAK'd
21	50	EP2PING	EP2 OUT was pinged and it NAK'd
22	54	EP4PING	EP4 OUT was pinged and it NAK'd
23	58	EP6PING	EP6 OUT was pinged and it NAK'd
24	5C	EP8PING	EP8 OUT was pinged and it NAK'd
25	60	ERRLIMIT	Bus errors exceeded the programmed limit
26	64	–	–
27	68	–	Reserved
28	6C	–	Reserved
29	70	EP2ISOERR	ISO EP2 OUT PID sequence error
30	74	EP4ISOERR	ISO EP4 OUT PID sequence error
31	78	EP6ISOERR	ISO EP6 OUT PID sequence error
32	7C	EP8ISOERR	ISO EP8 OUT PID sequence error

If Autovectoring is enabled (AV2EN = 1 in the INTSET-UP register), the FX2LP substitutes its INT2VEC byte. Therefore, if the high byte ("page") of a jump table address is preloaded at the location 0x0044, the automatically inserted INT2VEC byte at 0x0045 directs the jump to the correct address out of the 27 addresses within the page.

FIFO/GPIF Interrupt (INT4)

Just as the USB Interrupt is shared among 27 individual USB interrupt sources, the FIFO/GPIF interrupt is shared among 14 individual FIFO/GPIF sources. The FIFO/GPIF Interrupt, similar to the USB Interrupt, can employ autovectoring.

[Table 4 on page 8](#) shows the priority and INT4VEC values for the 14 FIFO/GPIF interrupt sources.

Reset and Wakeup

Reset Pin

The input pin, RESET#, resets the FX2LP when asserted. This pin has hysteresis and is active LOW. When a crystal is used with the CY7C680xxA, the reset period must enable stabilization of the crystal and the PLL. This reset period must be approximately 5 ms after VCC reaches 3.0 V. If the crystal input pin is driven by a clock signal, the internal PLL stabilizes in 200 μ s after VCC has reached 3.0 V^[4].

Figure 2 on page 9 shows a power-on reset condition and a reset applied during operation. A power-on reset is defined as the time reset that is asserted while power is being applied to the circuit. A powered reset is when the FX2LP is powered on and operating and the RESET# pin is asserted.

Cypress provides an application note which describes and recommends power-on reset implementation. For more information about reset implementation for the FX2 family of products, visit <http://www.cypress.com>.

Figure 2. Reset Timing Plots

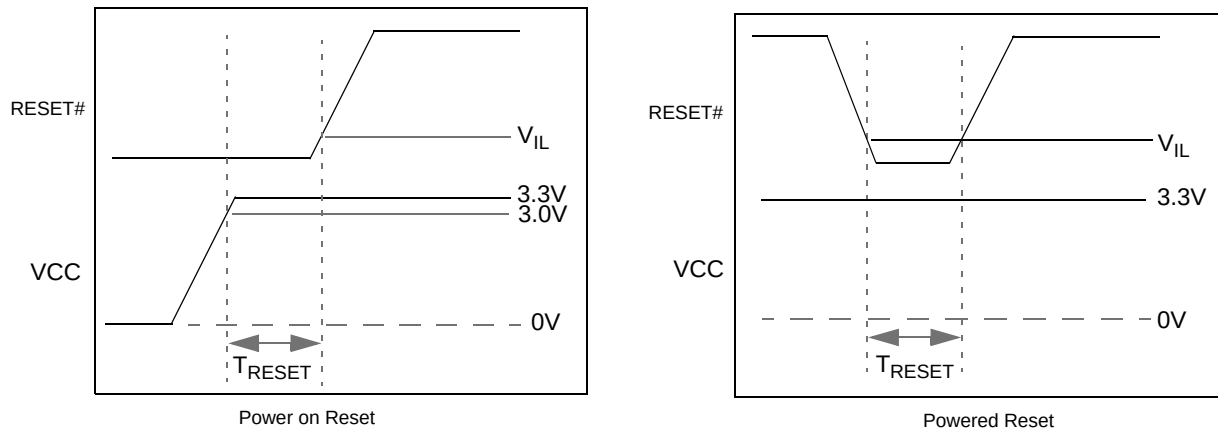


Table 5. Reset Timing Values

Condition	T_{RESET}
Power-on reset with crystal	5 ms
Power-on reset with external clock	200 μ s + clock stability time
Powered reset	200 μ s

Wakeup Pins

The 8051 puts itself and the rest of the chip into a power-down mode by setting PCON.0 = 1. This stops the oscillator and PLL. When WAKEUP is asserted by external logic, the oscillator restarts after the PLL stabilizes, and the 8051 receives a wakeup interrupt. This applies irrespective of whether FX2LP is connected to the USB.

The FX2LP exits the power-down (USB suspend) state by using one of the following methods:

- USB bus activity (if D+/D- lines are left floating, noise on these lines may indicate activity to the FX2LP and initiate a wakeup)
- External logic asserts the WAKEUP pin
- External logic asserts the PA3/WU2 pin

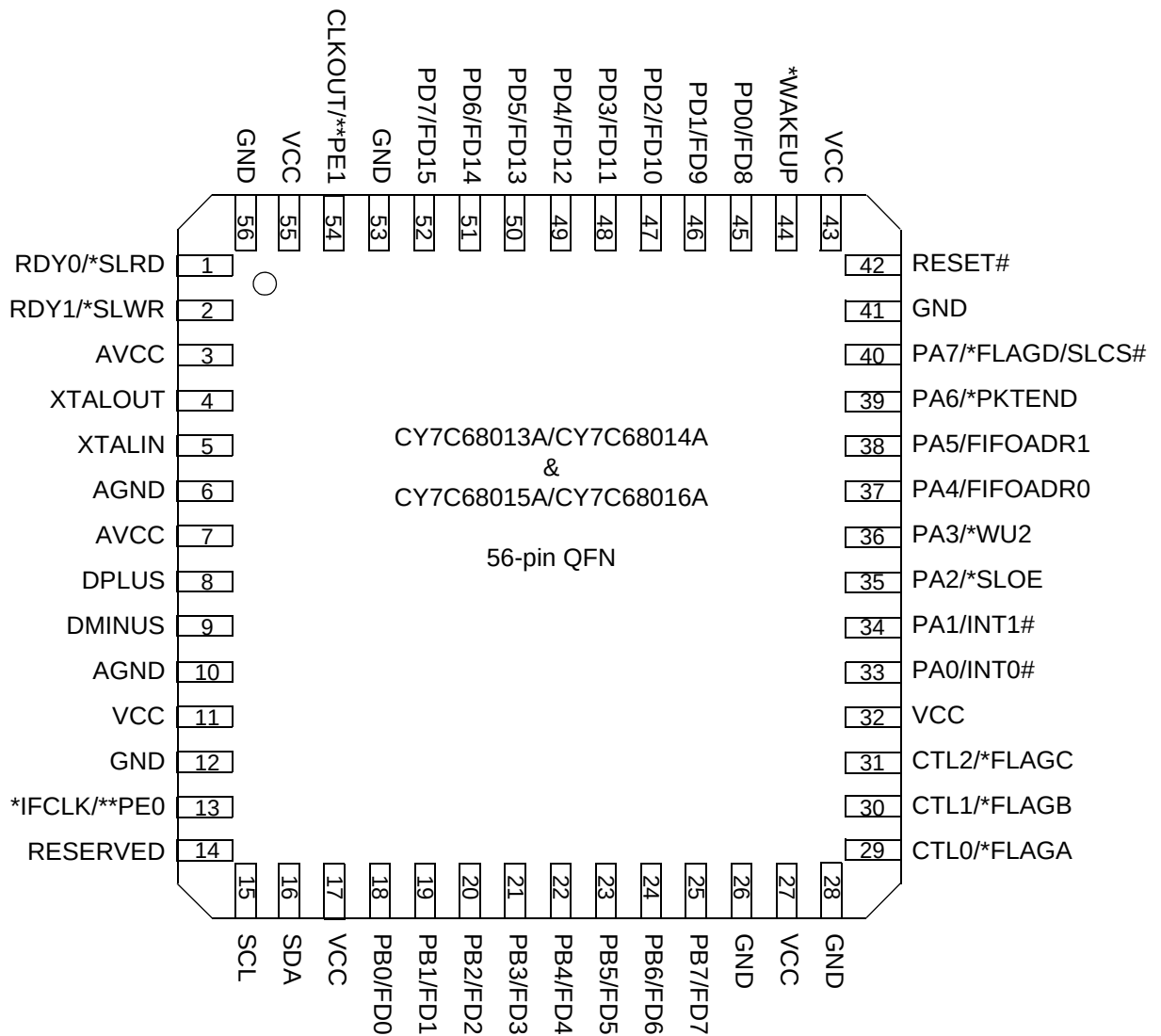
The second wakeup pin, WU2, can also be configured as a general-purpose I/O pin. This enables a simple external R-C network to be used as a periodic wakeup source. WAKEUP is by default active LOW.

Figure 9. CY7C68013A/CY7C68014A 56-Pin SSOP Pin Assignment

CY7C68013A/CY7C68014A 56-pin SSOP			
1	PD5/FD13	PD4/FD12	56
2	PD6/FD14	PD3/FD11	55
3	PD7/FD15	PD2/FD10	54
4	GND	PD1/FD9	53
5	CLKOUT	PD0/FD8	52
6	VCC	*WAKEUP	51
7	GND	VCC	50
8	RDY0/*SLRD	RESET#	49
9	RDY1/*SLWR	GND	48
10	AVCC	PA7/*FLAGD/SLCS#	47
11	XTALOUT	PA6/PKTEND	46
12	XTALIN	PA5/FIFOADR1	45
13	AGND	PA4/FIFOADR0	44
14	AVCC	PA3/*WU2	43
15	DPLUS	PA2/*SLOE	42
16	DMINUS	PA1/INT1#	41
17	AGND	PA0/INT0#	40
18	VCC	VCC	39
19	GND	CTL2/*FLAGC	38
20	*IFCLK	CTL1/*FLAGB	37
21	RESERVED	CTL0/*FLAGA	36
22	SCL	GND	35
23	SDA	VCC	34
24	VCC	GND	33
25	PB0/FD0	PB7/FD7	32
26	PB1/FD1	PB6/FD6	31
27	PB2/FD2	PB5/FD5	30
28	PB3/FD3	PB4/FD4	29

* denotes programmable polarity

Figure 10. CY7C68013A/14A/15A/16A 56-Pin QFN Pin Assignment



* denotes programmable polarity
** denotes CY7C68015A/CY7C68016A pinout

Table 11. FX2LP Pin Descriptions^[11] (continued)

128 TQFP	100 TQFP	56 SSOP	56 QFN	56 VFBGA	Name	Type	Default	Reset ^[12]	Description
30	24	—	—	—	T1	Input	N/A	N/A	T1 is the active HIGH T1 signal for 8051 Timer1, which provides the input to Timer1 when C/T1 is 1. When C/T1 is 0, Timer1 does not use this bit.
29	23	—	—	—	T0	Input	N/A	N/A	T0 is the active HIGH T0 signal for 8051 Timer0, which provides the input to Timer0 when C/T0 is 1. When C/T0 is 0, Timer0 does not use this bit.
53	43	—	—	—	RXD1	Input	N/A	N/A	RXD1 is an active HIGH input signal for 8051 UART1, which provides data to the UART in all modes.
52	42	—	—	—	TXD1	Output	H	L	TXD1 is an active HIGH output pin from 8051 UART1, which provides the output clock in sync mode, and the output data in async mode.
51	41	—	—	—	RXD0	Input	N/A	N/A	RXD0 is the active HIGH RXD0 input to 8051 UART0, which provides data to the UART in all modes.
50	40	—	—	—	TXD0	Output	H	L	TXD0 is the active HIGH TXD0 output from 8051 UART0, which provides the output clock in sync mode, and the output data in async mode.
42		—	—	—	CS#	Output	H	H	CS# is the active LOW chip select for external memory.
41	32	—	—	—	WR#	Output	H	H	WR# is the active LOW write strobe output for external memory.
40	31	—	—	—	RD#	Output	H	H	RD# is the active LOW read strobe output for external memory.
38		—	—	—	OE#	Output	H	H	OE# is the active LOW output enable for external memory.
33	27	21	14	2H	Reserved	Input	N/A	N/A	Reserved. Connect to ground.
101	79	51	44	7B	WAKEUP	Input	N/A	N/A	USB Wakeup. If the 8051 is in suspend, asserting this pin starts up the oscillator and interrupts the 8051 to enable it to exit the suspend mode. Holding WAKEUP asserted inhibits the EZ-USB chip from suspending. This pin has programmable polarity (WAKEUP.4).
36	29	22	15	3F	SCL	OD	Z	Z (if booting is done)	Clock for the I ² C interface. Connect to VCC with a 2.2-kΩ resistor, even if no I ² C peripheral is attached.
37	30	23	16	3G	SDA	OD	Z	Z (if booting is done)	Data for I ² C compatible interface. Connect to VCC with a 2.2-kΩ resistor, even if no I²C compatible peripheral is attached.
2	1	6	55	5A	VCC	Power	N/A	N/A	VCC. Connect to the 3.3-V power source.
26	20	18	11	1G	VCC	Power	N/A	N/A	VCC. Connect to the 3.3-V power source.
43	33	24	17	7E	VCC	Power	N/A	N/A	VCC. Connect to the 3.3-V power source.
48	38	—	—	—	VCC	Power	N/A	N/A	VCC. Connect to 3.3-V power source.
64	49	34	27	8E	VCC	Power	N/A	N/A	VCC. Connect to the 3.3-V power source.
68	53	—	—	—	VCC	Power	N/A	N/A	VCC. Connect to the 3.3-V power source.
81	66	39	32	5C	VCC	Power	N/A	N/A	VCC. Connect to the 3.3-V power source.

Table 12. FX2LP Register Summary (continued)

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
E65D	1	USBIRQ ^[14]	USB Interrupt Requests	0	EP0ACK	HSGRANT	URES	SUSP	SUTOK	SOF	SUDAV	0xxxxxxx	rrrrrrrr
E65E	1	EPIE	Endpoint Interrupt Enables	EP8	EP6	EP4	EP2	EP1OUT	EP1IN	EP0OUT	EP0IN	00000000	RW
E65F	1	EPIRQ ^[14]	Endpoint Interrupt Requests	EP8	EP6	EP4	EP2	EP1OUT	EP1IN	EP0OUT	EP0IN	0	RW
E660	1	GPIFIE ^[13]	GPIF Interrupt Enable	0	0	0	0	0	0	GPIFWF	GPIFDONE	00000000	RW
E661	1	GPIFIQ ^[13]	GPIF Interrupt Request	0	0	0	0	0	0	GPIFWF	GPIFDONE	000000xx	RW
E662	1	USBERRIE	USB Error Interrupt Enables	ISOEP8	ISOEP6	ISOEP4	ISOEP2	0	0	0	ERRLIMIT	00000000	RW
E663	1	USBERRIRQ ^[14]	USB Error Interrupt Requests	ISOEP8	ISOEP6	ISOEP4	ISOEP2	0	0	0	ERRLIMIT	0000000x	bbbbrrrr
E664	1	ERRCNTLIM	USB Error counter and limit	EC3	EC2	EC1	EC0	LIMIT3	LIMIT2	LIMIT1	LIMIT0	xxxx0100	rrrrrrrr
E665	1	CLRERRCNT	Clear Error Counter EC3:0	x	x	x	x	x	x	x	x	xxxxxxx	W
E666	1	INT2IVEC	Interrupt 2 (USB) Autovector	0	I2V4	I2V3	I2V2	I2V1	I2V0	0	0	00000000	R
E667	1	INT4IVEC	Interrupt 4 (slave FIFO & GPIF) Autovector	1	0	I4V3	I4V2	I4V1	I4V0	0	0	10000000	R
E668	1	INTSET-UP	Interrupt 2&4 setup	0	0	0	0	AV2EN	0	INT4SRC	AV4EN	00000000	RW
E669	7	reserved											
INPUT / OUTPUT													
E670	1	PORTACFG	I/O PORTA Alternate Configuration	FLAGD	SLCS	0	0	0	0	INT1	INT0	00000000	RW
E671	1	PORTCCFG	I/O PORTC Alternate Configuration	GPIFA7	GPIFA6	GPIFA5	GPIFA4	GPIFA3	GPIFA2	GPIFA1	GPIFA0	00000000	RW
E672	1	PORTTECFG	I/O PORTE Alternate Configuration	GPIFA8	T2EX	INT6	RXD1OUT	RXD0OUT	T2OUT	T1OUT	T0OUT	00000000	RW
E673	4	reserved											
E677	1	reserved											
E678	1	I ² CS	I ² C Bus Control & Status	START	STOP	LASTRD	ID1	ID0	BERR	ACK	DONE	000xx000	bbbbrrrr
E679	1	I2DAT	I ² C Bus Data	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxx	RW
E67A	1	I ² CTL	I ² C Bus Control	0	0	0	0	0	0	STOPIE	400KHZ	00000000	RW
E67B	1	XAUTODAT1	Autoptr1 MOVX access, when APTREN=1	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxx	RW
E67C	1	XAUTODAT2	Autoptr2 MOVX access, when APTREN=1	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxx	RW
UDMA CRC													
E67D	1	UDMACRCH ^[13]	UDMA CRC MSB	CRC15	CRC14	CRC13	CRC12	CRC11	CRC10	CRC9	CRC8	01001010	RW
E67E	1	UDMACRCL ^[13]	UDMA CRC LSB	CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0	10111010	RW
E67F	1	UDMACRC-QUALIFIER	UDMA CRC Qualifier	QENABLE	0	0	0	QSTATE	QSIGNA2	QSIGNA1	QSIGNA0	00000000	bbbbrrrr
USB CONTROL													
E680	1	USBCS	USB Control & Status	HSM	0	0	0	DISCON	NOSYNOSF	RENUM	SIGRSUME	x0000000	rrrrrrrr
E681	1	SUSPEND	Put chip into suspend	x	x	x	x	x	x	x	x	xxxxxxx	W
E682	1	WAKEUPCS	Wakeup Control & Status	WU2	WU	WU2POL	WUPOL	0	DPEN	WU2EN	WUEN	xx000101	bbbbrrrr
E683	1	TOGCTL	Toggle Control	Q	S	R	I/O	EP3	EP2	EP1	EP0	x0000000	rrrrrrrr
E684	1	USBFRAMEH	USB Frame count H	0	0	0	0	0	FC10	FC9	FC8	00000xxx	R
E685	1	USBFRAMEL	USB Frame count L	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	xxxxxxx	R
E686	1	MICROFRAME	Microframe count, 0-7	0	0	0	0	0	MF2	MF1	MF0	00000xxx	R
E687	1	FNADDR	USB Function address	0	FA6	FA5	FA4	FA3	FA2	FA1	FA0	0xxxxxxx	R
E688	2	reserved											
ENDPOINTS													
E68A	1	EP0BCH ^[13]	Endpoint 0 Byte Count H	(BC15)	(BC14)	(BC13)	(BC12)	(BC11)	(BC10)	(BC9)	(BC8)	xxxxxxx	RW
E68B	1	EP0BCL ^[13]	Endpoint 0 Byte Count L	(BC7)	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxx	RW
E68C	1	reserved											
E68D	1	EP1OUTBC	Endpoint 1 OUT Byte Count	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	0xxxxxxx	RW
E68E	1	reserved											
E68F	1	EP1INBC	Endpoint 1 IN Byte Count	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	0xxxxxxx	RW
E690	1	EP2BCH ^[13]	Endpoint 2 Byte Count H	0	0	0	0	0	BC10	BC9	BC8	00000xxx	RW
E691	1	EP2BCL ^[13]	Endpoint 2 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxx	RW
E692	2	reserved											
E694	1	EP4BCH ^[13]	Endpoint 4 Byte Count H	0	0	0	0	0	0	BC9	BC8	00000xxx	RW
E695	1	EP4BCL ^[13]	Endpoint 4 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxx	RW
E696	2	reserved											
E698	1	EP6BCH ^[13]	Endpoint 6 Byte Count H	0	0	0	0	0	BC10	BC9	BC8	00000xxx	RW
E699	1	EP6BCL ^[13]	Endpoint 6 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxx	RW
E69A	2	reserved											
E69C	1	EP8BCH ^[13]	Endpoint 8 Byte Count H	0	0	0	0	0	0	BC9	BC8	00000xxx	RW
E69D	1	EP8BCL ^[13]	Endpoint 8 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxx	RW
E69E	2	reserved											

Table 12. FX2LP Register Summary (continued)

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
E6CF	1	GPIFTCB2 ^[13]	GPIF Transaction Count Byte 2	TC23	TC22	TC21	TC20	TC19	TC18	TC17	TC16	00000000	RW
E6D0	1	GPIFTCB1 ^[13]	GPIF Transaction Count Byte 1	TC15	TC14	TC13	TC12	TC11	TC10	TC9	TC8	00000000	RW
E6D1	1	GPIFTCB0 ^[13]	GPIF Transaction Count Byte 0	TC7	TC6	TC5	TC4	TC3	TC2	TC1	TC0	00000001	RW
	2	reserved										00000000	RW
		reserved											
		reserved											
E6D2	1	EP2GPIFFLGSEL ^[13]	Endpoint 2 GPIF Flag select	0	0	0	0	0	0	FS1	FS0	00000000	RW
E6D3	1	EP2GPIFPFSTOP	Endpoint 2 GPIF stop transaction on prog. flag	0	0	0	0	0	0	0	FIFO2FLAG	00000000	RW
E6D4	1	EP2GPIFTRIG ^[13]	Endpoint 2 GPIF Trigger	x	x	x	x	x	x	x	x	xxxxxxx	W
	3	reserved											
		reserved											
		reserved											
E6DA	1	EP4GPIFFLGSEL ^[13]	Endpoint 4 GPIF Flag select	0	0	0	0	0	0	FS1	FS0	00000000	RW
E6DB	1	EP4GPIFPFSTOP	Endpoint 4 GPIF stop transaction on GPIF Flag	0	0	0	0	0	0	0	FIFO4FLAG	00000000	RW
E6DC	1	EP4GPIFTRIG ^[13]	Endpoint 4 GPIF Trigger	x	x	x	x	x	x	x	x	xxxxxxx	W
	3	reserved											
		reserved											
		reserved											
E6E2	1	EP6GPIFFLGSEL ^[13]	Endpoint 6 GPIF Flag select	0	0	0	0	0	0	FS1	FS0	00000000	RW
E6E3	1	EP6GPIFPFSTOP	Endpoint 6 GPIF stop transaction on prog. flag	0	0	0	0	0	0	0	FIFO6FLAG	00000000	RW
E6E4	1	EP6GPIFTRIG ^[13]	Endpoint 6 GPIF Trigger	x	x	x	x	x	x	x	x	xxxxxxx	W
	3	reserved											
		reserved											
		reserved											
E6EA	1	EP8GPIFFLGSEL ^[13]	Endpoint 8 GPIF Flag select	0	0	0	0	0	0	FS1	FS0	00000000	RW
E6EB	1	EP8GPIFPFSTOP	Endpoint 8 GPIF stop transaction on prog. flag	0	0	0	0	0	0	0	FIFO8FLAG	00000000	RW
E6EC	1	EP8GPIFTRIG ^[13]	Endpoint 8 GPIF Trigger	x	x	x	x	x	x	x	x	xxxxxxx	W
	3	reserved											
E6F0	1	XGPIFSGLDATH	GPIF Data H (16-bit mode only)	D15	D14	D13	D12	D11	D10	D9	D8	xxxxxxx	RW
E6F1	1	XGPIFSGLDATHX	Read/Write GPIF Data L & trigger transaction	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxx	RW
E6F2	1	XGPIFSGLDATHNOX	Read GPIF Data L, no transaction trigger	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxx	R
E6F3	1	GPIFREADYCFG	Internal RDY, Sync/Async, RDY pin states	INTRDY	SAS	TCXRDY5	0	0	0	0	0	00000000	bbbbrrrr
E6F4	1	GPIFREADYSTAT	GPIF Ready Status	0	0	RDY5	RDY4	RDY3	RDY2	RDY1	RDY0	00xxxxx	R
E6F5	1	GPIFABORT	Abort GPIF Waveforms	x	x	x	x	x	x	x	x	xxxxxxx	W
E6F6	2	reserved											
		ENDPOINT BUFFERS											
E740	64	EP0BUF	EP0-IN/-OUT buffer	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxx	RW
E780	64	EP10UTBUF	EP1-OUT buffer	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxx	RW
E7C0	64	EP1INBUF	EP1-IN buffer	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxx	RW
E800	2048	reserved											RW
F000	1024	EP2FIFOBUF	512/1024 byte EP 2 / slave FIFO buffer (IN or OUT)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxx	RW
F400	512	EP4FIFOBUF	512 byte EP 4 / slave FIFO buffer (IN or OUT)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxx	RW
F600	512	reserved											
F800	1024	EP6FIFOBUF	512/1024 byte EP 6 / slave FIFO buffer (IN or OUT)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxx	RW
FC00	512	EP8FIFOBUF	512 byte EP 8 / slave FIFO buffer (IN or OUT)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxx	RW
FE00	512	reserved											

Table 12. FX2LP Register Summary (continued)

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
xxxx		IPC Configuration Byte		0	DISCON	0	0	0	0	0	400KHZ	xxxxxxxx [16]	n/a
		Special Function Registers (SFRs)											
80	1	IOA ^[15]	Port A (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
81	1	SP	Stack Pointer	D7	D6	D5	D4	D3	D2	D1	D0	00000111	RW
82	1	DPL0	Data Pointer 0 L	A7	A6	A5	A4	A3	A2	A1	A0	00000000	RW
83	1	DPH0	Data Pointer 0 H	A15	A14	A13	A12	A11	A10	A9	A8	00000000	RW
84	1	DPL1 ^[15]	Data Pointer 1 L	A7	A6	A5	A4	A3	A2	A1	A0	00000000	RW
85	1	DPH1 ^[15]	Data Pointer 1 H	A15	A14	A13	A12	A11	A10	A9	A8	00000000	RW
86	1	DPS ^[15]	Data Pointer 0/1 select	0	0	0	0	0	0	0	SEL	00000000	RW
87	1	PCON	Power Control	SMOD0	x	1	1	x	x	x	IDLE	00110000	RW
88	1	TCON	Timer/Counter Control (bit addressable)	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00000000	RW
89	1	TMOD	Timer/Counter Mode Control	GATE	CT	M1	M0	GATE	CT	M1	M0	00000000	RW
8A	1	TL0	Timer 0 reload L	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
8B	1	TL1	Timer 1 reload L	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
8C	1	TH0	Timer 0 reload H	D15	D14	D13	D12	D11	D10	D9	D8	00000000	RW
8D	1	TH1	Timer 1 reload H	D15	D14	D13	D12	D11	D10	D9	D8	00000000	RW
8E	1	CKCON ^[15]	Clock Control	x	x	T2M	T1M	T0M	MD2	MD1	MD0	00000001	RW
8F	1	reserved											
90	1	IOB ^[15]	Port B (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
91	1	EXIF ^[15]	External Interrupt Flag(s)	IE5	IE4	IPCINT	USBNT	1	0	0	0	00001000	RW
92	1	MPAGE ^[15]	Upper Addr Byte of MOVX using @R0 / @R1	A15	A14	A13	A12	A11	A10	A9	A8	00000000	RW
93	5	reserved											
98	1	SCON0	Serial Port 0 Control (bit addressable)	SM0_0	SM1_0	SM2_0	REN_0	TB8_0	RB8_0	TI_0	RI_0	00000000	RW
99	1	SBUF0	Serial Port 0 Data Buffer	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
9A	1	AUTOPTRH1 ^[15]	Autopointer 1 Address H	A15	A14	A13	A12	A11	A10	A9	A8	00000000	RW
9B	1	AUTOPTRL1 ^[15]	Autopointer 1 Address L	A7	A6	A5	A4	A3	A2	A1	A0	00000000	RW
9C	1	reserved											
9D	1	AUTOPTRH2 ^[15]	Autopointer 2 Address H	A15	A14	A13	A12	A11	A10	A9	A8	00000000	RW
9E	1	AUTOPTRL2 ^[15]	Autopointer 2 Address L	A7	A6	A5	A4	A3	A2	A1	A0	00000000	RW
9F	1	reserved											
A0	1	IOC ^[15]	Port C (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
A1	1	INT2CLR ^[15]	Interrupt 2 clear	x	x	x	x	x	x	x	x	xxxxxxxx	W
A2	1	INT4CLR ^[15]	Interrupt 4 clear	x	x	x	x	x	x	x	x	xxxxxxxx	W
A3	5	reserved											
A8	1	IE	Interrupt Enable (bit addressable)	EA	ES1	ET2	ES0	ET1	EX1	ET0	EX0	00000000	RW
A9	1	reserved											
AA	1	EP2468STAT ^[15]	Endpoint 2,4,6,8 status flags	EP8F	EP8E	EP6F	EP6E	EP4F	EP4E	EP2F	EP2E	01011010	R
AB	1	EP24FIFOFLGS ^[15]	Endpoint 2,4 slave FIFO status flags	0	EP4PF	EP4EF	EP4FF	0	EP2PF	EP2EF	EP2FF	00100010	R
AC	1	EP68FIFOFLGS ^[15]	Endpoint 6,8 slave FIFO status flags	0	EP8PF	EP8EF	EP8FF	0	EP6PF	EP6EF	EP6FF	01100110	R
AD	2	reserved											
AF	1	AUTOPTRSETUP ^[15]	Autopointer 1&2 setup	0	0	0	0	0	APTR2INC	APTR1INC	APTREN	00000110	RW
B0	1	IOD ^[15]	Port D (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
B1	1	IOE ^[15]	Port E (NOT bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
B2	1	OEA ^[15]	Port A Output Enable	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
B3	1	OEB ^[15]	Port B Output Enable	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
B4	1	OEC ^[15]	Port C Output Enable	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
B5	1	OED ^[15]	Port D Output Enable	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
B6	1	OEE ^[15]	Port E Output Enable	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
B7	1	reserved											
B8	1	IP	Interrupt Priority (bit addressable)	1	PS1	PT2	PS0	PT1	PX1	PT0	PX0	10000000	RW
B9	1	reserved											
BA	1	EP01STAT ^[15]	Endpoint 0&1 Status	0	0	0	0	0	EP1INBSY	EP1OUTBSY	EP0BSY	00000000	R
BB	1	GPIFTRIG ^[15, 13]	Endpoint 2,4,6,8 GPIF slave FIFO Trigger	DONE	0	0	0	0	RW	EP1	EP0	10000xxx	brrrrbbb
BC	1	reserved											
BD	1	GPIFSGLDATH ^[15]	GPIF Data H (16-bit mode only)	D15	D14	D13	D12	D11	D10	D9	D8	xxxxxxxx	RW

Notes

15. SFRs not part of the standard 8051 architecture.

16. If no EEPROM is detected by the SIE then the default is 00000000.

Table 12. FX2LP Register Summary (continued)

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
BE	1	GPIFSGLDATLX ^[15]	GPIF Data L w/ Trigger	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxx	RW
BF	1	GPIFSGLDATL- NOX ^[15]	GPIF Data L w/ No Trigger	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxx	R
C0	1	SCON1 ^[15]	Serial Port 1 Control (bit addressable)	SM0_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	00000000	RW
C1	1	SBUF1 ^[15]	Serial Port 1 Data Buffer	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
C2	6	reserved											
C8	1	T2CON	Timer/Counter 2 Control (bit addressable)	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2	CPRL2	00000000	RW
C9	1	reserved											
CA	1	RCAP2L	Capture for Timer 2, au- to-reload, up-counter	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
CB	1	RCAP2H	Capture for Timer 2, au- to-reload, up-counter	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
CC	1	TL2	Timer 2 reload L	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
CD	1	TH2	Timer 2 reload H	D15	D14	D13	D12	D11	D10	D9	D8	00000000	RW
CE	2	reserved											
D0	1	PSW	Program Status Word (bit addressable)	CY	AC	F0	RS1	RS0	OV	F1	P	00000000	RW
D1	7	reserved											
D8	1	EICON ^[15]	External Interrupt Control	SMOD1	1	ERESI	RESI	INT6	0	0	0	01000000	RW
D9	7	reserved											
E0	1	ACC	Accumulator (bit address- able)	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
E1	7	reserved											
E8	1	EIE ^[15]	External Interrupt En- able(s)	1	1	1	EX6	EX5	EX4	E ² C	EUSB	11100000	RW
E9	7	reserved											
F0	1	B	B (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
F1	7	reserved											
F8	1	EIP ^[15]	External Interrupt Priority Control	1	1	1	PX6	PX5	PX4	P ² C	PUSB	11100000	RW
F9	7	reserved											

R = all bits read-only
W = all bits write-only
r = read-only bit
w = write-only bit
b = both read/write bit

Data Memory Read^[21]

Figure 13. Data Memory Read Timing Diagram

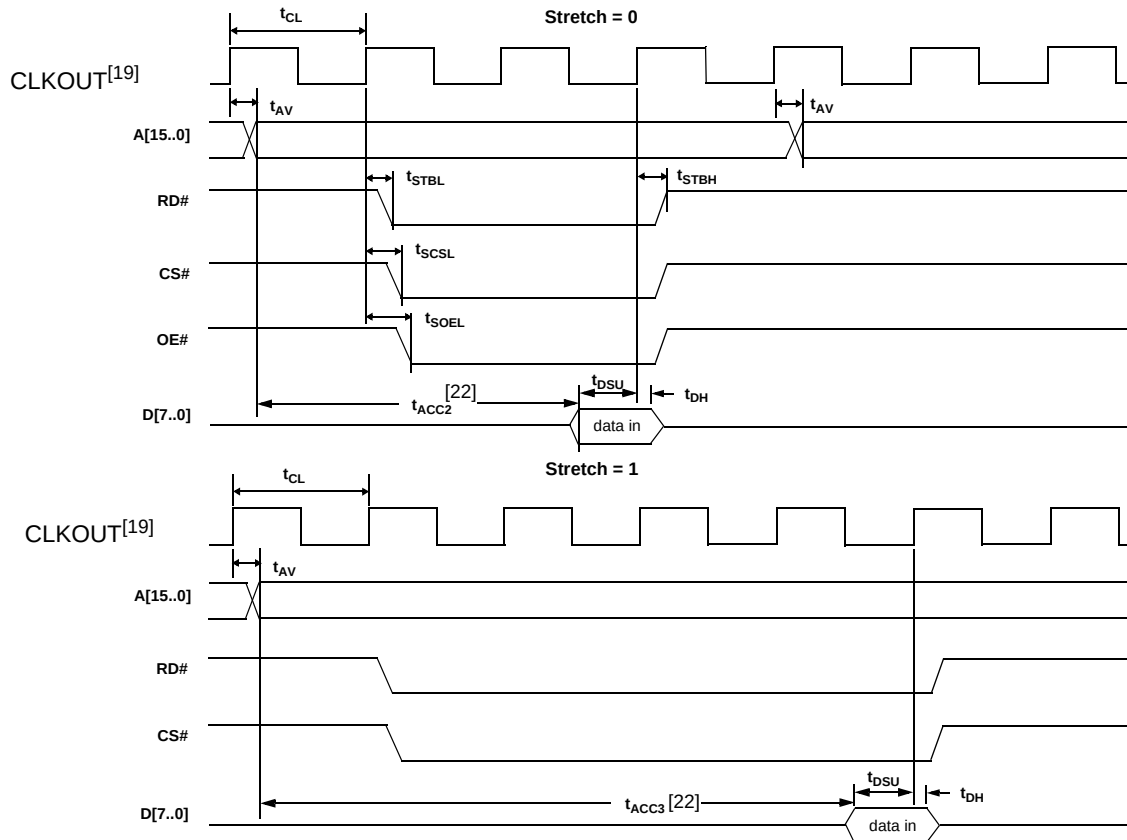


Table 16. Data Memory Read Parameters

Parameter	Description	Min	Typ	Max	Unit	Notes
t_{CL}	1/CLKOUT frequency	–	20.83	–	ns	48 MHz
		–	41.66	–	ns	24 MHz
		–	83.2	–	ns	12 MHz
t_{AV}	Delay from clock to valid address	–	–	10.7	ns	–
t_{STBL}	Clock to RD LOW	–	–	11	ns	–
t_{STBH}	Clock to RD HIGH	–	–	11	ns	–
t_{SCSL}	Clock to CS LOW	–	–	13	ns	–
t_{SOEL}	Clock to OE LOW	–	–	11.1	ns	–
t_{DSU}	Data setup to clock	9.6	–	–	ns	–
t_{DH}	Data hold time	0	–	–	ns	–

When using the AUTOPTR1 or AUTOPTR2 to address external memory, the address of AUTOPTR1 is only active while either RD# or WR# is active. The address of AUTOPTR2 is active throughout the cycle and meets the address valid time for which is based on the stretch value.

Notes

21. The stretch memory cycle feature enables EZ-USB firmware to adjust the speed of data memory accesses not the program memory accesses. Details including typical strobe width timings can be found in the section 12.1.2 of the [Technical Reference Manual](#). The address cycle width can be interpreted from these.

22. t_{ACC2} and t_{ACC3} are computed from these parameters as follows:

$$\begin{aligned}
 t_{ACC2}(24 \text{ MHz}) &= 3 \cdot t_{CL} - t_{AV} - t_{DSU} = 106 \text{ ns} \\
 t_{ACC2}(48 \text{ MHz}) &= 3 \cdot t_{CL} - t_{AV} - t_{DSU} = 43 \text{ ns} \\
 t_{ACC3}(24 \text{ MHz}) &= 5 \cdot t_{CL} - t_{AV} - t_{DSU} = 190 \text{ ns} \\
 t_{ACC3}(48 \text{ MHz}) &= 5 \cdot t_{CL} - t_{AV} - t_{DSU} = 86 \text{ ns}
 \end{aligned}$$

GPIF Synchronous Signals

Figure 18. GPIF Synchronous Signals Timing Diagram^[24]

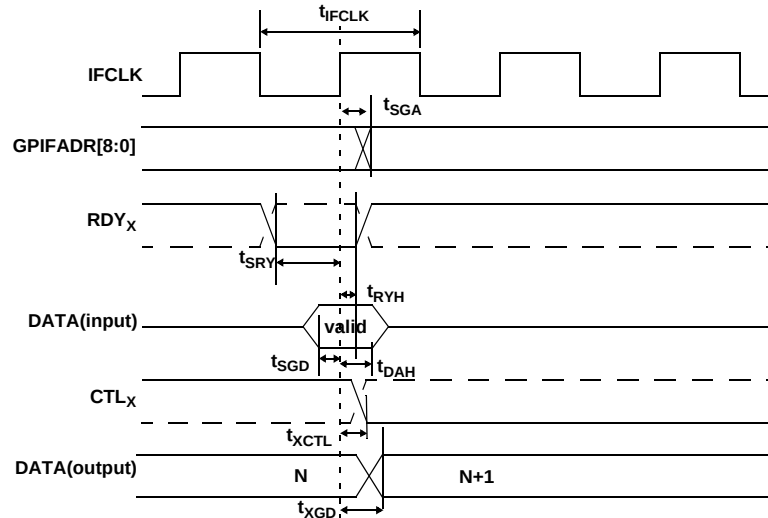


Table 18. GPIF Synchronous Signals Parameters with Internally Sourced IFCLK^[24, 25]

Parameter	Description	Min	Max	Typ		Unit
				Min	Max	
tIFCLK	IFCLK Period	20.83	—	—	—	ns
tSRY	RDY _x to clock setup time	8.9	—	—	—	ns
tRYH	Clock to RDY _x	0	—	—	—	ns
tSGD	GPIF data to clock setup time	9.2	—	—	—	ns
tDAH	GPIF data hold time	0	—	—	—	ns
tSGA	Clock to GPIF address propagation delay	—	7.5	—	—	ns
tXGD	Clock to GPIF data output propagation delay	—	11	—	—	ns
tXCTL	Clock to CTL _x output propagation delay	—	6.7	—	—	ns
tIFCLKR	IFCLK rise time	—	—	—	900	ps
tIFCLKF	IFCLK fall time	—	—	—	900	ps
tIFCLKOD	IFCLK output duty cycle	—	—	49	51	%
tIFCLKJ	IFCLK jitter peak to peak	—	—	—	300	ps

Table 19. GPIF Synchronous Signals Parameters with Externally Sourced IFCLK^[25]

Parameter	Description	Min	Max	Unit
tIFCLK	IFCLK period ^[26]	20.83	200	ns
tSRY	RDY _x to clock setup time	2.9	—	ns
tRYH	Clock to RDY _x	3.7	—	ns
tSGD	GPIF data to clock setup time	3.2	—	ns
tDAH	GPIF data hold time	4.5	—	ns
tSGA	Clock to GPIF address propagation delay	—	11.5	ns
tXGD	Clock to GPIF data output propagation delay	—	15	ns
tXCTL	Clock to CTL _x output propagation delay	—	10.7	ns

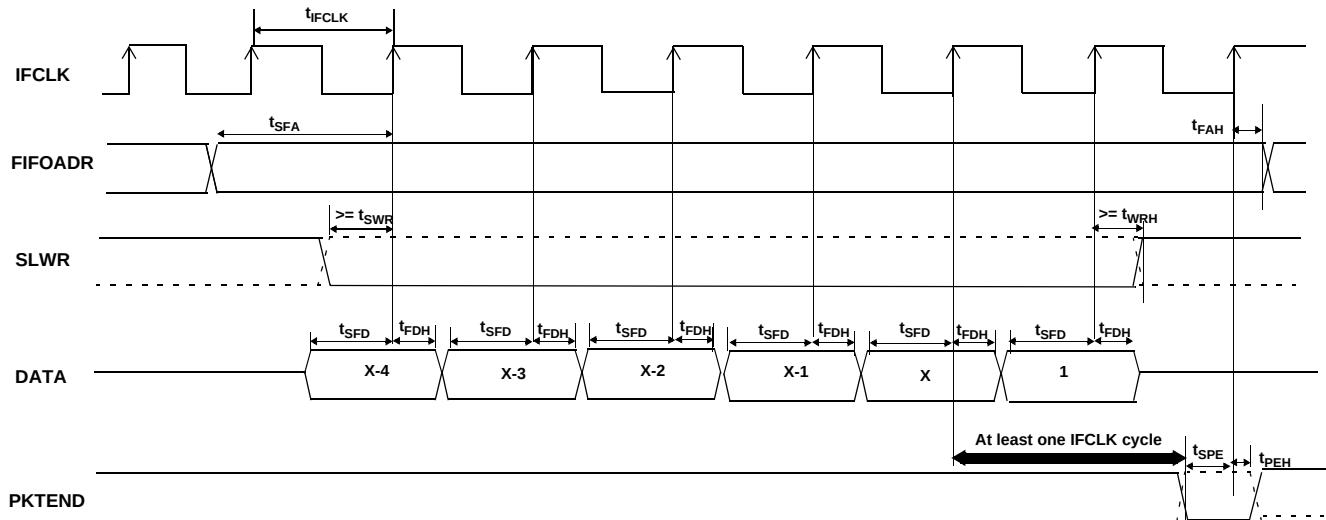
Notes

24. Dashed lines denote signals with programmable polarity.

25. GPIF asynchronous RDY_x signals have a minimum setup time of 50 ns when using the internal 48-MHz IFCLK.

26. IFCLK must not exceed 48 MHz.

Figure 24. Slave FIFO Synchronous Write Sequence and Timing Diagram^[24]



Slave FIFO Asynchronous Packet End Strobe

Figure 25. Slave FIFO Asynchronous Packet End Strobe Timing Diagram^[24]

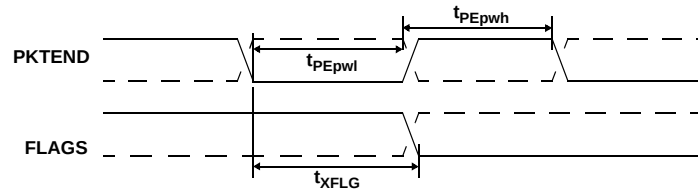


Table 28. Slave FIFO Asynchronous Packet End Strobe Parameters^[27]

Parameter	Description	Min	Max	Unit
t_{PEpwl}	PKTEND pulse width LOW	50	—	ns
t_{PEpwh}	PKTEND pulse width HIGH	50	—	ns
t_{XFLG}	PKTEND to FLAGS output propagation delay	—	115	ns

Slave FIFO Output Enable

Figure 26. Slave FIFO Output Enable Timing Diagram^[24]

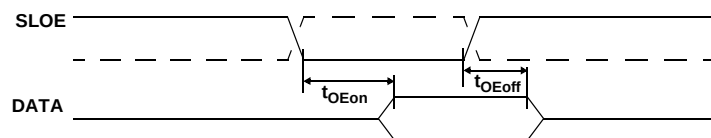


Table 29. Slave FIFO Output Enable Parameters

Parameter	Description	Min	Max	Unit
t_{OEon}	SLOE assert to FIFO DATA output		10.5	ns
t_{OEoff}	SLOE deassert to FIFO DATA hold		10.5	ns

Slave FIFO Address to Flags/Data

Figure 27. Slave FIFO Address to Flags/Data Timing Diagram^[24]

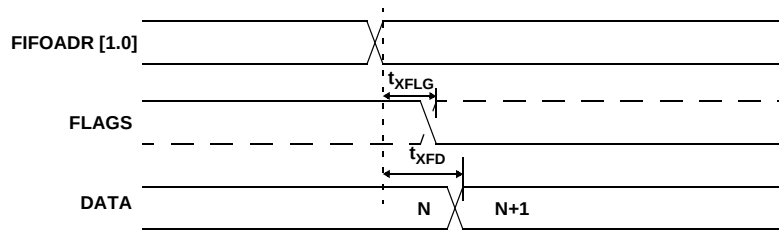


Table 30. Slave FIFO Address to Flags/Data Parameters

Parameter	Description	Min	Max	Unit
t_{XFLG}	FIFOADR[1:0] to FLAGS output propagation delay	–	10.7	ns
t_{XFD}	FIFOADR[1:0] to FIFODATA output propagation delay	–	14.3	ns

Slave FIFO Synchronous Address

Figure 28. Slave FIFO Synchronous Address Timing Diagram^[24]

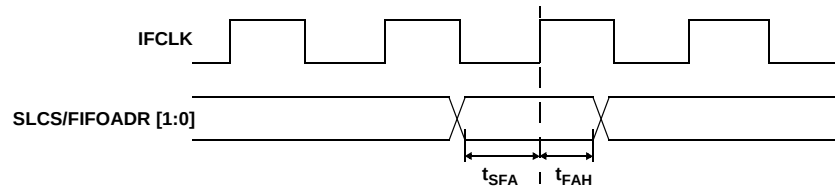


Table 31. Slave FIFO Synchronous Address Parameters^[25]

Parameter	Description	Min	Max	Unit
t_{IFCLK}	Interface clock period	20.83	200	ns
t_{SFA}	FIFOADR[1:0] to clock setup time	25	–	ns
t_{FAH}	Clock to FIFOADR[1:0] hold time	10	–	ns

Slave FIFO Asynchronous Address

Figure 29. Slave FIFO Asynchronous Address Timing Diagram^[24]

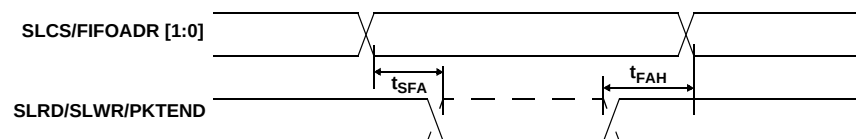


Table 32. Slave FIFO Asynchronous Address Parameters^[27]

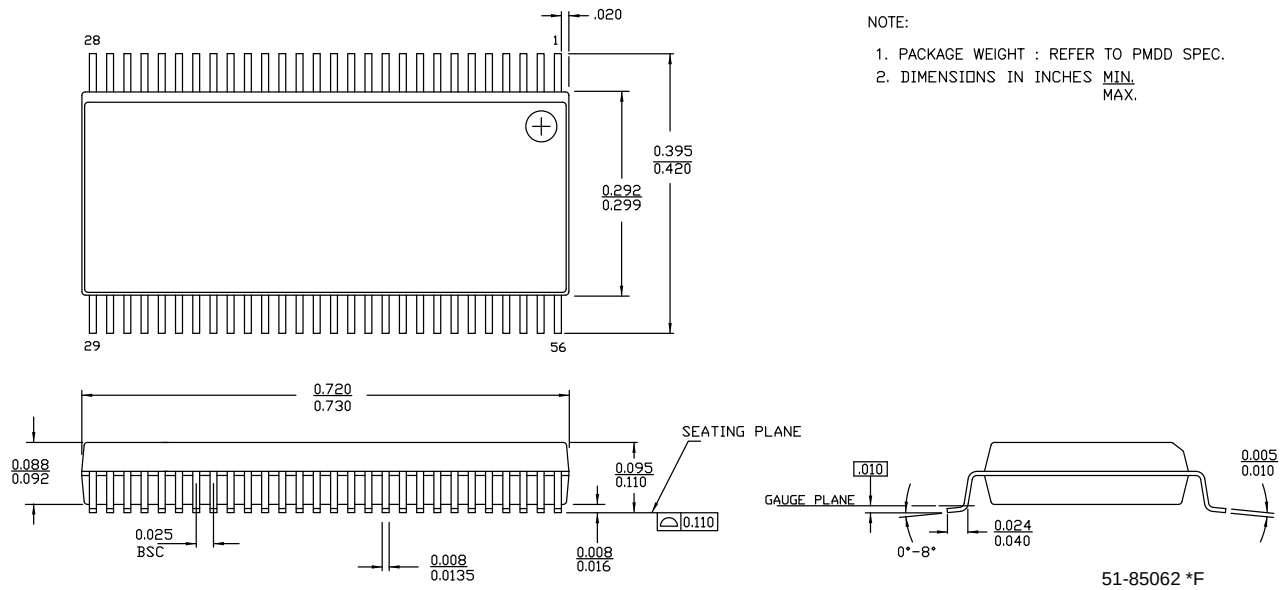
Parameter	Description	Min	Max	Unit
t_{SFA}	FIFOADR[1:0] to SLRD/SLWR/PKTEND setup time	10	–	ns
t_{FAH}	RD/WR/PKTEND to FIFOADR[1:0] hold time	10	–	ns

Package Diagrams

The FX2LP is available in five packages:

- 56-pin SSOP
- 56-pin QFN
- 100-pin TQFP
- 128-pin TQFP
- 56-ball VFBGA

Figure 36. 56-Pin Shrunk Small Outline Package O56 (51-85062)



Quad Flat Package No Leads (QFN) Package Design Notes

Electrical contact of the part to the PCB is made by soldering the leads on the bottom surface of the package to the PCB. Therefore, special attention is required to the heat transfer area below the package to provide a good thermal bond to the circuit board. Design a copper (Cu) fill in the PCB as a thermal pad under the package. Heat is transferred from the FX2LP through the device's metal paddle on the bottom side of the package. Heat from here is conducted to the PCB at the thermal pad. It is then conducted from the thermal pad to the PCB inner ground plane by a 5×5 array of via. A via is a plated-through hole in the PCB with a finished diameter of 13 mil. The QFN's metal die paddle must be soldered to the PCB's thermal pad. Solder mask is placed on the board top side over each via to resist solder flow into the via. The mask on the top side also minimizes outgassing during the solder reflow process.

For further information on this package design, refer to application notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages. You can find this on Amkor's website <http://www.amkor.com>.

This application note provides detailed information about board mounting guidelines, soldering flow, rework process, etc.

Figure 41 shows a cross-sectional area underneath the package. The cross section is of only one via. The solder paste template should be designed to allow at least 50% solder coverage. The thickness of the solder paste template should be 5 mil. Use the No Clean type 3 solder paste for mounting the part. Nitrogen purge is recommended during reflow.

Figure 42 is a plot of the solder mask pattern and Figure 43 displays an X-Ray image of the assembly (darker areas indicate solder).

Figure 41. Cross-section of the Area Underneath the QFN Package

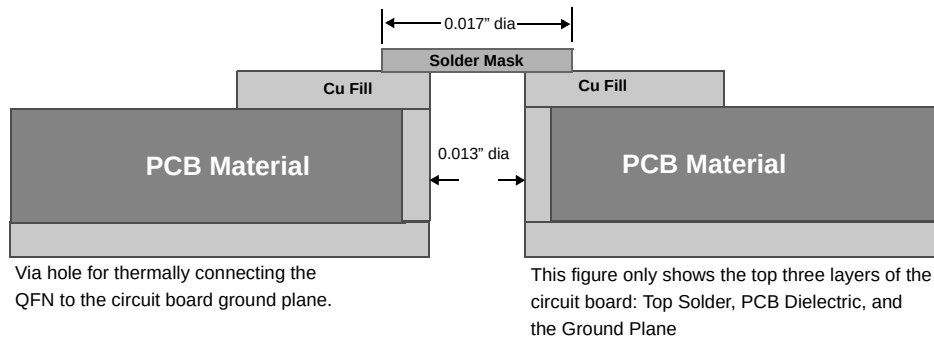


Figure 42. Plot of the Solder Mask (White Area)

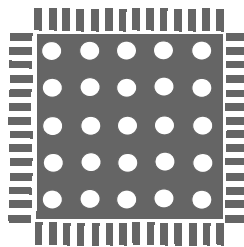
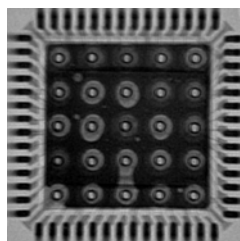


Figure 43. X-ray Image of the Assembly



Acronyms

Table 34. Acronyms Used in this Document

Acronym	Description
ASIC	application-specific integrated circuit
ATA	advanced technology attachment
DID	device identifier
DSL	digital service line
DSP	digital signal processor
ECC	error correction code
EEPROM	electrically erasable programmable read only memory
EPP	enhanced parallel port
FIFO	first in first out
GPIF	general programmable interface
GPIO	general purpose input output
I/O	input output
LAN	local area network
MPEG	moving picture experts group
PCMCIA	personal computer memory card international association
PID	product identifier
PLL	phase locked loop
QFN	quad flat no leads
RAM	random access memory
SIE	serial interface engine
SOF	start of frame
SSOP	super small outline package
TQFP	thin quad flat pack
USART	universal serial asynchronous receiver/transmitter
USB	universal serial bus
UTOPIA	universal test and operations physical-layer interface
VFBGA	very fine ball grid array
VID	vendor identifier

Document Conventions

Units of Measure

Table 35. Units of Measure

Symbol	Unit of Measure
kHz	kilohertz
mA	milliamperes
Mbps	megabits per second
MBPs	megabytes per second
MHz	megahertz
uA	microamperes
V	volts

Errata

This section describes the errata for the EZ-USB® FX2LP™ CY7C68013A/14A/15A/16A Rev. B silicon. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

Part Number	Package Type	Operating Range
CY7C68013A	All	Commercial
CY7C68014A	All	Commercial
CY7C68015A	All	Commercial
CY7C68016A	All	Commercial

CY7C68013A/14A/15A/16A Qualification Status

In production

CY7C68013A/14A/15A/16A Errata Summary

This table defines the errata for available CY7C68013A/14A/15A/16A family devices. An "X" indicates that the errata pertain to the selected device.

Items	CY7C68013A/14A/15A/16A	Silicon Revision	Fix Status
[1.]. Empty Flag Assertion	X	B	No silicon fix planned currently. Use the workaround.

1. Empty Flag Assertion

■ Problem Definition

In Slave FIFO Asynchronous Word Wide mode, if a single word data is transferred from the USB host to EP2, configured as OUT Endpoint (EP) in the first transaction, then the Empty flag behaves incorrectly. This does not happen if the data size is more than one word in the first transaction.

■ Parameters Affected

NA

■ Trigger Condition(S)

In Slave FIFO Asynchronous Word Wide Mode, after firmware boot and initialization, EP2 OUT endpoint empty flag indicates the status as 'Empty'. When data is received in EP2, the status changes to 'Not-Empty'. However, if data transferred to EP2 is a single word, then asserting SLRD with FIFOADR pointing to any other endpoint changes 'Not-Empty' status to 'Empty' for EP2 even though there is a word data (or it is untouched). This is noticed only when the single word is sent as the first transaction and not if it follows a multi-word packet as the first transaction.

■ Scope of Impact

External interface does not see data available in EP2 OUT endpoint and can end up waiting for data to be read.

■ Workaround

One of the following workarounds can be used:

- Send a pulse signal to the SLWR pin, with FIFOADR pins pointing to an endpoint other than EP2, after firmware initialization and before or after transferring the data to EP2 from the host
- Set the length of the first data to EP2 to be more than a word
- Prioritize EP2 read from the Master for multiple OUT EPs and single word write to EP2
- Write to an IN EP, if any, from the Master before reading from other OUT EPs (other than EP2) from the Master.

■ Fix Status

There is no silicon fix planned for this currently; use the workarounds provided.

Document History Page (continued)

Document Title: CY7C68013A, CY7C68014A, CY7C68015A, CY7C68016A, EZ-USB® FX2LP™ USB Microcontroller High-Speed USB Peripheral Controller Document Number: 38-08032				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*K	420505	MON	See ECN	Remove SLCS from figure in Section . Removed indications that SLRD can be asserted simultaneously with SLCS in Section and Section Added Absolute Maximum Temperature Rating for industrial packages in Section Changed number of packages stated in the description in Section to five. Added Table 13 on Thermal Coefficients for various packages
*L	2064406	CMCC/PYRS	See ECN	Changed TID number Removed T0OUT and T1OUT from CY7C68015A/16A Updated t_{SWR} Min value in Figure 21 Updated 56-lead QFN package diagram
*M	2710327	DPT	05/22/2009	Added 56-Pin QFN (8 X 8 mm) package diagram Updated ordering information for CY7C68013A-56LTXC, CY7C68013A-56LTXI, CY7C68014A-56LTXC, CY7C68015A-56LTXC, and CY7C68016A-56LTXC parts.
*N	2727334	ODC	07/01/09	Removed sentence on E-Pad size change from *F revision in the Document History Page Updated 56-Pin Sawn Package Diagram
*O	2756202	ODC	08/26/2009	Updated Ordering Information table and added note 24.
*P	2785207	ODC	10/12/2009	Added information on Pb-free parts in the Ordering information table.
*Q	2811890	ODC	11/20/2009	Updated Program I/Os for the CY7C68016A-56LTXC and CY7C68016A-56LTXCT parts in " Ordering Information " on page 56.
*R	2896281	ODC	03/19/10	Removed inactive parts from the ordering information table. Updated package diagrams. Updated links in Sales, Solutions and Legal Information.
*S	3035980	ODC	09/22/10	Updated template. Changed PPM requirement for the external crystal from +/- 10 ppm to +/- 100 ppm under Electrical specifications. Added table of contents, ordering code definitions, acronym table, and units of measure.
*T	3161410	AAE	02/03/2011	Replaced 56-Pin QFN 8 x 8 mm Punch Version Package Diagram (Figure 11.2) and 56-Pin QFN 8 x 8 mm Sawn Version Package Diagram (Figure 11.3). Updated Package Diagrams (Figure 11.4, Figure 11.5).
*U	3195232	ODC	03/14/2011	Updated table numbering. Added typical values to Table 18 on page 45 and Table 20 on page 46 based on data obtained from SHAK-63 and SHAK 69. Updated Table 13, "Thermal Characteristics," on page 39 (CDT 89510) Updated package diagram 001-03901 to *D.
*V	3512313	GAYA	02/01/2012	Removed obsolete part CY7C68014A-56BAXC Removed pruned part CY7C68016A-56LFXC Added parts CY7C68013A-56BAXCT and CY7C68013A-56PVXCT Updated Package Diagrams

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