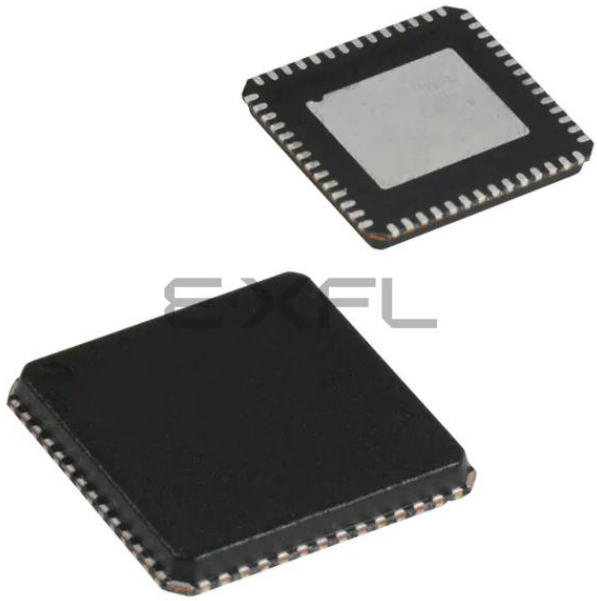

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	USB Microcontroller
Core Processor	8051
Program Memory Type	ROMless
Controller Series	CY7C680xx
RAM Size	16K x 8
Interface	I²C, USB, USART
Number of I/O	24
Voltage - Supply	3V ~ 3.6V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad
Supplier Device Package	56-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c68013a-56lfxct

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Table 4. Individual FIFO/GPIF Interrupt Sources

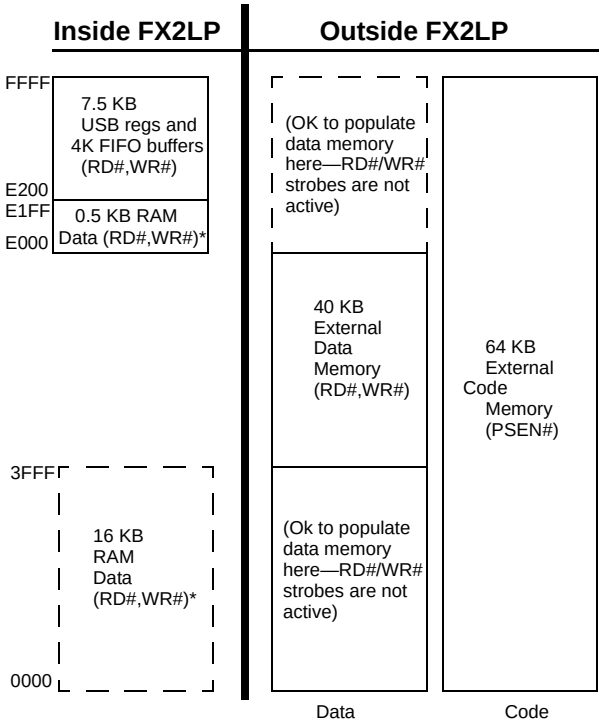
Priority	INT4VEC Value	Source	Notes
1	80	EP2PF	Endpoint 2 programmable flag
2	84	EP4PF	Endpoint 4 programmable flag
3	88	EP6PF	Endpoint 6 programmable flag
4	8C	EP8PF	Endpoint 8 programmable flag
5	90	EP2EF	Endpoint 2 empty flag [3]
6	94	EP4EF	Endpoint 4 empty flag
7	98	EP6EF	Endpoint 6 empty flag
8	9C	EP8EF	Endpoint 8 empty flag
9	A0	EP2FF	Endpoint 2 full flag
10	A4	EP4FF	Endpoint 4 full flag
11	A8	EP6FF	Endpoint 6 full flag
12	AC	EP8FF	Endpoint 8 full flag
13	B0	GPIFDONE	GPIF operation complete
14	B4	GPIFWF	GPIF waveform

If Autovectoring is enabled (AV4EN = 1 in the INTSET-UP register), the FX 2LP substitutes its INT4VEC byte. Therefore, if the high byte ("page") of a jump-table address is preloaded at location 0x0054, the automatically inserted INT4VEC byte at 0x0055 directs the jump to the correct address out of the 14 addresses within the page. When the ISR occurs, the FX2LP pushes the program counter to its stack then jumps to address 0x0053, where it expects to find a "jump" instruction to the interrupt service routine (ISR).

Note

3. Errata: In Slave FIFO Asynchronous Word Wide mode, if a single word data is transferred from the USB host to EP2, configured as OUT Endpoint (EP) in the first transaction, then the Empty flag behaves incorrectly. This does not happen if the data size is more than one word in the first transaction. For more information, see the "Errata" on page 65.

Figure 4. External Code Memory, EA = 1



*SUDPTR, USB upload/download, I^2C interface boot access

Register Addresses

FFFF F000	4 KB EP2-EP8 buffers (8 x 512)
EFFF E800	2 KB RESERVED
E7FF E7C0	64 BEP1IN
E7BF E780	64 Bytes EP1OUT
E77F E740	64 Bytes EP0 IN/OUT
E73F E700	64 Bytes RESERVED
E6FF E500	8051 Addressable Registers (512)
E4FF E480	Reserved (128)
E47F E400	128 Bytes GPIF Waveforms
E3FF E200	Reserved (512)
E1FF E000	512 Bytes 8051 xdata RAM

Endpoint RAM

Size

- 3 × 64 bytes (Endpoints 0 and 1)
- 8 × 512 bytes (Endpoints 2, 4, 6, 8)

Organization

- EP0
- Bidirectional endpoint zero, 64-byte buffer
- EP1IN, EP1OUT
- 64 byte buffers, bulk or interrupt
- EP2, 4, 6, 8
- Eight 512-byte buffers, bulk, interrupt, or isochronous. EP4 and EP8 can be double buffered; EP2 and 6 can be either double, triple, or quad buffered. For Hi-Speed endpoint configuration options, see Figure 5.

Setup Data Buffer

A separate 8-byte buffer at 0xE6B8-0xE6BF holds the setup data from a CONTROL transfer.

Endpoint Configurations (Hi-Speed Mode)

Endpoints 0 and 1 are the same for every configuration. Endpoint 0 is the only CONTROL endpoint, and endpoint 1 can be either BULK or INTERRUPT.

The endpoint buffers can be configured in any 1 of the 12 configurations shown in the vertical columns. When operating in the Full-Speed BULK mode, only the first 64 bytes of each buffer are used. For example, in Hi-Speed mode, the max packet size is 512 bytes, but in Full-Speed mode, it is 64 bytes. Even though a buffer is configured to a 512-byte buffer, in Full-Speed mode, only the first 64 bytes are used. The unused endpoint buffer space is not available for other operations. An example endpoint configuration is the EP2–1024 double-buffered; EP6–512 quad-buffered (column 8).

Figure 5. Endpoint Configuration

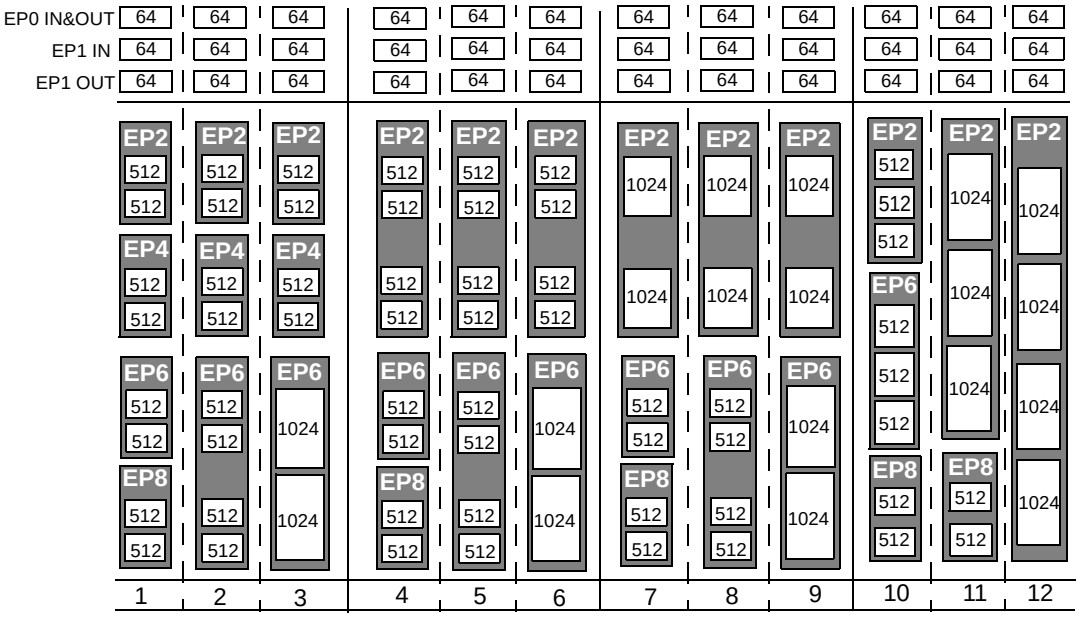
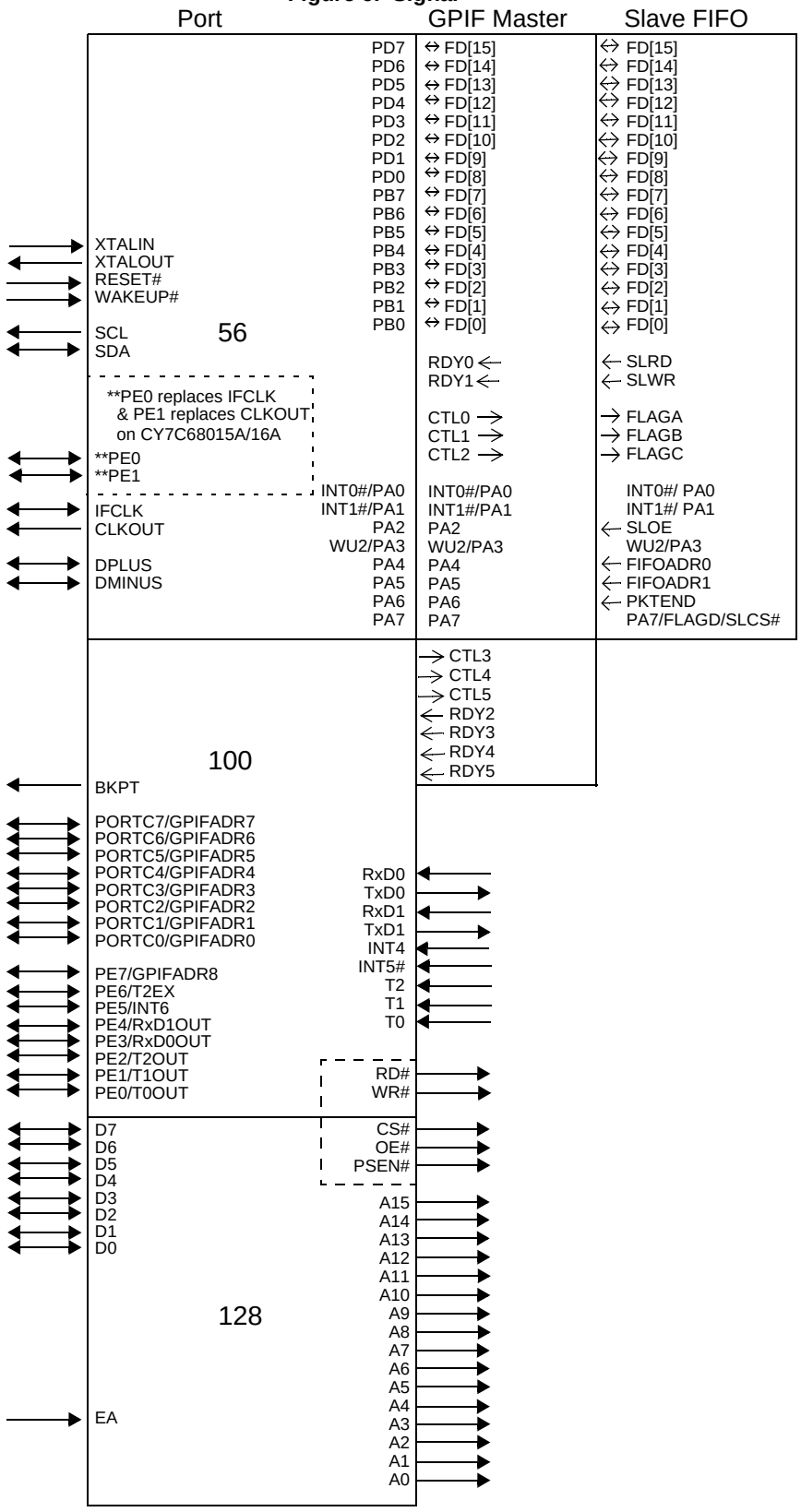


Figure 6. Signal



CY7C68013A/15A Pin Descriptions

Table 11. FX2LP Pin Descriptions[11]

128 TQFP	100 TQFP	56 SSOP	56 QFN	56 VFBGA	Name	Type	Default	Reset[12]	Description
10	9	10	3	2D	AVCC	Power	N/A	N/A	**Analog VCC**. Connect this pin to the 3.3 V power source. This signal provides power to the analog section of the chip.
17	16	14	7	1D	AVCC	Power	N/A	N/A	**Analog VCC**. Connect this pin to the 3.3 V power source. This signal provides power to the analog section of the chip.
13	12	13	6	2F	AGND	Ground	N/A	N/A	**Analog Ground**. Connect to ground with as short a path as possible.
20	19	17	10	1F	AGND	Ground	N/A	N/A	**Analog Ground**. Connect to ground with as short a path as possible.
19	18	16	9	1E	DMINUS	I/O/Z	Z	N/A	**USB D– Signal**. Connect to the USB D– signal.
18	17	15	8	2E	DPLUS	I/O/Z	Z	N/A	**USB D+ Signal**. Connect to the USB D+ signal.
94	–	–	–	–	A0	Output	L	L	**8051 Address Bus**. This bus is driven at all times. When the 8051 is addressing internal RAM it reflects the internal address.
95	–	–	–	–	A1	Output	L	L	
96	–	–	–	–	A2	Output	L	L	
97	–	–	–	–	A3	Output	L	L	
117	–	–	–	–	A4	Output	L	L	
118	–	–	–	–	A5	Output	L	L	
119	–	–	–	–	A6	Output	L	L	
120	–	–	–	–	A7	Output	L	L	
126	–	–	–	–	A8	Output	L	L	
127	–	–	–	–	A9	Output	L	L	
128	–	–	–	–	A10	Output	L	L	
21	–	–	–	–	A11	Output	L	L	
22	–	–	–	–	A12	Output	L	L	
23	–	–	–	–	A13	Output	L	L	
24	–	–	–	–	A14	Output	L	L	
25	–	–	–	–	A15	Output	L	L	
59	–	–	–	–	D0	I/O/Z	Z	Z	**8051 Data Bus**. This bidirectional bus is high impedance when inactive, input for bus reads, and output for bus writes. The data bus is used for external 8051 program and data memory. The data bus is active only for external bus accesses, and is driven LOW in suspend.
60	–	–	–	–	D1	I/O/Z	Z	Z	
61	–	–	–	–	D2	I/O/Z	Z	Z	
62	–	–	–	–	D3	I/O/Z	Z	Z	
63	–	–	–	–	D4	I/O/Z	Z	Z	
86	–	–	–	–	D5	I/O/Z	Z	Z	
87	–	–	–	–	D6	I/O/Z	Z	Z	
88	–	–	–	–	D7	I/O/Z	Z	Z	
39	–	–	–	–	PSEN#	Output	H	H	**Program Store Enable**. This active LOW signal indicates an 8051 code fetch from external memory. It is active for program memory fetches from 0x4000–0xFFFF when the EA pin is LOW, or from 0x0000–0xFFFF when the EA pin is HIGH.

Notes

11. Unused inputs must not be left floating. Tie either HIGH or LOW as appropriate. Outputs should only be pulled up or down to ensure signals at power up and in standby. Note also that no pins should be driven while the device is powered down.
12. The Reset column indicates the state of signals during reset (RESET# asserted) or during Power on Reset (POR).

Table 11. FX2LP Pin Descriptions[11] (continued)

128 TQFP	100 TQFP	56 SSOP	56 QFN	56 VFBGA	Name	Type	Default	Reset[12]	Description
34	28	–	–		BKPT	Output	L	L	**Breakpoint**. This pin goes active (HIGH) when the 8051 address bus matches the BPADDRH/L registers and breakpoints are enabled in the BREAKPT register (BPEN = 1). If the BPPULSE bit in the BREAKPT register is HIGH, this signal pulses HIGH for eight 12-/24-/48-MHz clocks. If the BPPULSE bit is LOW, the signal remains HIGH until the 8051 clears the BREAK bit (by writing 1 to it) in the BREAKPT register.
99	77	49	42	8B	RESET#	Input	N/A	N/A	**Active LOW Reset**. Resets the entire chip. See section "Reset and Wakeup" on page 9 for more details.
35	–	–	–	–	EA	Input	N/A	N/A	**External Access**. This pin determines where the 8051 fetches code between addresses 0x0000 and 0x3FFF. If EA = 0 the 8051 fetches this code from its internal RAM. IF EA = 1 the 8051 fetches this code from external memory.
12	11	12	5	1C	XTALIN	Input	N/A	N/A	**Crystal Input**. Connect this signal to a 24-MHz parallel-resonant, fundamental mode crystal and load capacitor to GND. It is also correct to drive XTALIN with an external 24-MHz square wave derived from another clock source. When driving from an external source, the driving signal should be a 3.3-V square wave.
11	10	11	4	2C	XTALOUT	Output	N/A	N/A	**Crystal Output**. Connect this signal to a 24-MHz parallel-resonant, fundamental mode crystal and load capacitor to GND. If an external clock is used to drive XTALIN, leave this pin open.
1	100	5	54	2B	CLKOUT on CY7C68013A and CY7C68014A ---------- PE1 on CY7C68015A and CY7C68016A	O/Z ---------- I/O/Z	12 MHz ---------- I	Clock Driven ---------- Z	**CLKOUT:** 12-, 24- or 48-MHz clock, phase-locked to the 24-MHz input clock. The 8051 defaults to 12-MHz operation. The 8051 may three-state this output by setting CPUCS.1 = 1. ---------- ------**PE1** is a bidirectional I/O port pin.
Port A									
82	67	40	33	8G	PA0 or INT0#	I/O/Z	I (PA0)	Z (PA0)	Multiplexed pin whose function is selected by PORTACFG.0 **PA0** is a bidirectional I/O port pin. **INT0#** is the active-LOW 8051 INT0 interrupt input signal, which is either edge-triggered (IT0 = 1) or level-triggered (IT0 = 0).
83	68	41	34	6G	PA1 or INT1#	I/O/Z	I (PA1)	Z (PA1)	Multiplexed pin whose function is selected by: PORTACFG.1 **PA1** is a bidirectional I/O port pin. **INT1#** is the active-LOW 8051 INT1 interrupt input signal, which is either edge-triggered (IT1 = 1) or level-triggered (IT1 = 0).

Table 11. FX2LP Pin Descriptions[11] (continued)

128 TQFP	100 TQFP	56 SSOP	56 QFN	56 VFBGA	Name	Type	Default	Reset[12]	Description
47	37	28	21	4G	PB3 or FD[3]	I/O/Z	I (PB3)	Z (PB3)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB3** is a bidirectional I/O port pin. **FD[3]** is the bidirectional FIFO/GPIF data bus.
54	44	29	22	5H	PB4 or FD[4]	I/O/Z	I (PB4)	Z (PB4)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB4** is a bidirectional I/O port pin. **FD[4]** is the bidirectional FIFO/GPIF data bus.
55	45	30	23	5G	PB5 or FD[5]	I/O/Z	I (PB5)	Z (PB5)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB5** is a bidirectional I/O port pin. **FD[5]** is the bidirectional FIFO/GPIF data bus.
56	46	31	24	5F	PB6 or FD[6]	I/O/Z	I (PB6)	Z (PB6)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB6** is a bidirectional I/O port pin. **FD[6]** is the bidirectional FIFO/GPIF data bus.
57	47	32	25	6H	PB7 or FD[7]	I/O/Z	I (PB7)	Z (PB7)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB7** is a bidirectional I/O port pin. **FD[7]** is the bidirectional FIFO/GPIF data bus.
PORT C									
72	57	–	–	–	PC0 or GPIFADR0	I/O/Z	I (PC0)	Z (PC0)	Multiplexed pin whose function is selected by PORTCCFG.0 **PC0** is a bidirectional I/O port pin. **GPIFADR0** is a GPIF address output pin.
73	58	–	–	–	PC1 or GPIFADR1	I/O/Z	I (PC1)	Z (PC1)	Multiplexed pin whose function is selected by PORTCCFG.1 **PC1** is a bidirectional I/O port pin. **GPIFADR1** is a GPIF address output pin.
74	59	–	–	–	PC2 or GPIFADR2	I/O/Z	I (PC2)	Z (PC2)	Multiplexed pin whose function is selected by PORTCCFG.2 **PC2** is a bidirectional I/O port pin. **GPIFADR2** is a GPIF address output pin.
75	60	–	–	–	PC3 or GPIFADR3	I/O/Z	I (PC3)	Z (PC3)	Multiplexed pin whose function is selected by PORTCCFG.3 **PC3** is a bidirectional I/O port pin. **GPIFADR3** is a GPIF address output pin.
76	61	–	–	–	PC4 or GPIFADR4	I/O/Z	I (PC4)	Z (PC4)	Multiplexed pin whose function is selected by PORTCCFG.4 **PC4** is a bidirectional I/O port pin. **GPIFADR4** is a GPIF address output pin.
77	62	–	–	–	PC5 or GPIFADR5	I/O/Z	I (PC5)	Z (PC5)	Multiplexed pin whose function is selected by PORTCCFG.5 **PC5** is a bidirectional I/O port pin. **GPIFADR5** is a GPIF address output pin.
78	63	–	–	–	PC6 or GPIFADR6	I/O/Z	I (PC6)	Z (PC6)	Multiplexed pin whose function is selected by PORTCCFG.6 **PC6** is a bidirectional I/O port pin. **GPIFADR6** is a GPIF address output pin.
79	64	–	–	–	PC7 or GPIFADR7	I/O/Z	I (PC7)	Z (PC7)	Multiplexed pin whose function is selected by PORTCCFG.7 **PC7** is a bidirectional I/O port pin. **GPIFADR7** is a GPIF address output pin.

Table 11. FX2LP Pin Descriptions[11] (continued)

128 TQFP	100 TQFP	56 SSOP	56 QFN	56 VFBGA	Name	Type	Default	Reset[12]	Description
PORT D									
102	80	52	45	8A	PD0 or FD[8]	I/O/Z	I (PD0)	Z (PD0)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[8]** is the bidirectional FIFO/GPIF data bus.
103	81	53	46	7A	PD1 or FD[9]	I/O/Z	I (PD1)	Z (PD1)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[9]** is the bidirectional FIFO/GPIF data bus.
104	82	54	47	6B	PD2 or FD[10]	I/O/Z	I (PD2)	Z (PD2)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[10]** is the bidirectional FIFO/GPIF data bus.
105	83	55	48	6A	PD3 or FD[11]	I/O/Z	I (PD3)	Z (PD3)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[11]** is the bidirectional FIFO/GPIF data bus.
121	95	56	49	3B	PD4 or FD[12]	I/O/Z	I (PD4)	Z (PD4)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[12]** is the bidirectional FIFO/GPIF data bus.
122	96	1	50	3A	PD5 or FD[13]	I/O/Z	I (PD5)	Z (PD5)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[13]** is the bidirectional FIFO/GPIF data bus.
123	97	2	51	3C	PD6 or FD[14]	I/O/Z	I (PD6)	Z (PD6)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[14]** is the bidirectional FIFO/GPIF data bus.
124	98	3	52	2A	PD7 or FD[15]	I/O/Z	I (PD7)	Z (PD7)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[15]** is the bidirectional FIFO/GPIF data bus.
Port E									
108	86	–	–	–	PE0 or T0OUT	I/O/Z	I (PE0)	Z (PE0)	Multiplexed pin whose function is selected by the PORTECFG.0 bit. **PE0** is a bidirectional I/O port pin. **T0OUT** is an active-HIGH signal from 8051 Timer-counter0. T0OUT outputs a high level for one CLKOUT clock cycle when Timer0 overflows. If Timer0 is operated in Mode 3 (two separate timer/counters), T0OUT is active when the low byte timer/counter overflows.
109	87	–	–	–	PE1 or T1OUT	I/O/Z	I (PE1)	Z (PE1)	Multiplexed pin whose function is selected by the PORTECFG.1 bit. **PE1** is a bidirectional I/O port pin. **T1OUT** is an active HIGH signal from 8051 Timer-counter1. T1OUT outputs a high level for one CLKOUT clock cycle when Timer1 overflows. If Timer1 is operated in Mode 3 (two separate timer/counters), T1OUT is active when the low byte timer/counter overflows.

Table 12. FX2LP Register Summary (continued)

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
E62B	1	ECC1B1	ECC1 Byte 1 Address	LINE7	LINE6	LINE5	LINE4	LINE3	LINE2	LINE1	LINE0	00000000	R
E62C	1	ECC1B2	ECC1 Byte 2 Address	COL5	COL4	COL3	COL2	COL1	COL0	LINE17	LINE16	00000000	R
E62D	1	ECC2B0	ECC2 Byte 0 Address	LINE15	LINE14	LINE13	LINE12	LINE11	LINE10	LINE9	LINE8	00000000	R
E62E	1	ECC2B1	ECC2 Byte 1 Address	LINE7	LINE6	LINE5	LINE4	LINE3	LINE2	LINE1	LINE0	00000000	R
E62F	1	ECC2B2	ECC2 Byte 2 Address	COL5	COL4	COL3	COL2	COL1	COL0	0	0	00000000	R
E630 H.S.	1	EP2FIFOPFH[13]	Endpoint 2 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	IN:PKTS[2] OUT:PFC12	IN:PKTS[1] OUT:PFC11	IN:PKTS[0] OUT:PFC10	0	PFC9	PFC8	10001000	bbbbbrbb
E630 F.S.	1	EP2FIFOPFH[13]	Endpoint 2 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	OUT:PFC12	OUT:PFC11	OUT:PFC10	0	PFC9	IN:PKTS[2] OUT:PFC8	10001000	bbbbbrbb
E631 H.S.	1	EP2FIFOPFL[13]	Endpoint 2 / slave FIFO Programmable Flag L	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E631 F.S	1	EP2FIFOPFL[13]	Endpoint 2 / slave FIFO Programmable Flag L	IN:PKTS[1] OUT:PFC7	IN:PKTS[0] OUT:PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E632 H.S.	1	EP4FIFOPFH[13]	Endpoint 4 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	0	IN: PKTS[1] OUT:PFC10	IN: PKTS[0] OUT:PFC9	0	0	PFC8	10001000	bbrbbrrb
E632 F.S	1	EP4FIFOPFH[13]	Endpoint 4 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	0	OUT:PFC10	OUT:PFC9	0	0	PFC8	10001000	bbrbbrrb
E633 H.S.	1	EP4FIFOPFL[13]	Endpoint 4 / slave FIFO Programmable Flag L	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E633 F.S	1	EP4FIFOPFL[13]	Endpoint 4 / slave FIFO Programmable Flag L	IN: PKTS[1] OUT:PFC7	IN: PKTS[0] OUT:PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E634 H.S.	1	EP6FIFOPFH[13]	Endpoint 6 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	IN:PKTS[2] OUT:PFC12	IN:PKTS[1] OUT:PFC11	IN:PKTS[0] OUT:PFC10	0	PFC9	PFC8	00001000	bbbbbrbb
E634 F.S	1	EP6FIFOPFH[13]	Endpoint 6 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	OUT:PFC12	OUT:PFC11	OUT:PFC10	0	PFC9	IN:PKTS[2] OUT:PFC8	00001000	bbbbbrbb
E635 H.S.	1	EP6FIFOPFL[13]	Endpoint 6 / slave FIFO Programmable Flag L	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E635 F.S	1	EP6FIFOPFL[13]	Endpoint 6 / slave FIFO Programmable Flag L	IN:PKTS[1] OUT:PFC7	IN:PKTS[0] OUT:PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E636 H.S.	1	EP8FIFOPFH[13]	Endpoint 8 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	0	IN: PKTS[1] OUT:PFC10	IN: PKTS[0] OUT:PFC9	0	0	PFC8	00001000	bbrbbrrb
E636 F.S	1	EP8FIFOPFH[13]	Endpoint 8 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	0	OUT:PFC10	OUT:PFC9	0	0	PFC8	00001000	bbrbbrrb
E637 H.S.	1	EP8FIFOPFL[13]	Endpoint 8 / slave FIFO Programmable Flag L	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E637 F.S	1	EP8FIFOPFL[13]	Endpoint 8 / slave FIFO Programmable Flag L	IN: PKTS[1] OUT:PFC7	IN: PKTS[0] OUT:PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
	8	reserved											
E640	1	EP2ISOINPKTS	EP2 (if ISO) IN Packets per frame (1-3)	AADJ	0	0	0	0	0	INPPF1	INPPF0	00000001	brrrrrbb
E641	1	EP4ISOINPKTS	EP4 (if ISO) IN Packets per frame (1-3)	AADJ	0	0	0	0	0	INPPF1	INPPF0	00000001	brrrrrrr
E642	1	EP6ISOINPKTS	EP6 (if ISO) IN Packets per frame (1-3)	AADJ	0	0	0	0	0	INPPF1	INPPF0	00000001	brrrrrbb
E643	1	EP8ISOINPKTS	EP8 (if ISO) IN Packets per frame (1-3)	AADJ	0	0	0	0	0	INPPF1	INPPF0	00000001	brrrrrrr
E644	4	reserved											
E648	1	INPKTEND[13]	Force IN Packet End	Skip	0	0	0	EP3	EP2	EP1	EP0	xxxxxxxx	W
E649	7	OUTPKTEND[13]	Force OUT Packet End	Skip	0	0	0	EP3	EP2	EP1	EP0	xxxxxxxx	W
		INTERRUPTS											
E650	1	EP2FIFOIE[13]	Endpoint 2 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGEPF	PF	EF	FF	00000000	RW
E651	1	EP2FIFOIRQ[13,14]	Endpoint 2 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000000	rrrrrbbb
E652	1	EP4FIFOIE[13]	Endpoint 4 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGEPF	PF	EF	FF	00000000	RW
E653	1	EP4FIFOIRQ[13,14]	Endpoint 4 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000000	rrrrrbbb
E654	1	EP6FIFOIE[13]	Endpoint 6 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGEPF	PF	EF	FF	00000000	RW
E655	1	EP6FIFOIRQ[13,14]	Endpoint 6 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000000	rrrrrbbb
E656	1	EP8FIFOIE[13]	Endpoint 8 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGEPF	PF	EF	FF	00000000	RW
E657	1	EP8FIFOIRQ[13,14]	Endpoint 8 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000000	rrrrrbbb
E658	1	IBNIE	IN-BULK-NAK Interrupt Enable	0	0	EP8	EP6	EP4	EP2	EP1	EP0	00000000	RW
E659	1	IBNIRQ[14]	IN-BULK-NAK interrupt Request	0	0	EP8	EP6	EP4	EP2	EP1	EP0	00xxxxxx	rrbbbbbb
E65A	1	NAKIE	Endpoint Ping-NAK / IBN Interrupt Enable	EP8	EP6	EP4	EP2	EP1	EP0	0	IBN	00000000	RW
E65B	1	NAKIRQ[14]	Endpoint Ping-NAK / IBN Interrupt Request	EP8	EP6	EP4	EP2	EP1	EP0	0	IBN	xxxxxx0x	bbbbbbrb
E65C	1	USBIE	USB Int Enables	0	EP0ACK	HSGRANT	URES	SUSP	SUTOK	SOF	SUDAV	00000000	RW

Note
14. The register can only be reset; it cannot be set.

Table 12. FX2LP Register Summary (continued)

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
BE	1	GPIFSGLDATLX[15]	GPIF Data L w/ Trigger	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
BF	1	GPIFSGLDATL-NOX[15]	GPIF Data L w/ No Trigger	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	R
C0	1	SCON1[15]	Serial Port 1 Control (bit addressable)	SM0_1	SM1_1	SM2_1	REN_1	TB8_1	RB8_1	TI_1	RI_1	00000000	RW
C1	1	SBUF1[15]	Serial Port 1 Data Buffer	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
C2	6	reserved											
C8	1	T2CON	Timer/Counter 2 Control (bit addressable)	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	CT2	CPRL2	00000000	RW
C9	1	reserved											
CA	1	RCAP2L	Capture for Timer 2, auto-reload, up-counter	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
CB	1	RCAP2H	Capture for Timer 2, auto-reload, up-counter	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
CC	1	TL2	Timer 2 reload L	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
CD	1	TH2	Timer 2 reload H	D15	D14	D13	D12	D11	D10	D9	D8	00000000	RW
CE	2	reserved											
D0	1	PSW	Program Status Word (bit addressable)	CY	AC	F0	RS1	RS0	OV	F1	P	00000000	RW
D1	7	reserved											
D8	1	EICON[15]	External Interrupt Control	SMOD1	1	ERESI	RESI	INT6	0	0	0	01000000	RW
D9	7	reserved											
E0	1	ACC	Accumulator (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
E1	7	reserved											
E8	1	EIE[15]	External Interrupt Enable(s)	1	1	1	EX6	EX5	EX4	EI²C	EUSB	11100000	RW
E9	7	reserved											
F0	1	B	B (bit addressable)	D7	D6	D5	D4	D3	D2	D1	D0	00000000	RW
F1	7	reserved											
F8	1	EIP[15]	External Interrupt Priority Control	1	1	1	PX6	PX5	PX4	PI²C	PUSB	11100000	RW
F9	7	reserved											

R = all bits read-only
W = all bits write-only
r = read-only bit
w = write-only bit
b = both read/write bit

Data Memory Read[21]

Figure 13. Data Memory Read Timing Diagram

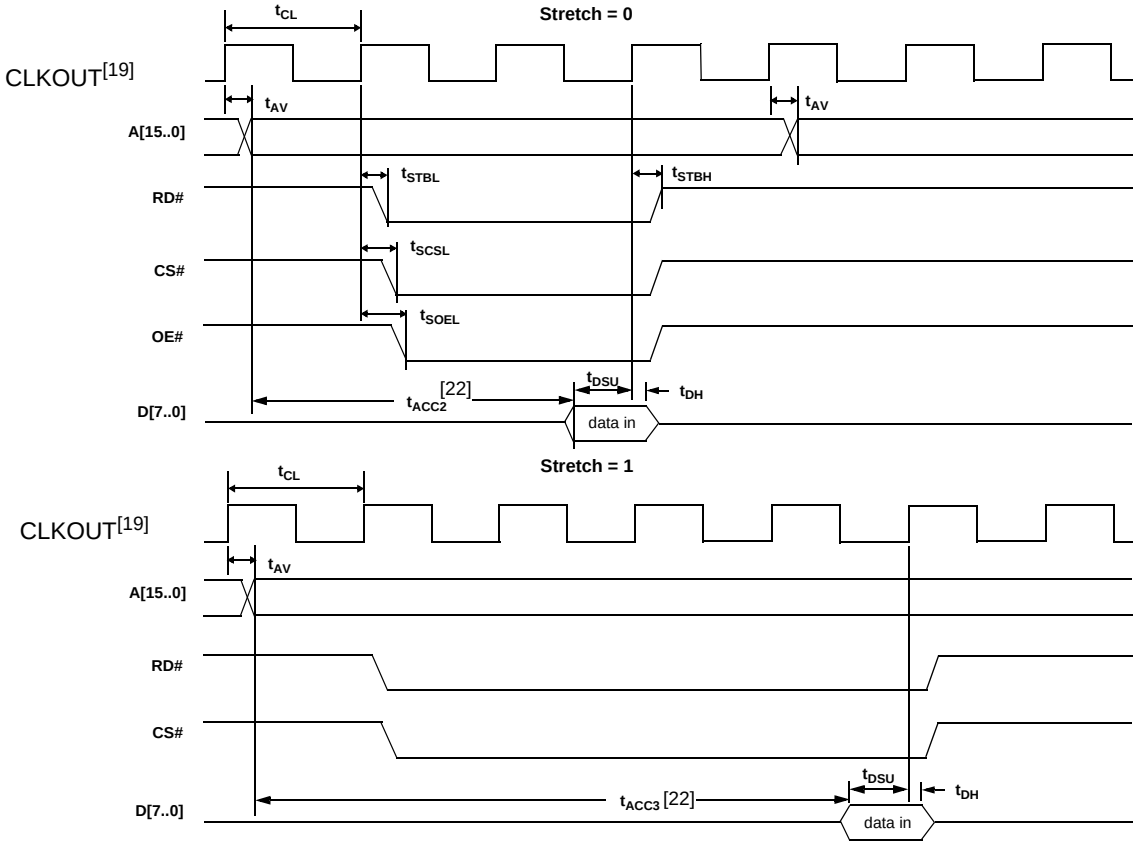


Table 16. Data Memory Read Parameters

Parameter	Description	Min	Typ	Max	Unit	Notes
t_{CL}	1/CLKOUT frequency	–	20.83	–	ns	48 MHz
		–	41.66	–	ns	24 MHz
		–	83.2	–	ns	12 MHz
t_{AV}	Delay from clock to valid address	–	–	10.7	ns	–
t_{STBL}	Clock to RD LOW	–	–	11	ns	–
t_{STBH}	Clock to RD HIGH	–	–	11	ns	–
t_{SCSL}	Clock to CS LOW	–	–	13	ns	–
t_{SOEL}	Clock to OE LOW	–	–	11.1	ns	–
t_{DSU}	Data setup to clock	9.6	–	–	ns	–
t_{DH}	Data hold time	0	–	–	ns	–

When using the AUTPOPTR1 or AUTOPTR2 to address external memory, the address of AUTOPTR1 is only active while either RD# or WR# is active. The address of AUTOPTR2 is active throughout the cycle and meets the address valid time for which is based on the stretch value.

Notes

21. The stretch memory cycle feature enables EZ-USB firmware to adjust the speed of data memory accesses not the program memory accesses. Details including typical strobe width timings can be found in the section 12.1.2 of the Technical Reference Manual. The address cycle width can be interpreted from these.
22. t_{ACC2} and t_{ACC3} are computed from these parameters as follows:
t_{ACC2}(24 MHz) = $3*t_{CL} – t_{AV} – t_{DSU}$ = 106 ns
t_{ACC2}(48 MHz) = $3*t_{CL} – t_{AV} – t_{DSU}$ = 43 ns
t_{ACC3}(24 MHz) = $5*t_{CL} – t_{AV} – t_{DSU}$ = 190 ns
t_{ACC3}(48 MHz) = $5*t_{CL} – t_{AV} – t_{DSU}$ = 86 ns

Slave FIFO Synchronous Read

Figure 19. Slave FIFO Synchronous Read Timing Diagram[24]

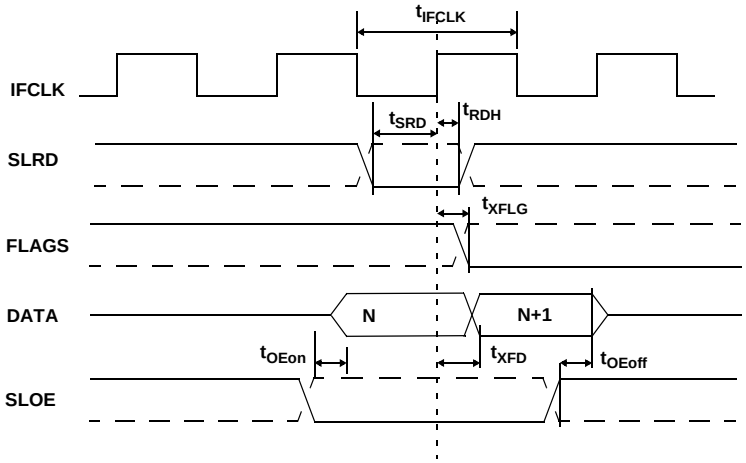


Table 20. Slave FIFO Synchronous Read Parameters with Internally Sourced IFCLK[25]

Parameter	Description	Min	Max	Typ		Unit
				Min	Max	
t_{IFCLK}	IFCLK period	20.83	–	–	–	ns
t_{SRD}	SLRD to clock setup time	18.7	–	–	–	ns
t_{RDH}	Clock to SLRD hold time	0	–	–	–	ns
t_{OEon}	SLOE turn on to FIFO data valid	–	10.5	–	–	ns
t_{OEoff}	SLOE turn off to FIFO data hold	–	10.5	–	–	ns
t_{XFLG}	Clock to FLAGS output propagation delay	–	9.5	–	–	ns
t_{XFD}	Clock to FIFO data output propagation delay	–	11	–	–	ns
t_{IFCLKR}	IFCLK rise time	–	–	–	900	ps
t_{IFCLKF}	IFCLK fall time	–	–	–	900	ps
$t_{IFCLKOD}$	IFCLK output duty cycle	–	–	49	51	%
t_{IFCLKJ}	IFCLK jitter peak to peak	–	–	–	300	ps

Table 21. Slave FIFO Synchronous Read Parameters with Externally Sourced IFCLK[25]

Parameter	Description	Min	Max	Unit
t_{IFCLK}	IFCLK period	20.83	200	ns
t_{SRD}	SLRD to clock setup time	12.7	–	ns
t_{RDH}	Clock to SLRD hold time	3.7	–	ns
t_{OEon}	SLOE turn on to FIFO data valid	–	10.5	ns
t_{OEoff}	SLOE turn off to FIFO data hold	–	10.5	ns
t_{XFLG}	Clock to FLAGS output propagation delay	–	13.5	ns
t_{XFD}	Clock to FIFO data output propagation delay	–	15	ns

Slave FIFO Asynchronous Read

Figure 20. Slave FIFO Asynchronous Read Timing Diagram[24]

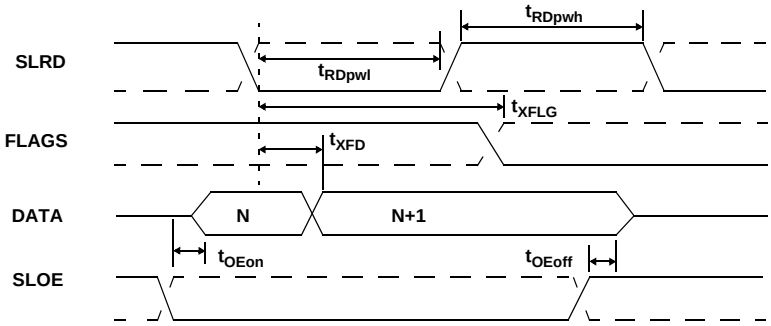


Table 22. Slave FIFO Asynchronous Read Parameters[27]

Parameter	Description	Min	Max	Unit
t_{RDpwl}	SLRD pulse width LOW	50	–	ns
t_{RDpwh}	SLRD pulse width HIGH	50	–	ns
t_{XFLG}	SLRD to FLAGS output propagation delay	–	70	ns
t_{XFD}	SLRD to FIFO data output propagation delay	–	15	ns
t_{OEon}	SLOE turn-on to FIFO data valid	–	10.5	ns
t_{OEoff}	SLOE turn-off to FIFO data hold	–	10.5	ns

Note
27. Slave FIFO asynchronous parameter values use internal IFCLK setting at 48 MHz.

Slave FIFO Address to Flags/Data

Figure 27. Slave FIFO Address to Flags/Data Timing Diagram[24]

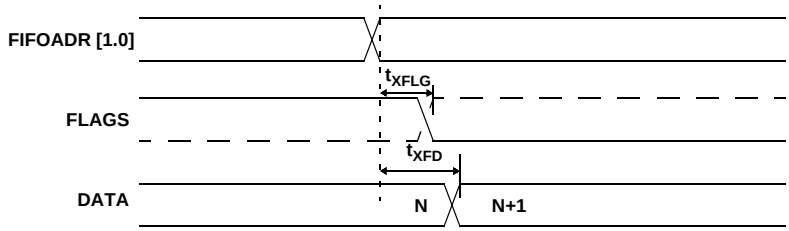


Table 30. Slave FIFO Address to Flags/Data Parameters

Parameter	Description	Min	Max	Unit
t_{XFLG}	FIFOADR[1:0] to FLAGS output propagation delay	–	10.7	ns
t_{XFD}	FIFOADR[1:0] to FIFODATA output propagation delay	–	14.3	ns

Slave FIFO Synchronous Address

Figure 28. Slave FIFO Synchronous Address Timing Diagram[24]

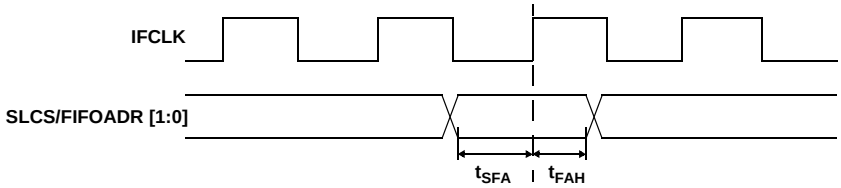


Table 31. Slave FIFO Synchronous Address Parameters[25]

Parameter	Description	Min	Max	Unit
t_{IFCLK}	Interface clock period	20.83	200	ns
t_{SFA}	FIFOADR[1:0] to clock setup time	25	–	ns
t_{FAH}	Clock to FIFOADR[1:0] hold time	10	–	ns

Slave FIFO Asynchronous Address

Figure 29. Slave FIFO Asynchronous Address Timing Diagram[24]

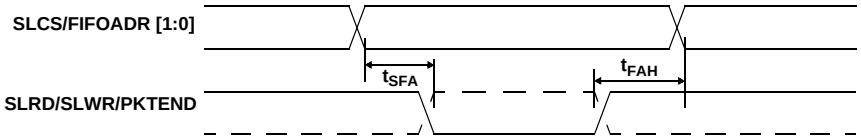
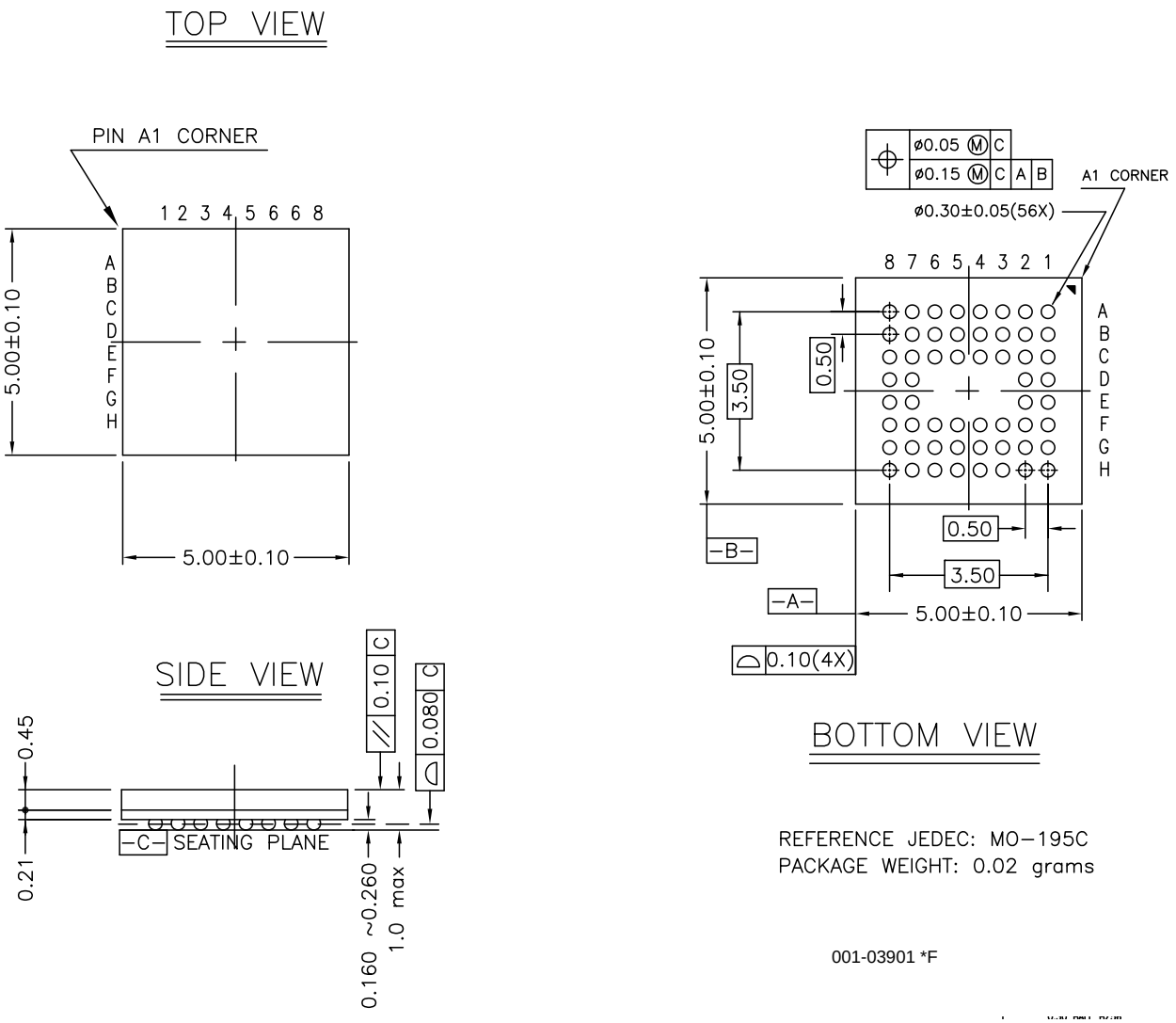


Table 32. Slave FIFO Asynchronous Address Parameters[27]

Parameter	Description	Min	Max	Unit
t_{SFA}	FIFOADR[1:0] to SLRD/SLWR/PKTEND setup time	10	–	ns
t_{FAH}	RD/WR/PKTEND to FIFOADR[1:0] hold time	10	–	ns

Figure 40. 56-Pin VFBGA (5 × 5 × 1.0 mm) 0.50 Pitch, 0.30 Ball BZ56 (001-03901)



PCB Layout Recommendations

Follow these recommendations to ensure reliable high performance operation:[29]

- Four-layer, impedance-controlled boards are required to maintain signal quality.
- Specify impedance targets (ask your board vendor what they can achieve).
- To control impedance, maintain trace widths and trace spacing.
- Minimize stubs to minimize reflected signals.
- Connections between the USB connector shell and signal ground must be near the USB connector.
- Bypass and flyback caps on VBUS, near connector, are recommended.
- DPLUS and DMINUS trace lengths should be kept to within 2 mm of each other in length, with preferred length of 20 to 30 mm.
- Maintain a solid ground plane under the DPLUS and DMINUS traces. Do not allow the plane to split under these traces.
- Do not place vias on the DPLUS or DMINUS trace routing.
- Isolate the DPLUS and DMINUS traces from all other signal traces by no less than 10 mm.

Note

29. Source for recommendations: *EZ-USB FX2™PCB Design Recommendations*, http://www.cypress.com and *High Speed USB Platform Design Guidelines*, http://www.usb.org/developers/docs/hs_usb_pdg_r1_0.pdf.

Acronyms

Table 34. Acronyms Used in this Document

Acronym	Description
ASIC	application-specific integrated circuit
ATA	advanced technology attachment
DID	device identifier
DSL	digital service line
DSP	digital signal processor
ECC	error correction code
EEPROM	electrically erasable programmable read only memory
EPP	enhanced parallel port
FIFO	first in first out
GPIF	general programmable interface
GPIO	general purpose input output
I/O	input output
LAN	local area network
MPEG	moving picture experts group
PCMCIA	personal computer memory card international association
PID	product identifier
PLL	phase locked loop
QFN	quad flat no leads
RAM	random access memory
SIE	serial interface engine
SOF	start of frame
SSOP	super small outline package
TQFP	thin quad flat pack
USART	universal serial asynchronous receiver/transmitter
USB	universal serial bus
UTOPIA	universal test and operations physical-layer interface
VFBGA	very fine ball grid array
VID	vendor identifier

Document Conventions

Units of Measure

Table 35. Units of Measure

Symbol	Unit of Measure
kHz	kilohertz
mA	milliamperes
Mbps	megabits per second
MBPs	megabytes per second
MHz	megahertz
uA	microamperes
V	volts

Document History Page (continued)

Document Title: CY7C68013A, CY7C68014A, CY7C68015A, CY7C68016A, EZ-USB® FX2LP™ USB Microcontroller High-Speed USB Peripheral Controller Document Number: 38-08032				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*K	420505	MON	See ECN	Remove SLCS from figure in Section . Removed indications that SLRD can be asserted simultaneously with SLCS in Section and Section Added Absolute Maximum Temperature Rating for industrial packages in Section Changed number of packages stated in the description in Section to five. Added Table 13 on Thermal Coefficients for various packages
*L	2064406	CMCC/PYRS	See ECN	Changed TID number Removed T0OUT and T1OUT from CY7C68015A/16A Updated t_{SWR} Min value in Figure 21 Updated 56-lead QFN package diagram
*M	2710327	DPT	05/22/2009	Added 56-Pin QFN (8 X 8 mm) package diagram Updated ordering information for CY7C68013A-56LTXC, CY7C68013A-56LTXI, CY7C68014A-56LTXC, CY7C68015A-56LTXC, and CY7C68016A-56LTXC parts.
*N	2727334	ODC	07/01/09	Removed sentence on E-Pad size change from *F revision in the Document History Page Updated 56-Pin Sawn Package Diagram
*O	2756202	ODC	08/26/2009	Updated Ordering Information table and added note 24.
*P	2785207	ODC	10/12/2009	Added information on Pb-free parts in the Ordering information table.
*Q	2811890	ODC	11/20/2009	Updated Program I/Os for the CY7C68016A-56LTXC and CY7C68016A-56LTXCT parts in "Ordering Information" on page 56.
*R	2896281	ODC	03/19/10	Removed inactive parts from the ordering information table. Updated package diagrams.Updated links in Sales, Solutions and Legal Information.
*S	3035980	ODC	09/22/10	Updated template. Changed PPM requirement for the external crystal from +/- 10 ppm to +/- 100 ppm under Electrical specifications. Added table of contents, ordering code definitions, acronym table, and units of measure.
*T	3161410	AAE	02/03/2011	Replaced 56-Pin QFN 8 × 8 mm Punch Version Package Diagram (Figure 11.2) and 56-Pin QFN 8 × 8 mm Sawn Version Package Diagram (Figure 11.3). Updated Package Diagrams (Figure 11.4, Figure 11.5).
*U	3195232	ODC	03/14/2011	Updated table numbering. Added typical values to Table 18 on page 45 and Table 20 on page 46 based on data obtained from SHAK-63 and SHAK 69. Updated Table 13, "Thermal Characteristics," on page 39 (CDT 89510) Updated package diagram 001-03901 to *D.
*V	3512313	GAYA	02/01/2012	Removed obsolete part CY7C68014A-56BAXC Removed pruned part CY7C68016A-56LFXC Added parts CY7C68013A-56BAXCT and CY7C68013A-56PVXCT Updated Package Diagrams

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