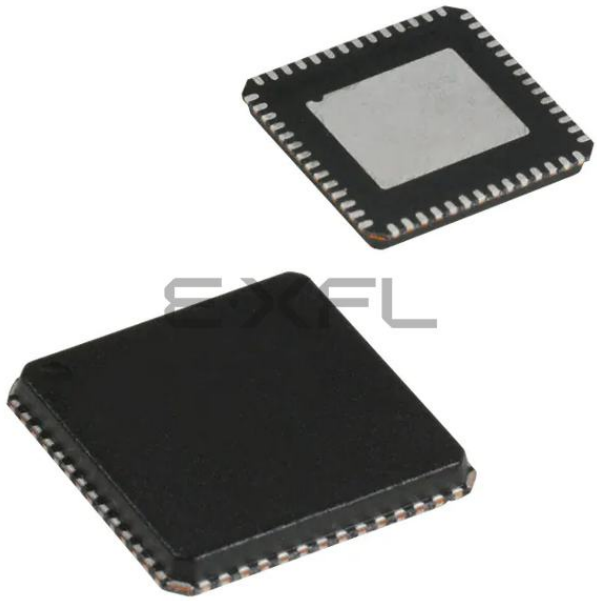


**Welcome to E-XFL.COM**

## Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

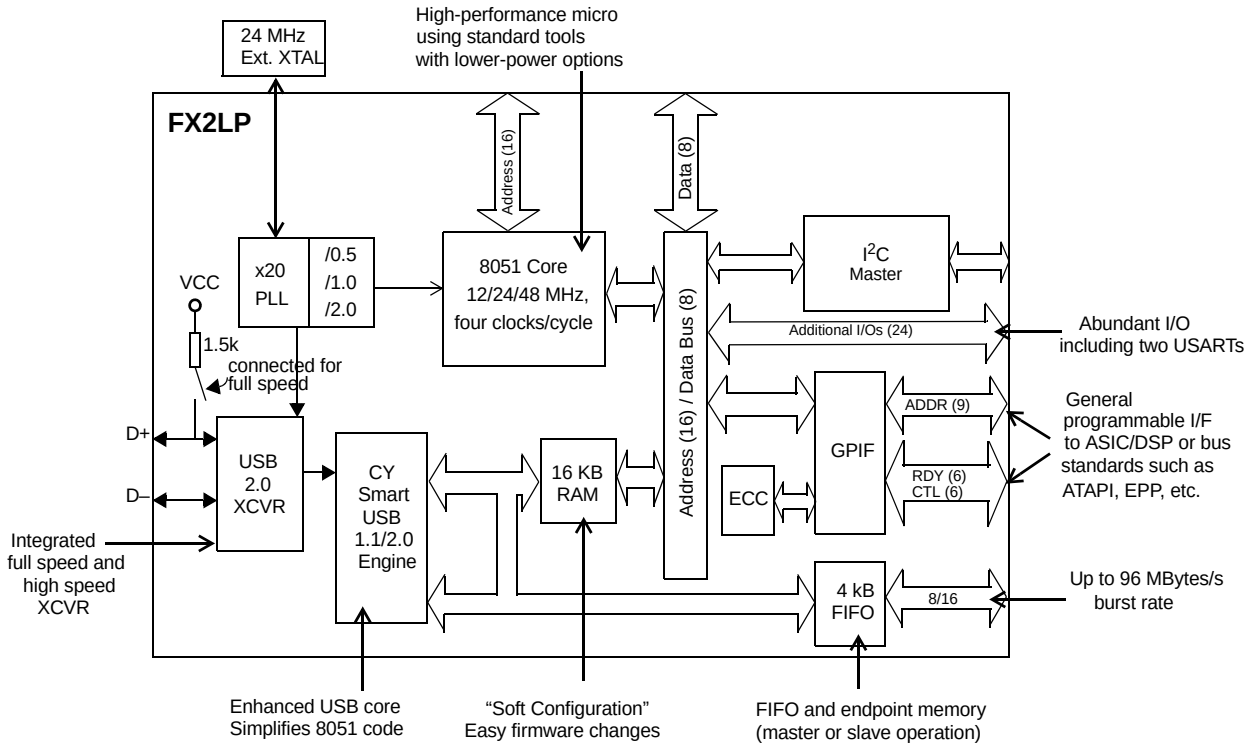
**Embedded - Microcontrollers - Application Specific** represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

## What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

| Details | |
|---|---|
| Product Status | Obsolete |
| Applications | USB Microcontroller |
| Core Processor | 8051 |
| Program Memory Type | ROMless |
| Controller Series | CY7C680xx |
| RAM Size | 16K x 8 |
| Interface | I²C, USB, USART |
| Number of I/O | 24 |
| Voltage - Supply | 3V ~ 3.6V |
| Operating Temperature | -40°C ~ 85°C |
| Mounting Type | Surface Mount |
| Package / Case | 56-VFQFN Exposed Pad |
| Supplier Device Package | 56-QFN (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy7c68013a-56lfxi |

## Logic Block Diagram




Cypress's EZ-USB® FX2LP™ (CY7C68013A/14A) is a low-power version of the EZ-USB FX2™ (CY7C68013), which is a highly integrated, low-power USB 2.0 microcontroller. By integrating the USB 2.0 transceiver, serial interface engine (SIE), enhanced 8051 microcontroller, and a programmable peripheral interface in a single chip, Cypress has created a cost-effective solution that provides superior time-to-market advantages with low power to enable bus-powered applications.

The ingenious architecture of FX2LP results in data transfer rates of over 53 Mbytes per second (the maximum allowable USB 2.0 bandwidth), while still using a low-cost 8051 microcontroller in a package as small as a 56 VFBGA (5 mm x 5 mm). Because it incorporates the USB 2.0 transceiver, the FX2LP is more economical, providing a smaller-footprint solution than a USB 2.0 SIE or external transceiver implementations.

With EZ-USB FX2LP, the Cypress Smart SIE handles most of the USB 1.1 and 2.0 protocol in hardware, freeing the embedded microcontroller for application-specific functions and decreasing the development time to ensure USB compatibility.

The general programmable interface (GPIF) and Master/Slave Endpoint FIFO (8-bit or 16-bit data bus) provide an easy and glueless interface to popular interfaces such as ATA, UTOPIA, EPP, PCMCIA, and most DSP/processors.

The FX2LP draws less current than the FX2 (CY7C68013), has double the on-chip code/data RAM, and is fit, form, and function compatible with the 56-, 100-, and 128-pin FX2.

Five packages are defined for the family: 56 VFBGA, 56 SSOP, 56 QFN, 100 TQFP, and 128 TQFP.

The FX2LP jump instruction is encoded as follows:.

**Table 3. INT2 USB Interrupts**

| USB INTERRUPT TABLE FOR INT2 | | | |
|---|---|---|---|
| **Priority** | **INT2VEC Value** | **Source** | **Notes** |
| 1 | 00 | SUDAV | Setup data available |
| 2 | 04 | SOF | Start of frame (or microframe) |
| 3 | 08 | SUTOK | Setup token received |
| 4 | 0C | SUSPEND | USB suspend request |
| 5 | 10 | USB RESET | Bus reset |
| 6 | 14 | HISPEED | Entered high speed operation |
| 7 | 18 | EP0ACK | FX2LP ACK'd the CONTROL Handshake |
| 8 | 1C | | reserved |
| 9 | 20 | EP0-IN | EP0-IN ready to be loaded with data |
| 10 | 24 | EP0-OUT | EP0-OUT has USB data |
| 11 | 28 | EP1-IN | EP1-IN ready to be loaded with data |
| 12 | 2C | EP1-OUT | EP1-OUT has USB data |
| 13 | 30 | EP2 | IN: buffer available. OUT: buffer has data |
| 14 | 34 | EP4 | IN: buffer available. OUT: buffer has data |
| 15 | 38 | EP6 | IN: buffer available. OUT: buffer has data |
| 16 | 3C | EP8 | IN: buffer available. OUT: buffer has data |
| 17 | 40 | IBN | IN-Bulk-NAK (any IN endpoint) |
| 18 | 44 | | reserved |
| 19 | 48 | EP0PING | EP0 OUT was pinged and it NAK'd |
| 20 | 4C | EP1PING | EP1 OUT was pinged and it NAK'd |
| 21 | 50 | EP2PING | EP2 OUT was pinged and it NAK'd |
| 22 | 54 | EP4PING | EP4 OUT was pinged and it NAK'd |
| 23 | 58 | EP6PING | EP6 OUT was pinged and it NAK'd |
| 24 | 5C | EP8PING | EP8 OUT was pinged and it NAK'd |
| 25 | 60 | ERRLIMIT | Bus errors exceeded the programmed limit |
| 26 | 64 | – | – |
| 27 | 68 | – | Reserved |
| 28 | 6C | – | Reserved |
| 29 | 70 | EP2ISOERR | ISO EP2 OUT PID sequence error |
| 30 | 74 | EP4ISOERR | ISO EP4 OUT PID sequence error |
| 31 | 78 | EP6ISOERR | ISO EP6 OUT PID sequence error |
| 32 | 7C | EP8ISOERR | ISO EP8 OUT PID sequence error |

If Autovectoring is enabled (AV2EN = 1 in the INTSET-UP register), the FX2LP substitutes its INT2VEC byte. Therefore, if the high byte ("page") of a jump table address is preloaded at the location 0x0044, the automatically inserted INT2VEC byte at 0x0045 directs the jump to the correct address out of the 27 addresses within the page.

*FIFO/GPIF Interrupt (INT4)*

Just as the USB Interrupt is shared among 27 individual USB interrupt sources, the FIFO/GPIF interrupt is shared among 14 individual FIFO/GPIF sources. The FIFO/GPIF Interrupt, similar to the USB Interrupt, can employ autovectoring.

Table 4 on page 8 shows the priority and INT4VEC values for the 14 FIFO/GPIF interrupt sources.

**Table 4. Individual FIFO/GPIF Interrupt Sources**

| Priority | INT4VEC Value | Source | Notes |
|---|---|---|---|
| 1 | 80 | EP2PF | Endpoint 2 programmable flag |
| 2 | 84 | EP4PF | Endpoint 4 programmable flag |
| 3 | 88 | EP6PF | Endpoint 6 programmable flag |
| 4 | 8C | EP8PF | Endpoint 8 programmable flag |
| 5 | 90 | EP2EF | Endpoint 2 empty flag [3] |
| 6 | 94 | EP4EF | Endpoint 4 empty flag |
| 7 | 98 | EP6EF | Endpoint 6 empty flag |
| 8 | 9C | EP8EF | Endpoint 8 empty flag |
| 9 | A0 | EP2FF | Endpoint 2 full flag |
| 10 | A4 | EP4FF | Endpoint 4 full flag |
| 11 | A8 | EP6FF | Endpoint 6 full flag |
| 12 | AC | EP8FF | Endpoint 8 full flag |
| 13 | B0 | GPIFDONE | GPIF operation complete |
| 14 | B4 | GPIFWF | GPIF waveform |

If Autovectoring is enabled (AV4EN = 1 in the INTSET-UP register), the FX 2LP substitutes its INT4VEC byte. Therefore, if the high byte (“page”) of a jump-table address is preloaded at location 0x0054, the automatically inserted INT4VEC byte at 0x0055 directs the jump to the correct address out of the 14 addresses within the page. When the ISR occurs, the FX2LP pushes the program counter to its stack then jumps to address 0x0053, where it expects to find a “jump” instruction to the interrupt service routine (ISR).

**Note**
3. Errata: In Slave FIFO Asynchronous Word Wide mode, if a single word data is transferred from the USB host to EP2, configured as OUT Endpoint (EP) in the first transaction, then the Empty flag behaves incorrectly. This does not happen if the data size is more than one word in the first transaction. For more information, see the “Errata” on page 65.

## Program/Data RAM

*SizeThe FX2LP has 16 KB of internal program/data RAM, where PSEN#/RD# signals are internally ORed to enable the 8051 to access it as both program and data memory. No USB control registers appears in this space.*

Two memory maps are shown in the following diagrams:

Figure 3 on page 10 shows the Internal Code Memory, EA = 0.

Figure 4 on page 11 shows the External Code Memory, EA = 1.

*Internal Code Memory, EA = 0*

This mode implements the internal 16 KB block of RAM (starting at 0) as combined code and data memory. When external RAM or ROM is added, the external read and write strobes are suppressed for memory spaces that exist inside the chip. This enables the user to connect a 64 KB memory without requiring address decodes to keep clear of internal memory spaces.

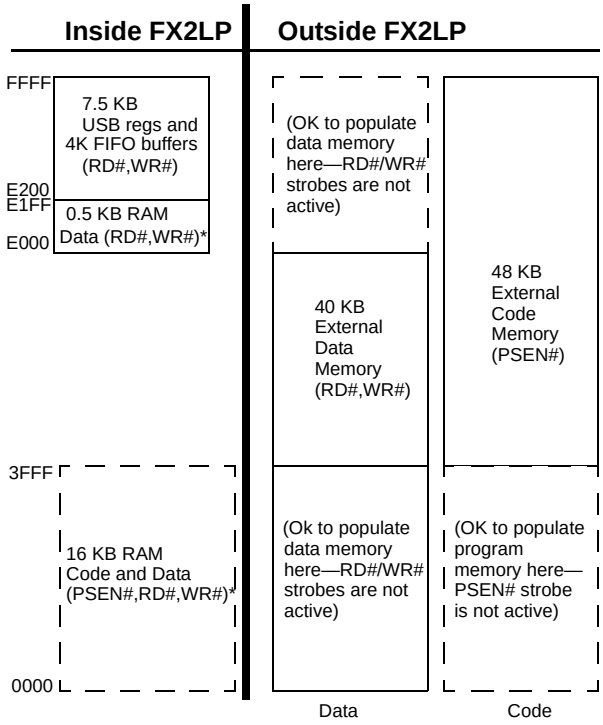
Only the internal 16 KB and scratch pad 0.5 KB RAM spaces have the following access:

- USB download
- USB upload
- Setup data pointer
- $I^2C$ interface boot load

*External Code Memory, EA = 1*

The bottom 16 KB of program memory is external and therefore the bottom 16 KB of internal RAM is accessible only as a data memory.

**Figure 3. Internal Code Memory, EA = 0**




*SUDPTR, USB upload/download, $I^2C$ interface boot access

**Note**
4. If the external clock is powered at the same time as the CY7C680xxA and has a stabilization wait period, it must be added to the 200 µs.

In the Slave (S) mode, FX2LP accepts either an internally derived clock or externally supplied clock (IFCLK, max frequency 48 MHz) and SLCS#, SLRD, SLWR, SLOE, PKTEND signals from external logic. When using an external IFCLK, the external clock must be present before switching to the external clock with the IFCLKSRC bit. Each endpoint can individually be selected for byte or word operation by an internal configuration bit and a Slave FIFO Output Enable signal (SLOE) that enables data of the selected width. External logic must ensure that the output enable signal is inactive when writing data to a slave FIFO. The slave interface can also operate asynchronously, where the SLRD and SLWR signals act directly as strobes, rather than a clock qualifier as in synchronous mode. The signals SLRD, SLWR, SLOE, and PKTEND are gated by the signal SLCS#.

*GPIF and FIFO Clock Rates*

An 8051 register bit selects one of two frequencies for the internally supplied interface clock: 30 MHz and 48 MHz. Alternatively, an externally supplied clock of 5 MHz–48 MHz feeding the IFCLK pin can be used as the interface clock. IFCLK can be configured to function as an output clock when the GPIF and FIFOs are internally clocked. An output enable bit in the IFCONFIG register turns this clock output off, if desired. Another bit within the IFCONFIG register inverts the IFCLK signal whether internally or externally sourced.

## GPIF

The GPIF is a flexible 8-bit or 16-bit parallel interface driven by a user-programmable finite state machine. It enables the CY7C68013A/15A to perform local bus mastering and can implement a wide variety of protocols such as ATA interface, printer parallel port, and Utopia.

The GPIF has six programmable control outputs (CTL), nine address outputs (GPIFADRx), and six general-purpose ready inputs (RDY). The data bus width can be 8 or 16 bits. Each GPIF vector defines the state of the control outputs, and determines what state a ready input (or multiple inputs) must be before proceeding. The GPIF vector can be programmed to advance a FIFO to the next data value, advance an address, etc. A sequence of the GPIF vectors make up a single waveform that is executed to perform the desired data move between the FX2LP and the external device.

*Six Control OUT Signals*

The 100-pin and 128-pin packages bring out all six Control Output pins (CTL0-CTL5). The 8051 programs the GPIF unit to define the CTL waveforms. The 56-pin package brings out three of these signals, CTL0–CTL2. CTLx waveform edges can be programmed to make transitions as fast as once per clock (20.8 ns using a 48-MHz clock).

*Six Ready IN Signals*

The 100-pin and 128-pin packages bring out all six Ready inputs (RDY0–RDY5). The 8051 programs the GPIF unit to test the RDY pins for GPIF branching. The 56-pin package brings out two of these signals, RDY0–1.

*Nine GPIF Address OUT Signals*

Nine GPIF address lines are available in the 100-pin and 128-pin packages, GPIFADR[8..0]. The GPIF address lines enable indexing through up to a 512-byte block of RAM. If more address lines are needed, then I/O port pins are used.

*Long Transfer Mode*

In the master mode, the 8051 appropriately sets GPIF transaction count registers (GPIFTCB3, GPIFTCB2, GPIFTCB1, or GPIFTCB0) for unattended transfers of up to $2^{32}$ transactions. The GPIF automatically throttles data flow to prevent under or overflow until the full number of requested transactions complete. The GPIF decrements the value in these registers to represent the current status of the transaction.

## ECC Generation[8]

The EZ-USB can calculate ECCs (Error Correcting Codes) on data that passes across its GPIF or Slave FIFO interfaces. There are two ECC configurations: Two ECCs, each calculated over 256 bytes (SmartMedia Standard); and one ECC calculated over 512 bytes.

The ECC can correct any one-bit error or detect any two-bit error.

*ECC Implementation*

The two ECC configurations are selected by the ECCM bit:

**ECCM = 0**

Two 3-byte ECCs, each calculated over a 256-byte block of data. This configuration conforms to the SmartMedia Standard.

Write any value to ECCRESET, then pass data across the GPIF or Slave FIFO interface. The ECC for the first 256 bytes of data is calculated and stored in ECC1. The ECC for the next 256 bytes is stored in ECC2. After the second ECC is calculated, the values in the ECCx registers do not change until ECCRESET is written again, even if more data is subsequently passed across the interface.

**ECCM = 1**

One 3-byte ECC calculated over a 512-byte block of data.

Write any value to ECCRESET then pass data across the GPIF or Slave FIFO interface. The ECC for the first 512 bytes of data is calculated and stored in ECC1; ECC2 is unused. After the ECC is calculated, the values in ECC1 do not change even if more data is subsequently passed across the interface, till ECCRESET is written again.

## USB Uploads and Downloads

The core has the ability to directly edit the data contents of the internal 16-KB RAM and of the internal 512-byte scratch pad RAM via a vendor-specific command. This capability is normally used when soft downloading the user code and is available only to and from the internal RAM, only when the 8051 is held in reset. The available RAM spaces are 16 KB from 0x0000–0x3FFF (code/data) and 512 bytes from 0xE000–0xE1FF (scratch pad data RAM)[9].

**Notes**
8. To use the ECC logic, the GPIF or Slave FIFO interface must be configured for byte-wide operation.
9. After the data is downloaded from the host, a “loader” can execute from internal RAM to transfer downloaded data to external memory.

**Figure 11. CY7C68013A 56-pin VFBGA Pin Assignment – Top View**

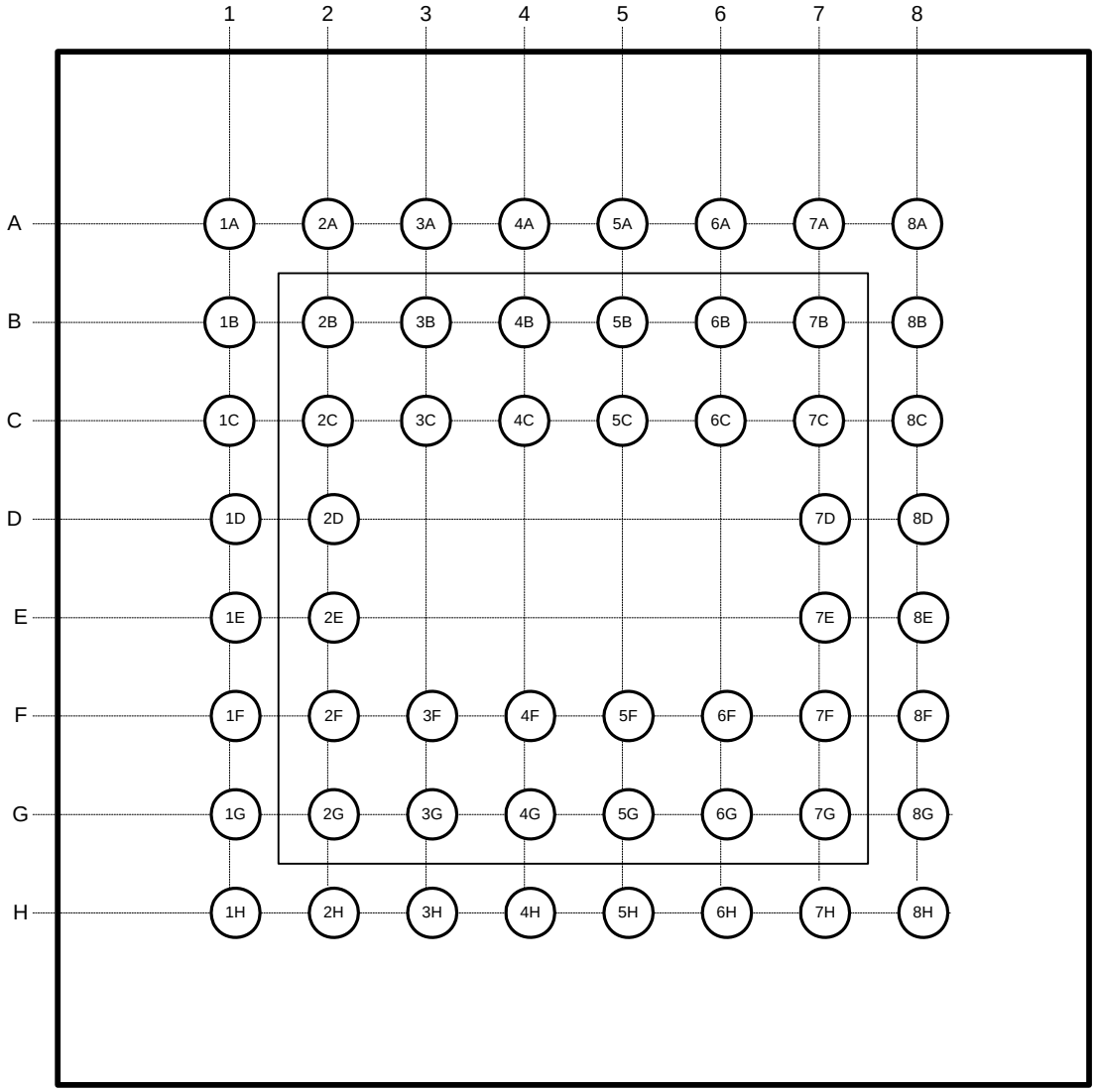


**Table 11. FX2LP Pin Descriptions**[11] (continued)

| 128 TQFP | 100 TQFP | 56 SSOP | 56 QFN | 56 VFBGA | Name | Type | Default | Reset[12] | Description |
|---|---|---|---|---|---|---|---|---|---|
| 34 | 28 | – | – | | BKPT | Output | L | L | **Breakpoint**. This pin goes active (HIGH) when the 8051 address bus matches the BPADDRH/L registers and breakpoints are enabled in the BREAKPT register (BPEN = 1). If the BPPULSE bit in the BREAKPT register is HIGH, this signal pulses HIGH for eight 12-/24-/48-MHz clocks. If the BPPULSE bit is LOW, the signal remains HIGH until the 8051 clears the BREAK bit (by writing 1 to it) in the BREAKPT register. |
| 99 | 77 | 49 | 42 | 8B | RESET# | Input | N/A | N/A | **Active LOW Reset**. Resets the entire chip. See section "Reset and Wakeup" on page 9 for more details. |
| 35 | – | – | – | – | EA | Input | N/A | N/A | **External Access**. This pin determines where the 8051 fetches code between addresses 0x0000 and 0x3FFF. If EA = 0 the 8051 fetches this code from its internal RAM. IF EA = 1 the 8051 fetches this code from external memory. |
| 12 | 11 | 12 | 5 | 1C | XTALIN | Input | N/A | N/A | **Crystal Input**. Connect this signal to a 24-MHz parallel-resonant, fundamental mode crystal and load capacitor to GND.<br>It is also correct to drive XTALIN with an external 24-MHz square wave derived from another clock source. When driving from an external source, the driving signal should be a 3.3-V square wave. |
| 11 | 10 | 11 | 4 | 2C | XTALOUT | Output | N/A | N/A | **Crystal Output**. Connect this signal to a 24-MHz parallel-resonant, fundamental mode crystal and load capacitor to GND.<br>If an external clock is used to drive XTALIN, leave this pin open. |
| 1 | 100 | 5 | 54 | 2B | CLKOUT on CY7C68013A and CY7C68014A<br>----------<br>PE1 on CY7C68015A and CY7C68016A | O/Z<br>----------<br>I/O/Z | 12 MHz<br>----------<br>I | Clock Driven<br>----------<br>Z | **CLKOUT:** 12-, 24- or 48-MHz clock, phase-locked to the 24-MHz input clock. The 8051 defaults to 12-MHz operation. The 8051 may three-state this output by setting CPUCS.1 = 1.<br>----------<br>------**PE1** is a bidirectional I/O port pin. |
| **Port A** | | | | | | | | | |
| 82 | 67 | 40 | 33 | 8G | PA0 or INT0# | I/O/Z | I (PA0) | Z (PA0) | Multiplexed pin whose function is selected by PORTACFG.0<br>**PA0** is a bidirectional I/O port pin.<br>**INT0#** is the active-LOW 8051 INT0 interrupt input signal, which is either edge-triggered (IT0 = 1) or level-triggered (IT0 = 0). |
| 83 | 68 | 41 | 34 | 6G | PA1 or INT1# | I/O/Z | I (PA1) | Z (PA1) | Multiplexed pin whose function is selected by: PORTACFG.1<br>**PA1** is a bidirectional I/O port pin.<br>**INT1#** is the active-LOW 8051 INT1 interrupt input signal, which is either edge-triggered (IT1 = 1) or level-triggered (IT1 = 0). |

## Register Summary

FX2LP register bit definitions are described in the FX2LP TRM in greater detail.

**Table 12. FX2LP Register Summary**

| Hex | Size | Name | Description | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Default | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | GPIF Waveform Memories | | | | | | | | | | | |
| E400 | 128 | WAVEDATA | GPIF Waveform Descriptor 0, 1, 2, 3 data | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| E480 | 128 | reserved | | | | | | | | | | | |
| | | GENERAL CONFIGURATION | | | | | | | | | | | |
| E50D | | GPCR2 | General Purpose Configuration Register 2 | reserved | reserved | reserved | FULL_SPEED_ONLY | reserved | reserved | reserved | reserved | 00000000 | R |
| E600 | 1 | CPUCS | CPU Control & Status | 0 | 0 | PORTCSTB | CLKSPD1 | CLKSPD0 | CLKINV | CLKOE | 8051RES | 00000010 | rrbbbbbr |
| E601 | 1 | IFCONFIG | Interface Configuration (Ports, GPIF, slave FIFOs) | IFCLKSRC | 3048MHZ | IFCLKOE | IFCLKPOL | ASYNC | GSTATE | IFCFG1 | IFCFG0 | 10000000 | RW |
| E602 | 1 | PINFLAGSAB[13] | Slave FIFO FLAGA and FLAGB Pin Configuration | FLAGB3 | FLAGB2 | FLAGB1 | FLAGB0 | FLAGA3 | FLAGA2 | FLAGA1 | FLAGA0 | 00000000 | RW |
| E603 | 1 | PINFLAGSCD[13] | Slave FIFO FLAGC and FLAGD Pin Configuration | FLAGD3 | FLAGD2 | FLAGD1 | FLAGD0 | FLAGC3 | FLAGC2 | FLAGC1 | FLAGC0 | 00000000 | RW |
| E604 | 1 | FIFORESET[13] | Restore FIFOS to default state | NAKALL | 0 | 0 | 0 | EP3 | EP2 | EP1 | EP0 | xxxxxxxx | W |
| E605 | 1 | BREAKPT | Breakpoint Control | 0 | 0 | 0 | 0 | BREAK | BPPULSE | BPEN | 0 | 00000000 | rrrrbbbr |
| E606 | 1 | BPADDRH | Breakpoint Address H | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | xxxxxxxx | RW |
| E607 | 1 | BPADDRL | Breakpoint Address L | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | xxxxxxxx | RW |
| E608 | 1 | UART230 | 230 Kbaud internally generated ref. clock | 0 | 0 | 0 | 0 | 0 | 0 | 230UART1 | 230UART0 | 00000000 | rrrrrrbb |
| E609 | 1 | FIFOPINPOLAR[13] | Slave FIFO Interface pins polarity | 0 | 0 | PKTEND | SLOE | SLRD | SLWR | EF | FF | 00000000 | rrbbbbbb |
| E60A | 1 | REVID | Chip Revision | rv7 | rv6 | rv5 | rv4 | rv3 | rv2 | rv1 | rv0 | RevA 00000001 | R |
| E60B | 1 | REVCTL[13] | Chip Revision Control | 0 | 0 | 0 | 0 | 0 | 0 | dyn_out | enh_pkt | 00000000 | rrrrrrbb |
| | | UDMA | | | | | | | | | | | |
| E60C | 1 | GPIFHOLDAMOUNT | MSTB Hold Time (for UDMA) | 0 | 0 | 0 | 0 | 0 | 0 | HOLDTIME1 | HOLDTIME0 | 00000000 | rrrrrrbb |
| | 3 | reserved | | | | | | | | | | | |
| | | ENDPOINT CONFIGURATION | | | | | | | | | | | |
| E610 | 1 | EP1OUTCFG | Endpoint 1-OUT Configuration | VALID | 0 | TYPE1 | TYPE0 | 0 | 0 | 0 | 0 | 10100000 | brbbrrrr |
| E611 | 1 | EP1INCFG | Endpoint 1-IN Configuration | VALID | 0 | TYPE1 | TYPE0 | 0 | 0 | 0 | 0 | 10100000 | brbbrrrr |
| E612 | 1 | EP2CFG | Endpoint 2 Configuration | VALID | DIR | TYPE1 | TYPE0 | SIZE | 0 | BUF1 | BUF0 | 10100010 | bbbbbrbb |
| E613 | 1 | EP4CFG | Endpoint 4 Configuration | VALID | DIR | TYPE1 | TYPE0 | 0 | 0 | 0 | 0 | 10100000 | bbbbrrrr |
| E614 | 1 | EP6CFG | Endpoint 6 Configuration | VALID | DIR | TYPE1 | TYPE0 | SIZE | 0 | BUF1 | BUF0 | 11100010 | bbbbbrbb |
| E615 | 1 | EP8CFG | Endpoint 8 Configuration | VALID | DIR | TYPE1 | TYPE0 | 0 | 0 | 0 | 0 | 11100000 | bbbbrrrr |
| | 2 | reserved | | | | | | | | | | | |
| E618 | 1 | EP2FIFOCFG[13] | Endpoint 2 / slave FIFO configuration | 0 | INFM1 | OEP1 | AUTOOUT | AUTOIN | ZEROLENIN | 0 | WORDWIDE | 00000101 | rbbbbbrb |
| E619 | 1 | EP4FIFOCFG[13] | Endpoint 4 / slave FIFO configuration | 0 | INFM1 | OEP1 | AUTOOUT | AUTOIN | ZEROLENIN | 0 | WORDWIDE | 00000101 | rbbbbbrb |
| E61A | 1 | EP6FIFOCFG[13] | Endpoint 6 / slave FIFO configuration | 0 | INFM1 | OEP1 | AUTOOUT | AUTOIN | ZEROLENIN | 0 | WORDWIDE | 00000101 | rbbbbbrb |
| E61B | 1 | EP8FIFOCFG[13] | Endpoint 8 / slave FIFO configuration | 0 | INFM1 | OEP1 | AUTOOUT | AUTOIN | ZEROLENIN | 0 | WORDWIDE | 00000101 | rbbbbbrb |
| E61C | 4 | reserved | | | | | | | | | | | |
| E620 | 1 | EP2AUTOINLENH[13] | Endpoint 2 AUTOIN Packet Length H | 0 | 0 | 0 | 0 | 0 | PL10 | PL9 | PL8 | 00000010 | rrrrrbbb |
| E621 | 1 | EP2AUTOINLENL[13] | Endpoint 2 AUTOIN Packet Length L | PL7 | PL6 | PL5 | PL4 | PL3 | PL2 | PL1 | PL0 | 00000000 | RW |
| E622 | 1 | EP4AUTOINLENH[13] | Endpoint 4 AUTOIN Packet Length H | 0 | 0 | 0 | 0 | 0 | 0 | PL9 | PL8 | 00000010 | rrrrrrbb |
| E623 | 1 | EP4AUTOINLENL[13] | Endpoint 4 AUTOIN Packet Length L | PL7 | PL6 | PL5 | PL4 | PL3 | PL2 | PL1 | PL0 | 00000000 | RW |
| E624 | 1 | EP6AUTOINLENH[13] | Endpoint 6 AUTOIN Packet Length H | 0 | 0 | 0 | 0 | 0 | PL10 | PL9 | PL8 | 00000010 | rrrrrbbb |
| E625 | 1 | EP6AUTOINLENL[13] | Endpoint 6 AUTOIN Packet Length L | PL7 | PL6 | PL5 | PL4 | PL3 | PL2 | PL1 | PL0 | 00000000 | RW |
| E626 | 1 | EP8AUTOINLENH[13] | Endpoint 8 AUTOIN Packet Length H | 0 | 0 | 0 | 0 | 0 | 0 | PL9 | PL8 | 00000010 | rrrrrrbb |
| E627 | 1 | EP8AUTOINLENL[13] | Endpoint 8 AUTOIN Packet Length L | PL7 | PL6 | PL5 | PL4 | PL3 | PL2 | PL1 | PL0 | 00000000 | RW |
| E628 | 1 | ECCCFG | ECC Configuration | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ECCM | 00000000 | rrrrrrrb |
| E629 | 1 | ECCRESET | ECC Reset | x | x | x | x | x | x | x | x | 00000000 | W |
| E62A | 1 | ECC1B0 | ECC1 Byte 0 Address | LINE15 | LINE14 | LINE13 | LINE12 | LINE11 | LINE10 | LINE9 | LINE8 | 00000000 | R |

**Note**
13. Read and writes to these registers may require synchronization delay; see Technical Reference Manual for “Synchronization Delay.”

**Table 12. FX2LP Register Summary** (continued)

| Hex | Size | Name | Description | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Default | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| xxxx | | I²C Configuration Byte | | 0 | DISCON | 0 | 0 | 0 | 0 | 0 | 400KHZ | xxxxxxxx [16] | n/a |
| | | Special Function Registers (SFRs) | | | | | | | | | | | |
| 80 | 1 | IOA[15] | Port A (bit addressable) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| 81 | 1 | SP | Stack Pointer | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00000111 | RW |
| 82 | 1 | DPL0 | Data Pointer 0 L | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | 00000000 | RW |
| 83 | 1 | DPH0 | Data Pointer 0 H | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | 00000000 | RW |
| 84 | 1 | DPL1[15] | Data Pointer 1 L | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | 00000000 | RW |
| 85 | 1 | DPH1[15] | Data Pointer 1 H | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | 00000000 | RW |
| 86 | 1 | DPS[15] | Data Pointer 0/1 select | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SEL | 00000000 | RW |
| 87 | 1 | PCON | Power Control | SMOD0 | x | 1 | 1 | x | x | x | IDLE | 00110000 | RW |
| 88 | 1 | TCON | Timer/Counter Control (bit addressable) | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 | 00000000 | RW |
| 89 | 1 | TMOD | Timer/Counter Mode Control | GATE | CT | M1 | M0 | GATE | CT | M1 | M0 | 00000000 | RW |
| 8A | 1 | TL0 | Timer 0 reload L | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00000000 | RW |
| 8B | 1 | TL1 | Timer 1 reload L | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00000000 | RW |
| 8C | 1 | TH0 | Timer 0 reload H | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | 00000000 | RW |
| 8D | 1 | TH1 | Timer 1 reload H | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | 00000000 | RW |
| 8E | 1 | CKCON[15] | Clock Control | x | x | T2M | T1M | T0M | MD2 | MD1 | MD0 | 00000001 | RW |
| 8F | 1 | reserved | | | | | | | | | | | |
| 90 | 1 | IOB[15] | Port B (bit addressable) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| 91 | 1 | EXIF[15] | External Interrupt Flag(s) | IE5 | IE4 | I²CINT | USBNT | 1 | 0 | 0 | 0 | 00001000 | RW |
| 92 | 1 | MPAGE[15] | Upper Addr Byte of MOVX using @R0 / @R1 | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | 00000000 | RW |
| 93 | 5 | reserved | | | | | | | | | | | |
| 98 | 1 | SCON0 | Serial Port 0 Control (bit addressable) | SM0_0 | SM1_0 | SM2_0 | REN_0 | TB8_0 | RB8_0 | TI_0 | RI_0 | 00000000 | RW |
| 99 | 1 | SBUF0 | Serial Port 0 Data Buffer | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00000000 | RW |
| 9A | 1 | AUTOPTRH1[15] | Autopointer 1 Address H | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | 00000000 | RW |
| 9B | 1 | AUTOPTRL1[15] | Autopointer 1 Address L | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | 00000000 | RW |
| 9C | 1 | reserved | | | | | | | | | | | |
| 9D | 1 | AUTOPTRH2[15] | Autopointer 2 Address H | A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | 00000000 | RW |
| 9E | 1 | AUTOPTRL2[15] | Autopointer 2 Address L | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | 00000000 | RW |
| 9F | 1 | reserved | | | | | | | | | | | |
| A0 | 1 | IOC[15] | Port C (bit addressable) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| A1 | 1 | INT2CLR[15] | Interrupt 2 clear | x | x | x | x | x | x | x | x | xxxxxxxx | W |
| A2 | 1 | INT4CLR[15] | Interrupt 4 clear | x | x | x | x | x | x | x | x | xxxxxxxx | W |
| A3 | 5 | reserved | | | | | | | | | | | |
| A8 | 1 | IE | Interrupt Enable (bit addressable) | EA | ES1 | ET2 | ES0 | ET1 | EX1 | ET0 | EX0 | 00000000 | RW |
| A9 | 1 | reserved | | | | | | | | | | | |
| AA | 1 | EP2468STAT[15] | Endpoint 2,4,6,8 status flags | EP8F | EP8E | EP6F | EP6E | EP4F | EP4E | EP2F | EP2E | 01011010 | R |
| AB | 1 | EP24FIFOFLGS[15] | Endpoint 2,4 slave FIFO status flags | 0 | EP4PF | EP4EF | EP4FF | 0 | EP2PF | EP2EF | EP2FF | 00100010 | R |
| AC | 1 | EP68FIFOFLGS[15] | Endpoint 6,8 slave FIFO status flags | 0 | EP8PF | EP8EF | EP8FF | 0 | EP6PF | EP6EF | EP6FF | 01100110 | R |
| AD | 2 | reserved | | | | | | | | | | | |
| AF | 1 | AUTOPTRSETUP[15] | Autopointer 1&2 setup | 0 | 0 | 0 | 0 | 0 | APTR2INC | APTR1INC | APTREN | 00000110 | RW |
| B0 | 1 | IOD[15] | Port D (bit addressable) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| B1 | 1 | IOE[15] | Port E (NOT bit addressable) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| B2 | 1 | OEA[15] | Port A Output Enable | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00000000 | RW |
| B3 | 1 | OEB[15] | Port B Output Enable | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00000000 | RW |
| B4 | 1 | OEC[15] | Port C Output Enable | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00000000 | RW |
| B5 | 1 | OED[15] | Port D Output Enable | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00000000 | RW |
| B6 | 1 | OEE[15] | Port E Output Enable | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | 00000000 | RW |
| B7 | 1 | reserved | | | | | | | | | | | |
| B8 | 1 | IP | Interrupt Priority (bit addressable) | 1 | PS1 | PT2 | PS0 | PT1 | PX1 | PT0 | PX0 | 10000000 | RW |
| B9 | 1 | reserved | | | | | | | | | | | |
| BA | 1 | EP01STAT[15] | Endpoint 0&1 Status | 0 | 0 | 0 | 0 | 0 | EP1INBSY | EP1OUTBSY | EP0BSY | 00000000 | R |
| BB | 1 | GPIFTRIG[15, 13] | Endpoint 2,4,6,8 GPIF slave FIFO Trigger | DONE | 0 | 0 | 0 | 0 | RW | EP1 | EP0 | 10000xxx | brrrrbbb |
| BC | 1 | reserved | | | | | | | | | | | |
| BD | 1 | GPIFSGLDATH[15] | GPIF Data H (16-bit mode only) | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | xxxxxxxx | RW |

**Notes**
15. SFRs not part of the standard 8051 architecture.
16. If no EEPROM is detected by the SIE then the default is 00000000.

## Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power supplied (commercial)..... 0 °C to +70 °C

Ambient temperature with power supplied (industrial)..... –40 °C to + 105 °C

Supply voltage to ground potential .....–0.5 V to +4.0 V

DC input voltage to any input pin[17] ..... 5.25 V

DC voltage applied to outputs in high Z state ..... –0.5 V to $V_{CC}$ + 0.5 V

Power dissipation ..... 300 mW

Static discharge voltage..... .....>2000 V

Max output current, per I/O port ..... 10 mA

Max output current, all five I/O ports (128-pin and 100-pin packages)..... 50 mA

## Operating Conditions

$T_A$ (ambient temperature under bias) Commercial ..... 0 °C to +70 °C

$T_A$ (ambient temperature under bias) Industrial ..... –40 °C to +105 °C

Supply voltage .....+3.00 V to +3.60 V

Ground voltage ..... 0 V

$F_{OSC}$ (oscillator or crystal frequency) ..... 24 MHz ± 100 ppm, parallel resonant

## Thermal Characteristics

The following table displays the thermal characteristics of various packages:

**Table 13. Thermal Characteristics**

| Package | Ambient Temperature (°C) | $\theta_{Jc}$ Junction to Case Thermal Resistance (°C/W) | $\theta_{Ja}$ Junction to Ambient Thermal Resistance (°C/W) |
|---|---|---|---|
| 56 SSOP | 70 | 24.4 | 47.7 |
| 100 TQFP | 70 | 11.9 | 45.9 |
| 128 TQFP | 70 | 15.5 | 43.2 |
| 56 QFN | 70 | 10.6 | 25.2 |
| 56 VFBGA | 70 | 30.9 | 58.6 |

The junction temperature $\theta_j$, can be calculated using the following equation: $\theta_j = P*\theta_{Ja} + \theta_a$

Where,

P = Power

$\theta_{Ja}$ = Junction to ambient temperature ($\theta_{Jc} + \theta_{Ca}$)

$\theta_a$ = Ambient temperature (70 °C)

The case temperature $\theta_c$, can be calculated using the following equation: $\theta_c = P*\theta_{Ca} + \theta_a$

where,

P = Power

$\theta_{Ca}$ = Case to ambient temperature

$\theta_a$ = Ambient temperature (70 °C)

**Note**
17. Do not power I/O with the chip power OFF.

## Data Memory Read[21]

**Figure 13. Data Memory Read Timing Diagram**

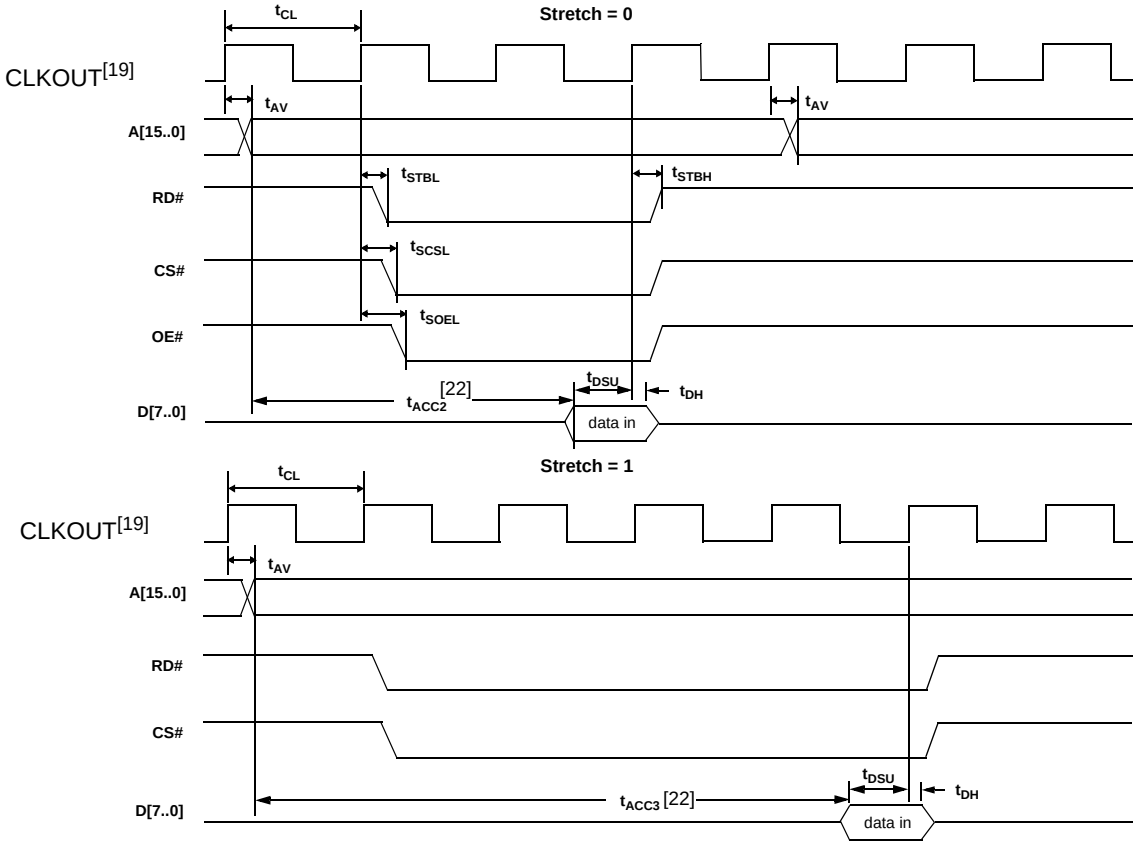



**Table 16. Data Memory Read Parameters**

| Parameter | Description | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| $t_{CL}$ | 1/CLKOUT frequency | – | 20.83 | – | ns | 48 MHz |
| | | – | 41.66 | – | ns | 24 MHz |
| | | – | 83.2 | – | ns | 12 MHz |
| $t_{AV}$ | Delay from clock to valid address | – | – | 10.7 | ns | – |
| $t_{STBL}$ | Clock to RD LOW | – | – | 11 | ns | – |
| $t_{STBH}$ | Clock to RD HIGH | – | – | 11 | ns | – |
| $t_{SCSL}$ | Clock to CS LOW | – | – | 13 | ns | – |
| $t_{SOEL}$ | Clock to OE LOW | – | – | 11.1 | ns | – |
| $t_{DSU}$ | Data setup to clock | 9.6 | – | – | ns | – |
| $t_{DH}$ | Data hold time | 0 | – | – | ns | – |

When using the AUTPOPTR1 or AUTOPTR2 to address external memory, the address of AUTOPTR1 is only active while either RD# or WR# is active. The address of AUTOPTR2 is active throughout the cycle and meets the address valid time for which is based on the stretch value.

**Notes**

21. The stretch memory cycle feature enables EZ-USB firmware to adjust the speed of data memory accesses not the program memory accesses. Details including typical strobe width timings can be found in the section 12.1.2 of the Technical Reference Manual. The address cycle width can be interpreted from these.
22. $t_{ACC2}$ and $t_{ACC3}$ are computed from these parameters as follows:
$t_{ACC2}$(24 MHz) = 3*$t_{CL}$ – $t_{AV}$ –$t_{DSU}$ = 106 ns
$t_{ACC2}$(48 MHz) = 3*$t_{CL}$ – $t_{AV}$ – $t_{DSU}$ = 43 ns
$t_{ACC3}$(24 MHz) = 5*$t_{CL}$ – $t_{AV}$ –$t_{DSU}$ = 190 ns
$t_{ACC3}$(48 MHz) = 5*$t_{CL}$ – $t_{AV}$ – $t_{DSU}$ = 86 ns

## Data Memory Write[23]

**Figure 14. Data Memory Write Timing Diagram**

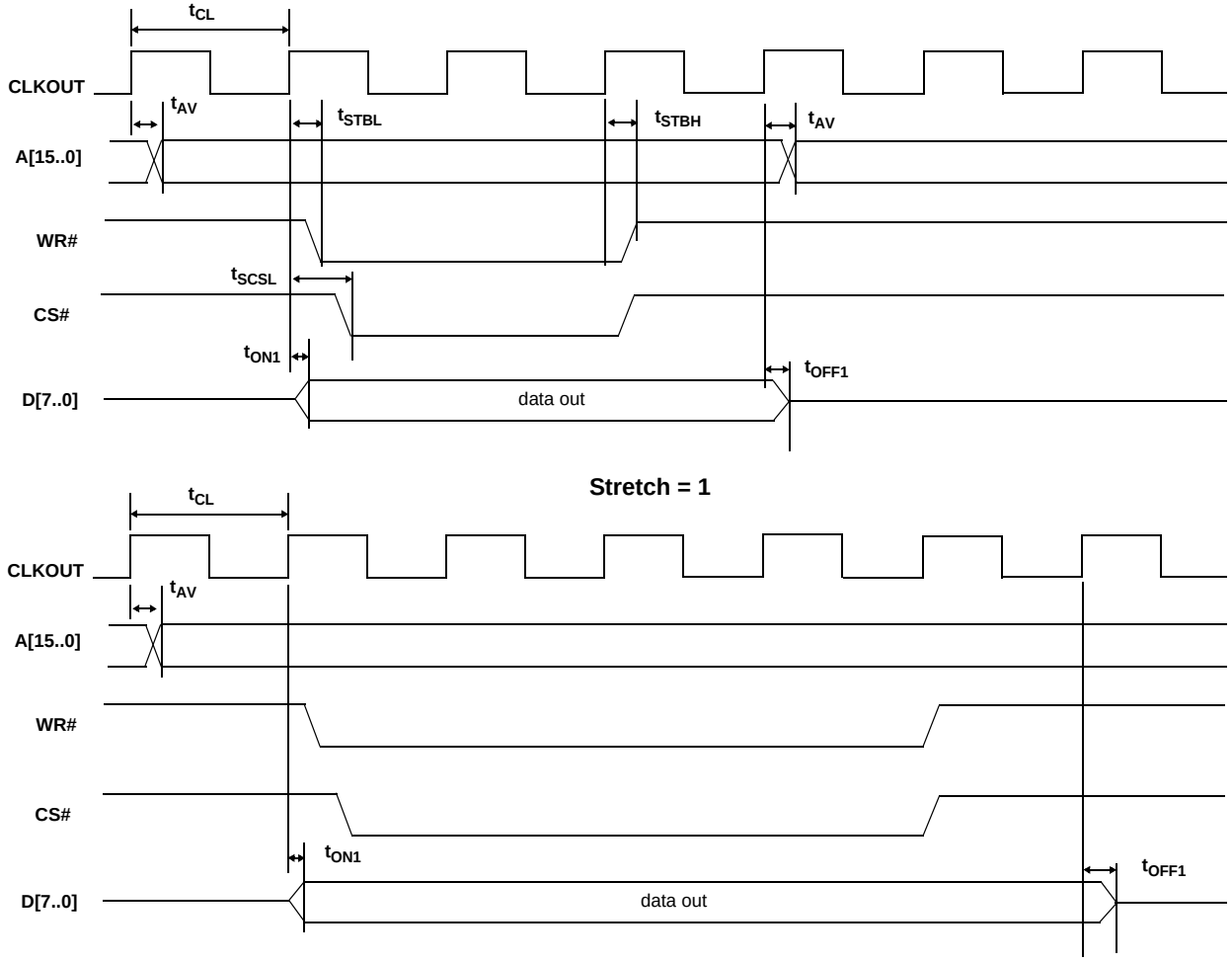


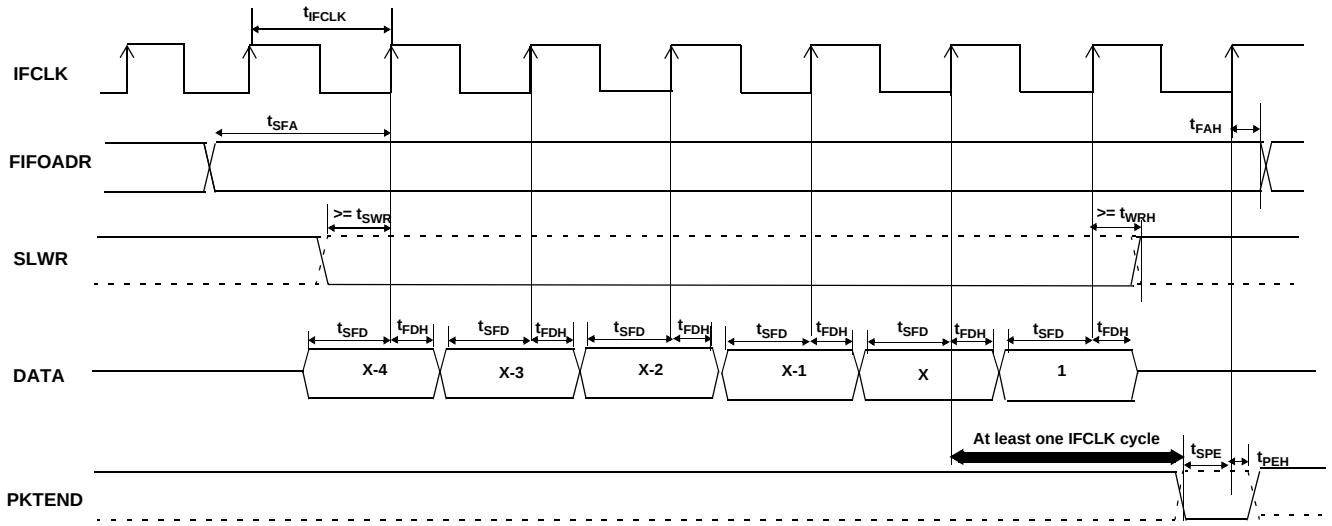

**Table 17. Data Memory Write Parameters**

| Parameter | Description | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $t_{AV}$ | Delay from clock to valid address | 0 | 10.7 | ns | – |
| $t_{STBL}$ | Clock to WR pulse LOW | 0 | 11.2 | ns | – |
| $t_{STBH}$ | Clock to WR pulse HIGH | 0 | 11.2 | ns | – |
| $t_{SCSL}$ | Clock to CS pulse LOW | – | 13.0 | ns | – |
| $t_{ON1}$ | Clock to data turn-on | 0 | 13.1 | ns | – |
| $t_{OFF1}$ | Clock to data hold time | 0 | 13.1 | ns | – |

When using the AUTPOPTR1 or AUTOPTR2 to address external memory, the address of AUTOPTR1 is only active while either RD# or WR# are active. The address of AUTOPTR2 is active throughout the cycle and meets the address valid time for which is based on the stretch value.

**Note**
23. The stretch memory cycle feature enables EZ-USB firmware to adjust the speed of data memory accesses not the program memory accesses. Details including typical strobe width timings can be found in the section 12.1.2 of the Technical Reference Manual. The address cycle width can be interpreted from these.

**Figure 24. Slave FIFO Synchronous Write Sequence and Timing Diagram[24]**




## Slave FIFO Asynchronous Packet End Strobe

**Figure 25. Slave FIFO Asynchronous Packet End Strobe Timing Diagram[24]**

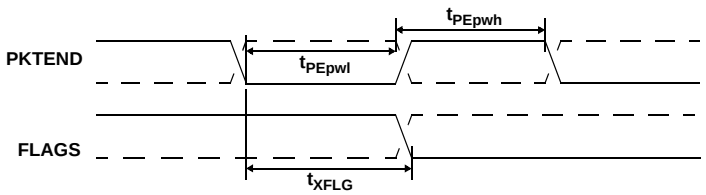



**Table 28. Slave FIFO Asynchronous Packet End Strobe Parameters[27]**

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{PEpwl}$ | PKTEND pulse width LOW | 50 | – | ns |
| $t_{PWpwh}$ | PKTEND pulse width HIGH | 50 | – | ns |
| $t_{XFLG}$ | PKTEND to FLAGS output propagation delay | – | 115 | ns |

## Slave FIFO Output Enable

**Figure 26. Slave FIFO Output Enable Timing Diagram[24]**

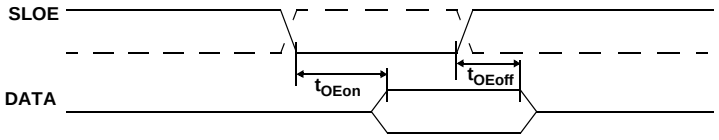



**Table 29. Slave FIFO Output Enable Parameters**

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{OEon}$ | SLOE assert to FIFO DATA output | | 10.5 | ns |
| $t_{OEoff}$ | SLOE deassert to FIFO DATA hold | | 10.5 | ns |

### Slave FIFO Address to Flags/Data

**Figure 27. Slave FIFO Address to Flags/Data Timing Diagram[24]**

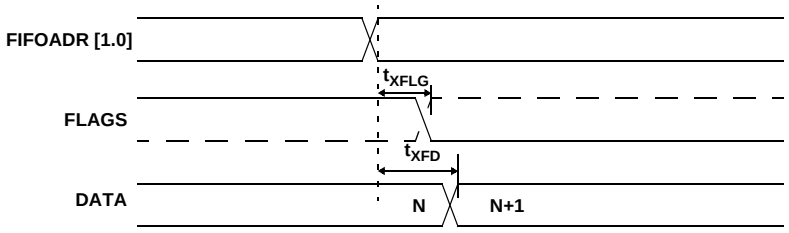



**Table 30. Slave FIFO Address to Flags/Data Parameters**

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{XFLG}$ | FIFOADR[1:0] to FLAGS output propagation delay | – | 10.7 | ns |
| $t_{XFD}$ | FIFOADR[1:0] to FIFODATA output propagation delay | – | 14.3 | ns |

### Slave FIFO Synchronous Address

**Figure 28. Slave FIFO Synchronous Address Timing Diagram[24]**

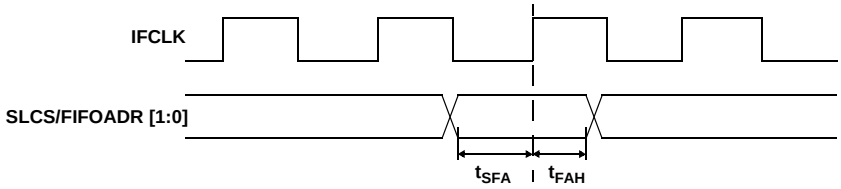



**Table 31. Slave FIFO Synchronous Address Parameters[25]**

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{IFCLK}$ | Interface clock period | 20.83 | 200 | ns |
| $t_{SFA}$ | FIFOADR[1:0] to clock setup time | 25 | – | ns |
| $t_{FAH}$ | Clock to FIFOADR[1:0] hold time | 10 | – | ns |

### Slave FIFO Asynchronous Address

**Figure 29. Slave FIFO Asynchronous Address Timing Diagram[24]**

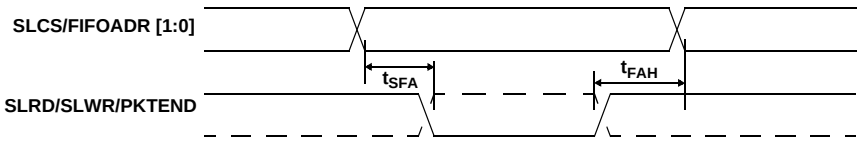



**Table 32. Slave FIFO Asynchronous Address Parameters[27]**

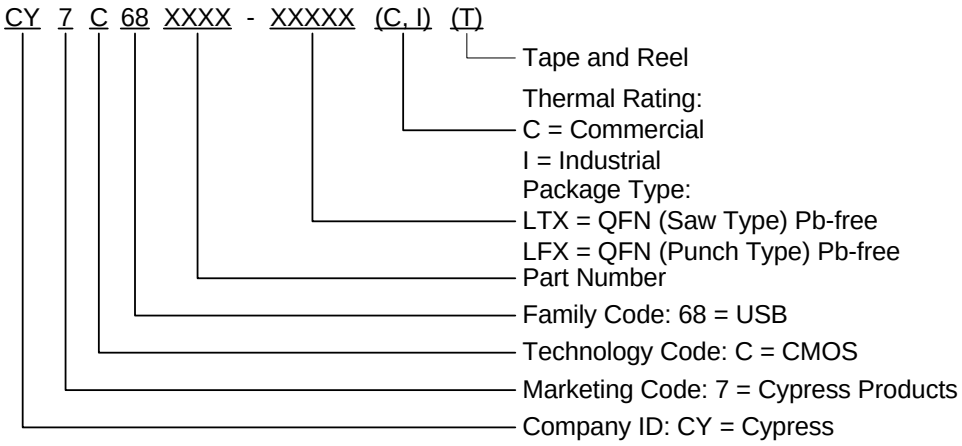
| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{SFA}$ | FIFOADR[1:0] to SLRD/SLWR/PKTEND setup time | 10 | – | ns |
| $t_{FAH}$ | RD/WR/PKTEND to FIFOADR[1:0] hold time | 10 | – | ns |

## Ordering Information

**Table 33. Ordering Information**

| Ordering Code | Package Type | RAM Size | # Prog I/Os | 8051 Address /Data Bus | Serial Debug[28] |
|---|---|---|---|---|---|
| **Ideal for Battery Powered Applications** | | | | | |
| CY7C68014A-128AXC | 128 TQFP – Pb-free | 16 K | 40 | 16-/8-bit | Y |
| CY7C68014A-100AXC | 100 TQFP – Pb-free | 16 K | 40 | – | Y |
| CY7C68014A-56PVXC | 56 SSOP – Pb-free | 16 K | 24 | – | N |
| CY7C68014A-56LTXC | 56 QFN - Pb-free | 16 K | 24 | – | N |
| CY7C68016A-56LTXC | 56 QFN - Pb-free | 16 K | 26 | – | N |
| CY7C68016A-56LTXCT | 56 QFN - Pb-free | 16 K | 26 | – | N |
| **Ideal for Non Battery Powered Applications** | | | | | |
| CY7C68013A-128AXC | 128 TQFP – Pb-free | 16 K | 40 | 16-/8-bit | Y |
| CY7C68013A-128AXI | 128 TQFP – Pb-free (Industrial) | 16 K | 40 | 16-/8-bit | Y |
| CY7C68013A-100AXC | 100 TQFP – Pb-free | 16 K | 40 | – | Y |
| CY7C68013A-100AXI | 100 TQFP – Pb-free (Industrial) | 16 K | 40 | – | Y |
| CY7C68013A-56PVXC | 56 SSOP – Pb-free | 16 K | 24 | – | N |
| CY7C68013A-56PVXCT | 56 SSOP – Pb-free | 16 K | 24 | – | N |
| CY7C68013A-56PVXI | 56 SSOP – Pb-free (Industrial) | 16 K | 24 | – | N |
| CY7C68013A-56BAXC | 56 VFBGA – Pb-free | 16 K | 24 | – | N |
| CY7C68013A-56BAXCT | 56 VFBGA – Pb-free | 16 K | 24 | – | N |
| CY7C68013A-56LTXC | 56 QFN – Pb-free | 16 K | 24 | – | N |
| CY7C68013A-56LTXCT | 56 QFN – Pb-free | 16 K | 24 | – | N |
| CY7C68013A-56LTXI | 56 QFN – Pb-free (Industrial) | 16 K | 24 | – | N |
| CY7C68015A-56LTXC | 56 QFN – Pb-free | 16 K | 26 | – | N |
| **Development Tool Kit** | | | | | |
| CY3684 | EZ-USB FX2LP development kit | | | | |
| **Reference Design Kit** | | | | | |
| CY4611B | USB 2.0 to ATA/ATAPI reference design using EZ-USB FX2LP | | | | |

### Ordering Code Definitions




**Note**
28. As UART is not available in the 56-pin package of CY7C68013A, serial port debugging using Keil Monitor is not possible.

## Package Diagrams

The FX2LP is available in five packages:

- 56-pin SSOP
- 56-pin QFN
- 100-pin TQFP
- 128-pin TQFP
- 56-ball VFBGA

**Figure 36. 56-Pin Shrunk Small Outline Package O56 (51-85062)**

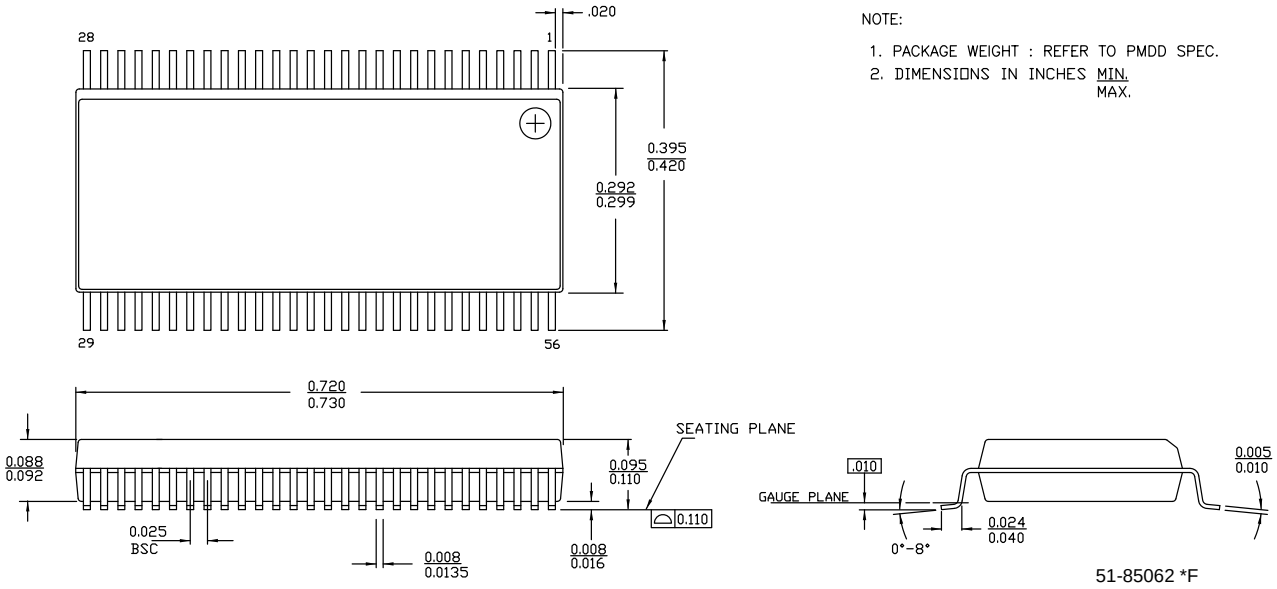


**Figure 38. 100-Pin Thin Plastic Quad Flatpack (14 × 20 × 1.4 mm) A100RA (51-85050)**

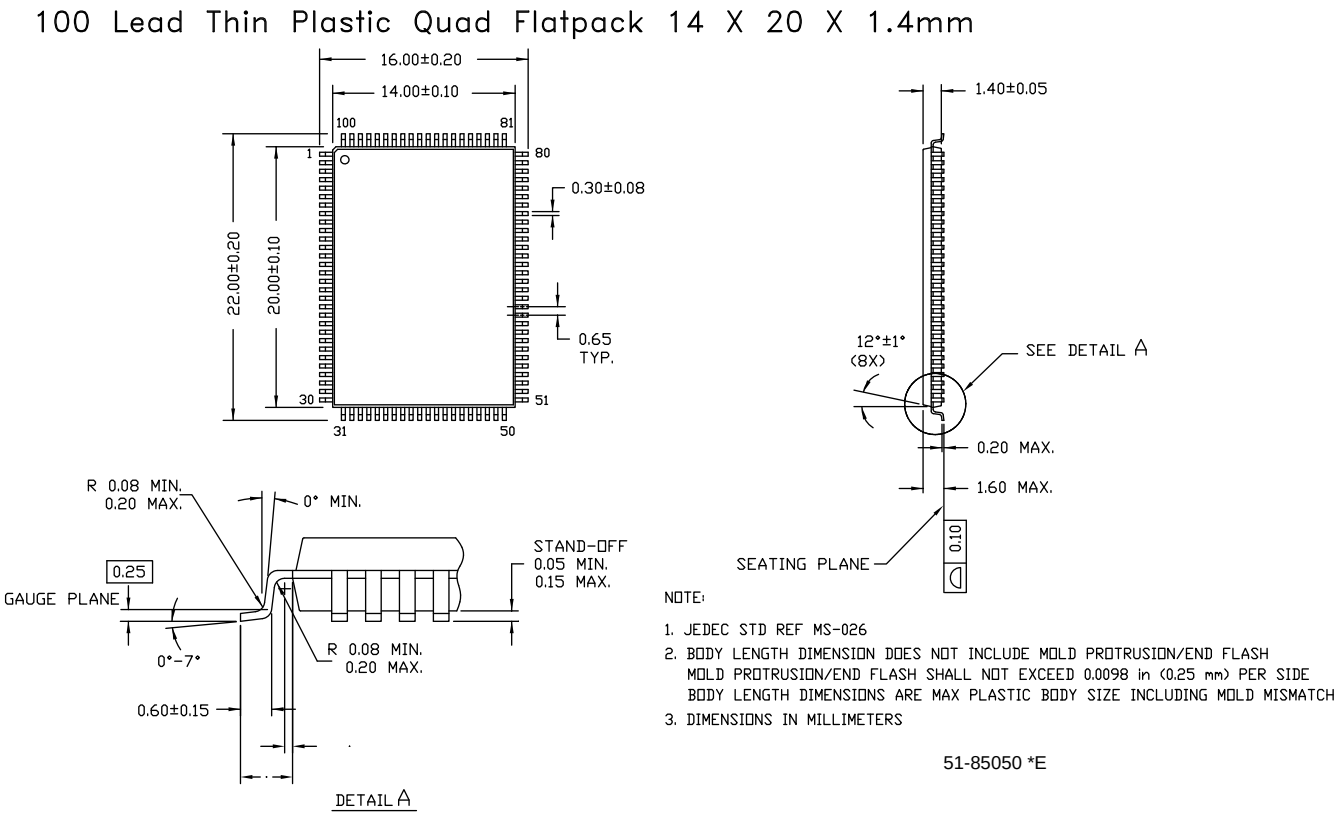
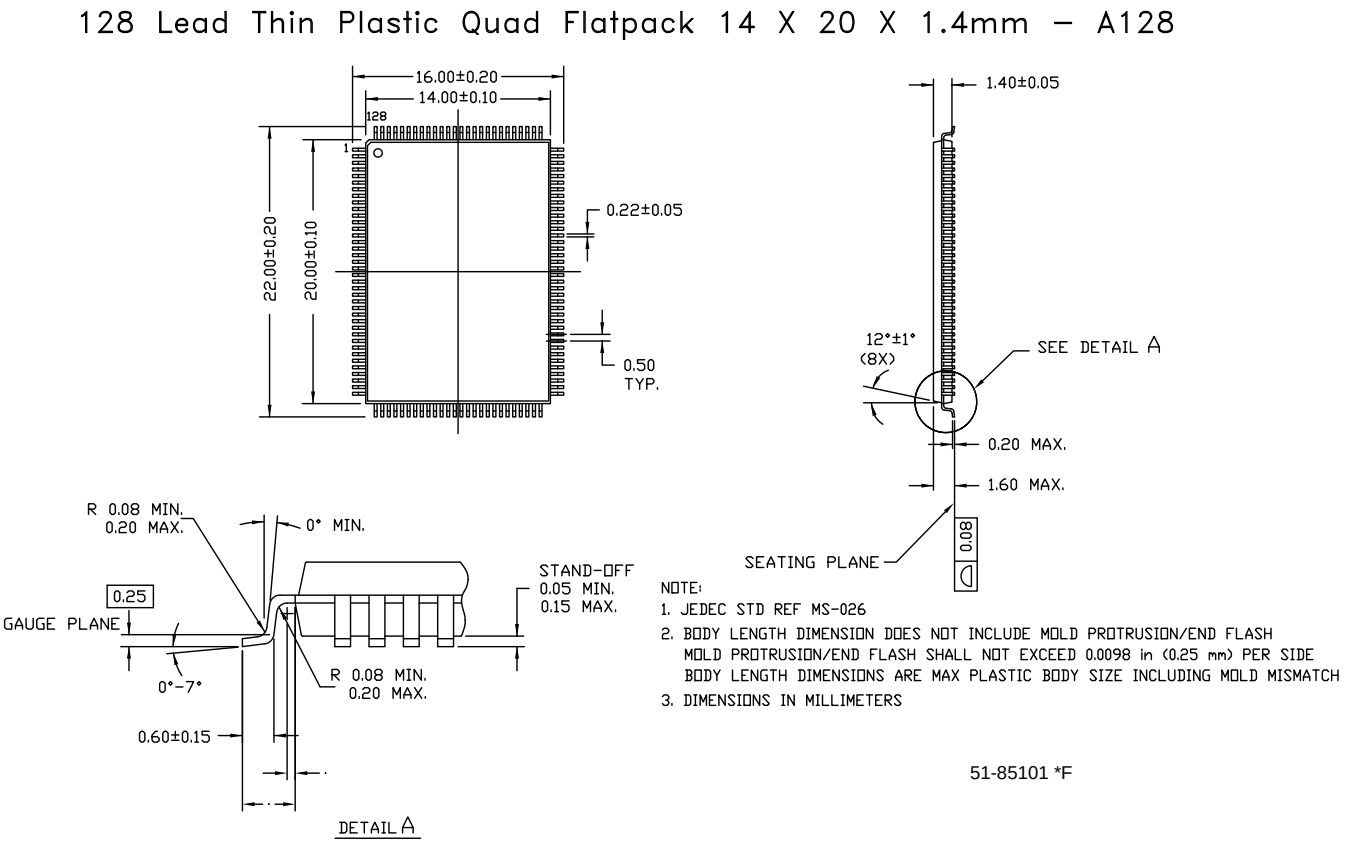


**Figure 39. 128-Pin Thin Plastic Quad Flatpack (14 × 20 × 1.4 mm) A128 (51-85101)**



# Errata

This section describes the errata for the EZ-USB® FX2LP™ CY7C68013A/14A/15A/16A Rev. B silicon. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

## Part Numbers Affected

| Part Number | Package Type | Operating Range |
|---|---|---|
| CY7C68013A | All | Commercial |
| CY7C68014A | All | Commercial |
| CY7C68015A | All | Commercial |
| CY7C68016A | All | Commercial |

## CY7C68013A/14A/15A/16A Qualification Status

In production

## CY7C68013A/14A/15A/16A Errata Summary

This table defines the errata for available CY7C68013A/14A/15A/16A family devices. An "X" indicates that the errata pertain to the selected device.

| Items | CY7C68013A/14A/15A/16A | Silicon Revision | Fix Status |
|---|---|---|---|
| [1.]. Empty Flag Assertion | X | B | No silicon fix planned currently. Use the workaround. |

### 1. Empty Flag Assertion

**■ Problem Definition**

In Slave FIFO Asynchronous Word Wide mode, if a single word data is transferred from the USB host to EP2, configured as OUT Endpoint (EP) in the first transaction, then the Empty flag behaves incorrectly. This does not happen if the data size is more than one word in the first transaction.

**■ Parameters Affected**

NA

**■ Trigger Condition(S)**

In Slave FIFO Asynchronous Word Wide Mode, after firmware boot and initialization, EP2 OUT endpoint empty flag indicates the status as ‘Empty’. When data is received in EP2, the status changes to ‘Not-Empty’. However, if data transferred to EP2 is a single word, then asserting SLRD with FIFOADR pointing to any other endpoint changes ‘Not-Empty’ status to ‘Empty’ for EP2 even though there is a word data (or it is untouched). This is noticed only when the single word is sent as the first transaction and not if it follows a multi-word packet as the first transaction.

**■ Scope of Impact**

External interface does not see data available in EP2 OUT endpoint and can end up waiting for data to be read.

**■ Workaround**

One of the following workarounds can be used:

- Send a pulse signal to the SLWR pin, with FIFOADR pins pointing to an endpoint other than EP2, after firmware initialization and before or after transferring the data to EP2 from the host
- Set the length of the first data to EP2 to be more than a word
- Prioritize EP2 read from the Master for multiple OUT EPs and single word write to EP2
- Write to an IN EP, if any, from the Master before reading from other OUT EPs (other than EP2) from the Master.

**■ Fix Status**

There is no silicon fix planned for this currently; use the workarounds provided.

# Sales, Solutions, and Legal Information

## Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

### Products

| | |
|---|---|
| ARM® Cortex® Microcontrollers | cypress.com/arm |
| Automotive | cypress.com/automotive |
| Clocks & Buffers | cypress.com/clocks |
| Interface | cypress.com/interface |
| Lighting & Power Control | cypress.com/powerpsoc |
| Memory | cypress.com/memory |
| PSoC | cypress.com/psoc |
| Touch Sensing | cypress.com/touch |
| USB Controllers | cypress.com/usb |
| Wireless/RF | cypress.com/wireless |

### PSoC®Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

### Cypress Developer Community

Forums | Projects | Video | Blogs | Training | Components

### Technical Support

cypress.com/support