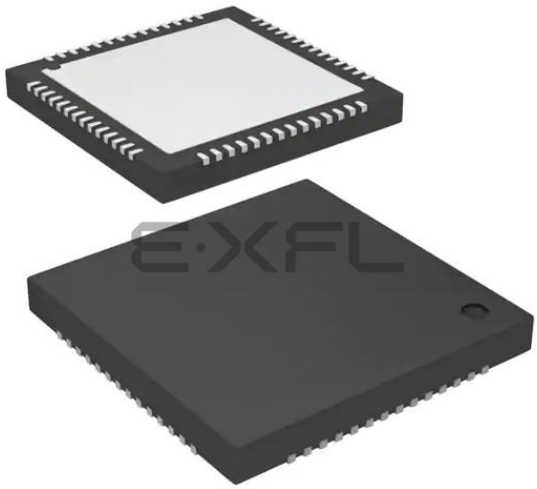

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## Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

**Embedded - Microcontrollers - Application Specific** represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

## What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

| Details | |
|---|---|
| Product Status | Active |
| Applications | USB Microcontroller |
| Core Processor | 8051 |
| Program Memory Type | ROMless |
| Controller Series | CY7C680xx |
| RAM Size | 16K x 8 |
| Interface | I²C, USB, USART |
| Number of I/O | 24 |
| Voltage - Supply | 3V ~ 3.6V |
| Operating Temperature | 0°C ~ 70°C |
| Mounting Type | Surface Mount |
| Package / Case | 56-VFQFN Exposed Pad |
| Supplier Device Package | 56-QFN (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/cy7c68013a-56ltxct |

## Applications

- Portable video recorder
- MPEG/TV conversion
- DSL modems
- ATA interface
- Memory card readers
- Legacy conversion devices
- Cameras
- Scanners
- Wireless LAN
- MP3 players
- Networking

The “Reference Designs” section of the Cypress web site provides additional tools for typical USB 2.0 applications. Each reference design comes complete with firmware source and object code, schematics, and documentation. Visit www.cypress.com for more information.

## Functional Overview

### USB Signaling Speed

FX2LP operates at two of the three rates defined in the USB Specification Revision 2.0, dated April 27, 2000:

- Full speed, with a signaling bit rate of 12 Mbps
- High speed, with a signaling bit rate of 480 Mbps

FX2LP does not support the Low Speed signaling mode of 1.5 Mbps.

### 8051 Microprocessor

The 8051 microprocessor embedded in the FX2LP family has 256 bytes of register RAM, an expanded interrupt system, three timer/counters, and two USARTs.

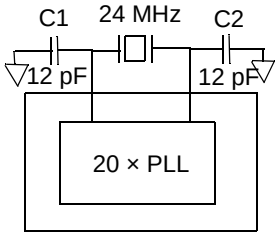
*8051 Clock Frequency*

FX2LP has an on-chip oscillator circuit that uses an external 24-MHz (±100 ppm) crystal with the following characteristics:

- Parallel resonant
- Fundamental mode
- 500-µW drive level
- 12-pF (5% tolerance) load capacitors

An on-chip PLL multiplies the 24-MHz oscillator up to 480 MHz, as required by the transceiver/PHY; internal counters divide it down for use as the 8051 clock. The default 8051 clock frequency is 12 MHz. The clock frequency of the 8051 can be changed by the 8051 through the CPUCS register, dynamically.

**Figure 1. Crystal Configuration**




12-pF capacitor values assume a trace capacitance of 3 pF per side on a four-layer FR4 PCA

The CLKOUT pin, which can be three-stated and inverted using internal control bits, outputs the 50% duty cycle 8051 clock, at the selected 8051 clock frequency: 48 MHz, 24 MHz, or 12 MHz.

*USARTs*

FX2LP contains two standard 8051 USARTs, addressed through Special Function Register (SFR) bits. The USART interface pins are available on separate I/O pins, and are not multiplexed with port pins.

UART0 and UART1 can operate using an internal clock at 230 KBaud with no more than 1% baud rate error. 230 KBaud operation is achieved by an internally derived clock source that generates overflow pulses at the appropriate time. The internal clock adjusts for the 8051 clock rate (48 MHz, 24 MHz, and 12 MHz) such that it always presents the correct frequency for the 230-KBaud operation.[1]

*Special Function Registers*

Certain 8051 SFR addresses are populated to provide fast access to critical FX2LP functions. These SFR additions are shown in Table 1 on page 6. Bold type indicates nonstandard, enhanced 8051 registers. The two SFR rows that end with “0” and “8” contain bit-addressable registers. The four I/O ports A to D use the SFR addresses used in the standard 8051 for ports 0 to 3, which are not implemented in FX2LP. Because of the faster and more efficient SFR addressing, the FX2LP I/O ports are not addressable in external RAM space (using the MOVX instruction).

### $I^2C$ Bus

FX2LP supports the $I^2C$ bus as a master only at 100/400 kHz. SCL and SDA pins have open-drain outputs and hysteresis inputs. These signals must be pulled up to 3.3 V, even if no $I^2C$ device is connected.

### Buses

All packages, 8-bit or 16-bit “FIFO” bidirectional data bus, multiplexed on I/O ports B and D. 128-pin package: adds 16-bit output-only 8051 address bus, 8-bit bidirectional data bus.

**Note**
1. 115-KBaud operation is also possible by programming the 8051 SMOD0 or SMOD1 bits to a “1” for UART0, UART1, or both respectively.

*Default Full-Speed Alternate Settings*

**Table 6. Default Full Speed Alternate Settings**[5, 6]

| Alternate Setting | 0 | 1 | 2 | 3 |
|---|---|---|---|---|
| ep0 | 64 | 64 | 64 | 64 |
| ep1out | 0 | 64 bulk | 64 int | 64 int |
| ep1in | 0 | 64 bulk | 64 int | 64 int |
| ep2 | 0 | 64 bulk out (2×) | 64 int out (2×) | 64 iso out (2×) |
| ep4 | 0 | 64 bulk out (2×) | 64 bulk out (2×) | 64 bulk out (2×) |
| ep6 | 0 | 64 bulk in (2×) | 64 int in (2×) | 64 iso in (2×) |
| ep8 | 0 | 64 bulk in (2×) | 64 bulk in (2×) | 64 bulk in (2×) |

*Default High Speed Alternate Settings*

**Table 7. Default Hi-Speed Alternate Settings**[5, 6]

| Alternate Setting | 0 | 1 | 2 | 3 |
|---|---|---|---|---|
| ep0 | 64 | 64 | 64 | 64 |
| ep1out | 0 | 512 bulk[7] | 64 int | 64 int |
| ep1in | 0 | 512 bulk[7] | 64 int | 64 int |
| ep2 | 0 | 512 bulk out (2×) | 512 int out (2×) | 512 iso out (2×) |
| ep4 | 0 | 512 bulk out (2×) | 512 bulk out (2×) | 512 bulk out (2×) |
| ep6 | 0 | 512 bulk in (2×) | 512 int in (2×) | 512 iso in (2×) |
| ep8 | 0 | 512 bulk in (2×) | 512 bulk in (2×) | 512 bulk in (2×) |

## External FIFO Interface

*Architecture*

The FX2LP slave FIFO architecture has eight 512-byte blocks in the endpoint RAM that directly serve as FIFO memories and are controlled by FIFO control signals (such as IFCLK, SLCS#, SLRD, SLWR, SLOE, PKTEND, and flags).

In operation, some of the eight RAM blocks fill or empty from the SIE, while the others are connected to the I/O transfer logic. The transfer logic takes two forms: the GPIF for internally generated control signals and the slave FIFO interface for externally controlled transfers.

*Master/Slave Control Signals*

The FX2LP endpoint FIFOs are implemented as eight physically distinct 256×16 RAM blocks. The 8051/SIE can switch any of the RAM blocks between two domains, the USB (SIE) domain and the 8051-I/O Unit domain. This switching is done virtually instantaneously, giving essentially zero transfer time between "USB FIFOs" and "Slave FIFOs." Because they are physically the same memory, no bytes are actually transferred between buffers.

At any time, some RAM blocks are filling/emptying with the USB data under SIE control, while other RAM blocks are available to the 8051, the I/O control unit, or both. The RAM blocks operates as single-port in the USB domain, and dual-port in the 8051-I/O domain. The blocks can be configured as single-, double-, triple-, or quad-buffered as previously shown.

The I/O control unit implements either an internal master (M for Master) or external master (S for Slave) interface.

In Master (M) mode, the GPIF internally controls FIFOADR[1..0] to select a FIFO. The RDY pins (two in the 56-pin package, six in the 100-pin and 128-pin packages) can be used as flag inputs from an external FIFO or other logic if desired. The GPIF can be run from either an internally derived clock or externally supplied clock (IFCLK), at a rate that transfers data up to 96 MBytes/s (48

**Notes**
5. "0" means "not implemented."
6. "2×" means "double buffered."
7. Even though these buffers are 64 bytes, they are reported as 512 for USB 2.0 compliance. The user must never transfer packets larger than 64 bytes to EP1.

## Autopointer Access

FX2LP provides two identical autopointers. They are similar to the internal 8051 data pointers but with an additional feature: they can optionally increment after every memory access. This capability is available to and from both internal and external RAM. Autopointers are available in external FX2LP registers under the control of a mode bit (AUTOPTRSET-UP.0). Using the external FX2LP autopointer access (at 0xE67B – 0xE67C) enables the autopointer to access all internal and external RAM to the part.

Also, autopointers can point to any FX2LP register or endpoint buffer space. When the autopointer access to external memory is enabled, locations 0xE67B and 0xE67C in XDATA and code space cannot be used.

## I²C Controller

FX2LP has one I²C port that is driven by two internal controllers, the one that automatically operates at boot time to load VID/PID/DID and configuration information, and another that the 8051 uses when running to control external I²C devices. The I²C port operates in master mode only.

### *I²C Port Pins*

The I²C pins SCL and SDA must have external 2.2-kΩ pull-up resistors even if no EEPROM is connected to the FX2LP. External EEPROM device address pins must be configured properly. See Table 8 for configuring the device address pins.

**Table 8. Strap Boot EEPROM Address Lines to These Values**

| Bytes | Example EEPROM | A2 | A1 | A0 |
|---|---|---|---|---|
| 16 | 24LC00[10] | N/A | N/A | N/A |
| 128 | 24LC01 | 0 | 0 | 0 |
| 256 | 24LC02 | 0 | 0 | 0 |
| 4K | 24LC32 | 0 | 0 | 1 |
| 8K | 24LC64 | 0 | 0 | 1 |
| 16K | 24LC128 | 0 | 0 | 1 |

### *I²C Interface Boot Load Access*

At power-on reset, the I²C interface boot loader loads the VID/PID/DID configuration bytes and up to 16 KB of program/data. The available RAM spaces are 16 KB from 0x0000–0x3FFF and 512 bytes from 0xE000–0xE1FF. The 8051 is in reset. I²C interface boot loads only occur after power-on reset.

### *I²C Interface General-Purpose Access*

The 8051 can control peripherals connected to the I²C bus using the I2CTL and I2DAT registers. FX2LP provides I²C master control only; it is never an I²C slave.

## Compatible with Previous Generation EZ-USB FX2

The EZ-USB FX2LP is form-, fit-, and with minor exceptions, functionally-compatible with its predecessor, the EZ-USB FX2.

This makes for an easy transition for designers wanting to upgrade their systems from the FX2 to the FX2LP. The pinout and package selection are identical and a vast majority of firmware previously developed for the FX2 functions in the FX2LP.

For designers migrating from the FX2 to the FX2LP, a change in the bill of material and review of the memory allocation (due to increased internal memory) is required. For more information about migrating from EZ-USB FX2 to EZ-USB FX2LP, see the application note titled *Migrating from EZ-USB FX2 to EZ-USB FX2LP* available in the Cypress web site.

**Table 9. Part Number Conversion Table**

| EZ-USB FX2 Part Number | EZ-USB FX2LP Part Number | Package Description |
|---|---|---|
| CY7C68013-56PVC | CY7C68013A-56PVXC or CY7C68014A-56PVXC | 56-pin SSOP |
| CY7C68013-56PVCT | CY7C68013A-56PVXCT or CY7C68014A-56PVXCT | 56-pin SSOP – Tape and Reel |
| CY7C68013-56LFC | CY7C68013A-56LFXC or CY7C68014A-56LFXC | 56-pin QFN |
| CY7C68013-100AC | CY7C68013A-100AXC or CY7C68014A-100AXC | 100-pin TQFP |
| CY7C68013-128AC | CY7C68013A-128AXC or CY7C68014A-128AXC | 128-pin TQFP |

## CY7C68013A/14A and CY7C68015A/16A Differences

CY7C68013A is identical to CY7C68014A in form, fit, and functionality. CY7C68015A is identical to CY7C68016A in form, fit, and functionality. CY7C68014A and CY7C68016A have a lower suspend current than CY7C68013A and CY7C68015A respectively and are ideal for power-sensitive battery applications.

CY7C68015A and CY7C68016A are available in 56-pin QFN package only. Two additional GPIO signals are available on the CY7C68015A and CY7C68016A to provide more flexibility when neither IFCLK or CLKOUT are needed in the 56-pin package.

USB developers wanting to convert their FX2 56-pin application to a bus-powered system directly benefit from these additional signals. The two GPIOs give developers the signals they need for the power-control circuitry of their bus-powered application without pushing them to a high-pincount version of FX2LP.

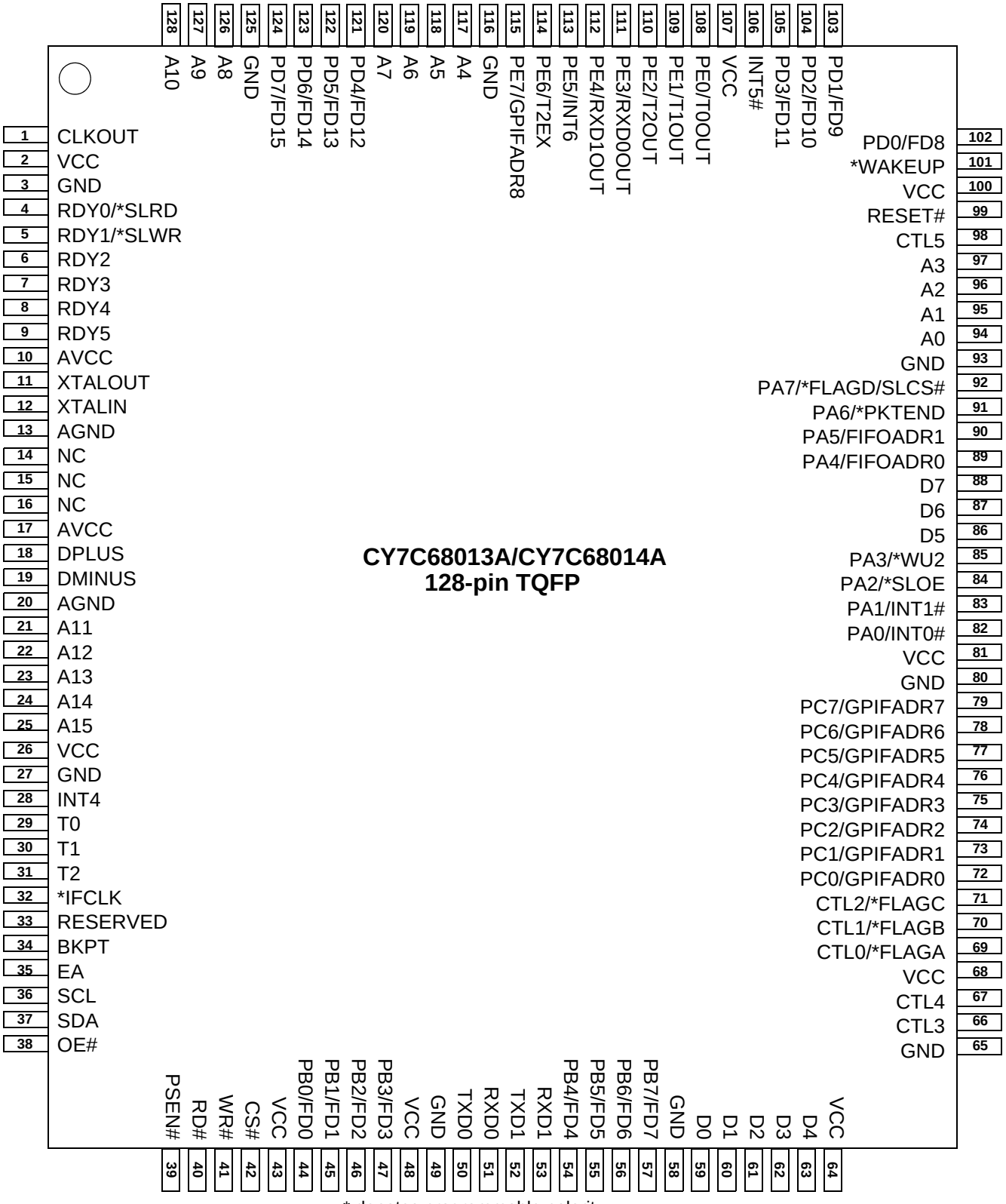
The CY7C68015A is only available in the 56-pin QFN package

**Table 10. CY7C68013A/14A and CY7C68015A/16A Pin Differences**

| CY7C68013A/CY7C68014A | CY7C68015A/CY7C68016A |
|---|---|
| IFCLK | PE0 |
| CLKOUT | PE1 |

**Note**
10. This EEPROM does not have address pins.

**Figure 7. CY7C68013A/CY7C68014A 128-Pin TQFP Pin Assignment**




* denotes programmable polarity

**Table 11. FX2LP Pin Descriptions**[11] (continued)

| 128 TQFP | 100 TQFP | 56 SSOP | 56 QFN | 56 VFBGA | Name | Type | Default | Reset[12] | Description |
|---|---|---|---|---|---|---|---|---|---|
| 30 | 24 | – | – | – | T1 | Input | N/A | N/A | **T1** is the active HIGH T1 signal for 8051 Timer1, which provides the input to Timer1 when C/T1 is 1. When C/T1 is 0, Timer1 does not use this bit. |
| 29 | 23 | – | – | – | T0 | Input | N/A | N/A | **T0** is the active HIGH T0 signal for 8051 Timer0, which provides the input to Timer0 when C/T0 is 1. When C/T0 is 0, Timer0 does not use this bit. |
| 53 | 43 | – | – | – | RXD1 | Input | N/A | N/A | **RXD1**is an active HIGH input signal for 8051 UART1, which provides data to the UART in all modes. |
| 52 | 42 | – | – | – | TXD1 | Output | H | L | **TXD1**is an active HIGH output pin from 8051 UART1, which provides the output clock in sync mode, and the output data in async mode. |
| 51 | 41 | – | – | – | RXD0 | Input | N/A | N/A | **RXD0** is the active HIGH RXD0 input to 8051 UART0, which provides data to the UART in all modes. |
| 50 | 40 | – | – | – | TXD0 | Output | H | L | **TXD0** is the active HIGH TXD0 output from 8051 UART0, which provides the output clock in sync mode, and the output data in async mode. |
| 42 | | – | – | – | CS# | Output | H | H | **CS#** is the active LOW chip select for external memory. |
| 41 | 32 | – | – | – | WR# | Output | H | H | **WR#** is the active LOW write strobe output for external memory. |
| 40 | 31 | – | – | – | RD# | Output | H | H | **RD#** is the active LOW read strobe output for external memory. |
| 38 | | – | – | – | OE# | Output | H | H | **OE#** is the active LOW output enable for external memory. |
| | | | | | | | | | |
| 33 | 27 | 21 | 14 | 2H | Reserved | Input | N/A | N/A | **Reserved**. Connect to ground. |
| | | | | | | | | | |
| 101 | 79 | 51 | 44 | 7B | WAKEUP | Input | N/A | N/A | **USB Wakeup**. If the 8051 is in suspend, asserting this pin starts up the oscillator and interrupts the 8051 to enable it to exit the suspend mode. Holding WAKEUP asserted inhibits the EZ-USB chip from suspending. This pin has programmable polarity (WAKEUP.4). |
| 36 | 29 | 22 | 15 | 3F | SCL | OD | Z | Z (if booting is done) | **Clock** for the $I^2C$ interface. Connect to VCC with a 2.2-kΩ resistor, even if no $I^2C$ peripheral is attached. |
| 37 | 30 | 23 | 16 | 3G | SDA | OD | Z | Z (if booting is done) | **Data** for **$I^2C$ compatible interface**. Connect to VCC with a 2.2-kΩ resistor, **even if no $I^2C$ compatible peripheral is attached**. |
| | | | | | | | | | |
| 2 | 1 | 6 | 55 | 5A | VCC | Power | N/A | N/A | **VCC**. Connect to the 3.3-V power source. |
| 26 | 20 | 18 | 11 | 1G | VCC | Power | N/A | N/A | **VCC**. Connect to the 3.3-V power source. |
| 43 | 33 | 24 | 17 | 7E | VCC | Power | N/A | N/A | **VCC**. Connect to the 3.3-V power source. |
| 48 | 38 | – | – | – | VCC | Power | N/A | N/A | **VCC**. Connect to 3.3-V power source. |
| 64 | 49 | 34 | 27 | 8E | VCC | Power | N/A | N/A | **VCC**. Connect to the 3.3-V power source. |
| 68 | 53 | – | – | – | VCC | Power | N/A | N/A | **VCC**. Connect to the 3.3-V power source. |
| 81 | 66 | 39 | 32 | 5C | VCC | Power | N/A | N/A | **VCC**. Connect to the 3.3-V power source. |

**Table 12. FX2LP Register Summary** (continued)

| Hex | Size | Name | Description | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Default | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E62B | 1 | ECC1B1 | ECC1 Byte 1 Address | LINE7 | LINE6 | LINE5 | LINE4 | LINE3 | LINE2 | LINE1 | LINE0 | 00000000 | R |
| E62C | 1 | ECC1B2 | ECC1 Byte 2 Address | COL5 | COL4 | COL3 | COL2 | COL1 | COL0 | LINE17 | LINE16 | 00000000 | R |
| E62D | 1 | ECC2B0 | ECC2 Byte 0 Address | LINE15 | LINE14 | LINE13 | LINE12 | LINE11 | LINE10 | LINE9 | LINE8 | 00000000 | R |
| E62E | 1 | ECC2B1 | ECC2 Byte 1 Address | LINE7 | LINE6 | LINE5 | LINE4 | LINE3 | LINE2 | LINE1 | LINE0 | 00000000 | R |
| E62F | 1 | ECC2B2 | ECC2 Byte 2 Address | COL5 | COL4 | COL3 | COL2 | COL1 | COL0 | 0 | 0 | 00000000 | R |
| E630 H.S. | 1 | EP2FIFOPFH[13] | Endpoint 2 / slave FIFO Programmable Flag H | DECIS | PKTSTAT | IN:PKTS[2] OUT:PFC12 | IN:PKTS[1] OUT:PFC11 | IN:PKTS[0] OUT:PFC10 | 0 | PFC9 | PFC8 | 10001000 | bbbbbrbb |
| E630 F.S. | 1 | EP2FIFOPFH[13] | Endpoint 2 / slave FIFO Programmable Flag H | DECIS | PKTSTAT | OUT:PFC12 | OUT:PFC11 | OUT:PFC10 | 0 | PFC9 | IN:PKTS[2] OUT:PFC8 | 10001000 | bbbbbrbb |
| E631 H.S. | 1 | EP2FIFOPFL[13] | Endpoint 2 / slave FIFO Programmable Flag L | PFC7 | PFC6 | PFC5 | PFC4 | PFC3 | PFC2 | PFC1 | PFC0 | 00000000 | RW |
| E631 F.S | 1 | EP2FIFOPFL[13] | Endpoint 2 / slave FIFO Programmable Flag L | IN:PKTS[1] OUT:PFC7 | IN:PKTS[0] OUT:PFC6 | PFC5 | PFC4 | PFC3 | PFC2 | PFC1 | PFC0 | 00000000 | RW |
| E632 H.S. | 1 | EP4FIFOPFH[13] | Endpoint 4 / slave FIFO Programmable Flag H | DECIS | PKTSTAT | 0 | IN: PKTS[1] OUT:PFC10 | IN: PKTS[0] OUT:PFC9 | 0 | 0 | PFC8 | 10001000 | bbrbbrrb |
| E632 F.S | 1 | EP4FIFOPFH[13] | Endpoint 4 / slave FIFO Programmable Flag H | DECIS | PKTSTAT | 0 | OUT:PFC10 | OUT:PFC9 | 0 | 0 | PFC8 | 10001000 | bbrbbrrb |
| E633 H.S. | 1 | EP4FIFOPFL[13] | Endpoint 4 / slave FIFO Programmable Flag L | PFC7 | PFC6 | PFC5 | PFC4 | PFC3 | PFC2 | PFC1 | PFC0 | 00000000 | RW |
| E633 F.S | 1 | EP4FIFOPFL[13] | Endpoint 4 / slave FIFO Programmable Flag L | IN: PKTS[1] OUT:PFC7 | IN: PKTS[0] OUT:PFC6 | PFC5 | PFC4 | PFC3 | PFC2 | PFC1 | PFC0 | 00000000 | RW |
| E634 H.S. | 1 | EP6FIFOPFH[13] | Endpoint 6 / slave FIFO Programmable Flag H | DECIS | PKTSTAT | IN:PKTS[2] OUT:PFC12 | IN:PKTS[1] OUT:PFC11 | IN:PKTS[0] OUT:PFC10 | 0 | PFC9 | PFC8 | 00001000 | bbbbbrbb |
| E634 F.S | 1 | EP6FIFOPFH[13] | Endpoint 6 / slave FIFO Programmable Flag H | DECIS | PKTSTAT | OUT:PFC12 | OUT:PFC11 | OUT:PFC10 | 0 | PFC9 | IN:PKTS[2] OUT:PFC8 | 00001000 | bbbbbrbb |
| E635 H.S. | 1 | EP6FIFOPFL[13] | Endpoint 6 / slave FIFO Programmable Flag L | PFC7 | PFC6 | PFC5 | PFC4 | PFC3 | PFC2 | PFC1 | PFC0 | 00000000 | RW |
| E635 F.S | 1 | EP6FIFOPFL[13] | Endpoint 6 / slave FIFO Programmable Flag L | IN:PKTS[1] OUT:PFC7 | IN:PKTS[0] OUT:PFC6 | PFC5 | PFC4 | PFC3 | PFC2 | PFC1 | PFC0 | 00000000 | RW |
| E636 H.S. | 1 | EP8FIFOPFH[13] | Endpoint 8 / slave FIFO Programmable Flag H | DECIS | PKTSTAT | 0 | IN: PKTS[1] OUT:PFC10 | IN: PKTS[0] OUT:PFC9 | 0 | 0 | PFC8 | 00001000 | bbrbbrrb |
| E636 F.S | 1 | EP8FIFOPFH[13] | Endpoint 8 / slave FIFO Programmable Flag H | DECIS | PKTSTAT | 0 | OUT:PFC10 | OUT:PFC9 | 0 | 0 | PFC8 | 00001000 | bbrbbrrb |
| E637 H.S. | 1 | EP8FIFOPFL[13] | Endpoint 8 / slave FIFO Programmable Flag L | PFC7 | PFC6 | PFC5 | PFC4 | PFC3 | PFC2 | PFC1 | PFC0 | 00000000 | RW |
| E637 F.S | 1 | EP8FIFOPFL[13] | Endpoint 8 / slave FIFO Programmable Flag L | IN: PKTS[1] OUT:PFC7 | IN: PKTS[0] OUT:PFC6 | PFC5 | PFC4 | PFC3 | PFC2 | PFC1 | PFC0 | 00000000 | RW |
| | 8 | reserved | | | | | | | | | | | |
| E640 | 1 | EP2ISOINPKTS | EP2 (if ISO) IN Packets per frame (1-3) | AADJ | 0 | 0 | 0 | 0 | 0 | INPPF1 | INPPF0 | 00000001 | brrrrrbb |
| E641 | 1 | EP4ISOINPKTS | EP4 (if ISO) IN Packets per frame (1-3) | AADJ | 0 | 0 | 0 | 0 | 0 | INPPF1 | INPPF0 | 00000001 | brrrrrrr |
| E642 | 1 | EP6ISOINPKTS | EP6 (if ISO) IN Packets per frame (1-3) | AADJ | 0 | 0 | 0 | 0 | 0 | INPPF1 | INPPF0 | 00000001 | brrrrrbb |
| E643 | 1 | EP8ISOINPKTS | EP8 (if ISO) IN Packets per frame (1-3) | AADJ | 0 | 0 | 0 | 0 | 0 | INPPF1 | INPPF0 | 00000001 | brrrrrrr |
| E644 | 4 | reserved | | | | | | | | | | | |
| E648 | 1 | INPKTEND[13] | Force IN Packet End | Skip | 0 | 0 | 0 | EP3 | EP2 | EP1 | EP0 | xxxxxxxx | W |
| E649 | 7 | OUTPKTEND[13] | Force OUT Packet End | Skip | 0 | 0 | 0 | EP3 | EP2 | EP1 | EP0 | xxxxxxxx | W |
| | | INTERRUPTS | | | | | | | | | | | |
| E650 | 1 | EP2FIFOIE[13] | Endpoint 2 slave FIFO Flag Interrupt Enable | 0 | 0 | 0 | 0 | EDGEPF | PF | EF | FF | 00000000 | RW |
| E651 | 1 | EP2FIFOIRQ[13,14] | Endpoint 2 slave FIFO Flag Interrupt Request | 0 | 0 | 0 | 0 | 0 | PF | EF | FF | 00000000 | rrrrrbbb |
| E652 | 1 | EP4FIFOIE[13] | Endpoint 4 slave FIFO Flag Interrupt Enable | 0 | 0 | 0 | 0 | EDGEPF | PF | EF | FF | 00000000 | RW |
| E653 | 1 | EP4FIFOIRQ[13,14] | Endpoint 4 slave FIFO Flag Interrupt Request | 0 | 0 | 0 | 0 | 0 | PF | EF | FF | 00000000 | rrrrrbbb |
| E654 | 1 | EP6FIFOIE[13] | Endpoint 6 slave FIFO Flag Interrupt Enable | 0 | 0 | 0 | 0 | EDGEPF | PF | EF | FF | 00000000 | RW |
| E655 | 1 | EP6FIFOIRQ[13,14] | Endpoint 6 slave FIFO Flag Interrupt Request | 0 | 0 | 0 | 0 | 0 | PF | EF | FF | 00000000 | rrrrrbbb |
| E656 | 1 | EP8FIFOIE[13] | Endpoint 8 slave FIFO Flag Interrupt Enable | 0 | 0 | 0 | 0 | EDGEPF | PF | EF | FF | 00000000 | RW |
| E657 | 1 | EP8FIFOIRQ[13,14] | Endpoint 8 slave FIFO Flag Interrupt Request | 0 | 0 | 0 | 0 | 0 | PF | EF | FF | 00000000 | rrrrrbbb |
| E658 | 1 | IBNIE | IN-BULK-NAK Interrupt Enable | 0 | 0 | EP8 | EP6 | EP4 | EP2 | EP1 | EP0 | 00000000 | RW |
| E659 | 1 | IBNIRQ[14] | IN-BULK-NAK interrupt Request | 0 | 0 | EP8 | EP6 | EP4 | EP2 | EP1 | EP0 | 00xxxxxx | rrbbbbbb |
| E65A | 1 | NAKIE | Endpoint Ping-NAK / IBN Interrupt Enable | EP8 | EP6 | EP4 | EP2 | EP1 | EP0 | 0 | IBN | 00000000 | RW |
| E65B | 1 | NAKIRQ[14] | Endpoint Ping-NAK / IBN Interrupt Request | EP8 | EP6 | EP4 | EP2 | EP1 | EP0 | 0 | IBN | xxxxxx0x | bbbbbbrb |
| E65C | 1 | USBIE | USB Int Enables | 0 | EP0ACK | HSGRANT | URES | SUSP | SUTOK | SOF | SUDAV | 00000000 | RW |

**Note**
14. The register can only be reset; it cannot be set.

**Table 12. FX2LP Register Summary** (continued)

| Hex | Size | Name | Description | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Default | Access |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E6CF | 1 | GPIFTCB2[13] | GPIF Transaction Count Byte 2 | TC23 | TC22 | TC21 | TC20 | TC19 | TC18 | TC17 | TC16 | 00000000 | RW |
| E6D0 | 1 | GPIFTCB1[13] | GPIF Transaction Count Byte 1 | TC15 | TC14 | TC13 | TC12 | TC11 | TC10 | TC9 | TC8 | 00000000 | RW |
| E6D1 | 1 | GPIFTCB0[13] | GPIF Transaction Count Byte 0 | TC7 | TC6 | TC5 | TC4 | TC3 | TC2 | TC1 | TC0 | 00000001 | RW |
| | 2 | reserved | | | | | | | | | | 00000000 | RW |
| | | reserved | | | | | | | | | | | |
| | | reserved | | | | | | | | | | | |
| E6D2 | 1 | EP2GPIFFLGSEL[13] | Endpoint 2 GPIF Flag select | 0 | 0 | 0 | 0 | 0 | 0 | FS1 | FS0 | 00000000 | RW |
| E6D3 | 1 | EP2GPIFPFSTOP | Endpoint 2 GPIF stop transaction on prog. flag | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FIFO2FLAG | 00000000 | RW |
| E6D4 | 1 | EP2GPIFTRIG[13] | Endpoint 2 GPIF Trigger | x | x | x | x | x | x | x | x | xxxxxxxx | W |
| | 3 | reserved | | | | | | | | | | | |
| | | reserved | | | | | | | | | | | |
| | | reserved | | | | | | | | | | | |
| E6DA | 1 | EP4GPIFFLGSEL[13] | Endpoint 4 GPIF Flag select | 0 | 0 | 0 | 0 | 0 | 0 | FS1 | FS0 | 00000000 | RW |
| E6DB | 1 | EP4GPIFPFSTOP | Endpoint 4 GPIF stop transaction on GPIF Flag | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FIFO4FLAG | 00000000 | RW |
| E6DC | 1 | EP4GPIFTRIG[13] | Endpoint 4 GPIF Trigger | x | x | x | x | x | x | x | x | xxxxxxxx | W |
| | 3 | reserved | | | | | | | | | | | |
| | | reserved | | | | | | | | | | | |
| | | reserved | | | | | | | | | | | |
| E6E2 | 1 | EP6GPIFFLGSEL[13] | Endpoint 6 GPIF Flag select | 0 | 0 | 0 | 0 | 0 | 0 | FS1 | FS0 | 00000000 | RW |
| E6E3 | 1 | EP6GPIFPFSTOP | Endpoint 6 GPIF stop transaction on prog. flag | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FIFO6FLAG | 00000000 | RW |
| E6E4 | 1 | EP6GPIFTRIG[13] | Endpoint 6 GPIF Trigger | x | x | x | x | x | x | x | x | xxxxxxxx | W |
| | 3 | reserved | | | | | | | | | | | |
| | | reserved | | | | | | | | | | | |
| | | reserved | | | | | | | | | | | |
| E6EA | 1 | EP8GPIFFLGSEL[13] | Endpoint 8 GPIF Flag select | 0 | 0 | 0 | 0 | 0 | 0 | FS1 | FS0 | 00000000 | RW |
| E6EB | 1 | EP8GPIFPFSTOP | Endpoint 8 GPIF stop transaction on prog. flag | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FIFO8FLAG | 00000000 | RW |
| E6EC | 1 | EP8GPIFTRIG[13] | Endpoint 8 GPIF Trigger | x | x | x | x | x | x | x | x | xxxxxxxx | W |
| | 3 | reserved | | | | | | | | | | | |
| E6F0 | 1 | XGPIFSGLDATH | GPIF Data H (16-bit mode only) | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | xxxxxxxx | RW |
| E6F1 | 1 | XGPIFSGLDATLX | Read/Write GPIF Data L & trigger transaction | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| E6F2 | 1 | XGPIFSGLDATLNOX | Read GPIF Data L, no transaction trigger | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | R |
| E6F3 | 1 | GPIFREADYCFG | Internal RDY, Sync/Async, RDY pin states | INTRDY | SAS | TCXRDY5 | 0 | 0 | 0 | 0 | 0 | 00000000 | bbbrrrrr |
| | | | | | | | | | | | | | |
| E6F4 | 1 | GPIFREADYSTAT | GPIF Ready Status | 0 | 0 | RDY5 | RDY4 | RDY3 | RDY2 | RDY1 | RDY0 | 00xxxxxx | R |
| E6F5 | 1 | GPIFABORT | Abort GPIF Waveforms | x | x | x | x | x | x | x | x | xxxxxxxx | W |
| E6F6 | 2 | reserved | | | | | | | | | | | |
| | | ENDPOINT BUFFERS | | | | | | | | | | | |
| E740 | 64 | EP0BUF | EP0-IN/-OUT buffer | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| E780 | 64 | EP10UTBUF | EP1-OUT buffer | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| E7C0 | 64 | EP1INBUF | EP1-IN buffer | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| E800 | 2048 | reserved | | | | | | | | | | | RW |
| F000 | 1024 | EP2FIFOBUF | 512/1024 byte EP 2 / slave FIFO buffer (IN or OUT) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| F400 | 512 | EP4FIFOBUF | 512 byte EP 4 / slave FIFO buffer (IN or OUT) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| F600 | 512 | reserved | | | | | | | | | | | |
| F800 | 1024 | EP6FIFOBUF | 512/1024 byte EP 6 / slave FIFO buffer (IN or OUT) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| FC00 | 512 | EP8FIFOBUF | 512 byte EP 8 / slave FIFO buffer (IN or OUT) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | xxxxxxxx | RW |
| FE00 | 512 | reserved | | | | | | | | | | | |

## Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power supplied (commercial)..... 0 °C to +70 °C

Ambient temperature with power supplied (industrial)..... –40 °C to + 105 °C

Supply voltage to ground potential .....–0.5 V to +4.0 V

DC input voltage to any input pin[17] ..... 5.25 V

DC voltage applied to outputs in high Z state ..... –0.5 V to $V_{CC}$ + 0.5 V

Power dissipation ..... 300 mW

Static discharge voltage..... .....>2000 V

Max output current, per I/O port ..... 10 mA

Max output current, all five I/O ports (128-pin and 100-pin packages)..... 50 mA

## Operating Conditions

$T_A$ (ambient temperature under bias) Commercial ..... 0 °C to +70 °C

$T_A$ (ambient temperature under bias) Industrial ..... –40 °C to +105 °C

Supply voltage .....+3.00 V to +3.60 V

Ground voltage ..... 0 V

$F_{OSC}$ (oscillator or crystal frequency) ..... 24 MHz ± 100 ppm, parallel resonant

## Thermal Characteristics

The following table displays the thermal characteristics of various packages:

**Table 13. Thermal Characteristics**

| Package | Ambient Temperature (°C) | $\theta_{Jc}$ Junction to Case Thermal Resistance (°C/W) | $\theta_{Ja}$ Junction to Ambient Thermal Resistance (°C/W) |
|---|---|---|---|
| 56 SSOP | 70 | 24.4 | 47.7 |
| 100 TQFP | 70 | 11.9 | 45.9 |
| 128 TQFP | 70 | 15.5 | 43.2 |
| 56 QFN | 70 | 10.6 | 25.2 |
| 56 VFBGA | 70 | 30.9 | 58.6 |

The junction temperature $\theta_j$, can be calculated using the following equation: $\theta_j = P*\theta_{Ja} + \theta_a$

Where,

P = Power

$\theta_{Ja}$ = Junction to ambient temperature ($\theta_{Jc} + \theta_{Ca}$)

$\theta_a$ = Ambient temperature (70 °C)

The case temperature $\theta_c$, can be calculated using the following equation: $\theta_c = P*\theta_{Ca} + \theta_a$

where,

P = Power

$\theta_{Ca}$ = Case to ambient temperature

$\theta_a$ = Ambient temperature (70 °C)

**Note**
17. Do not power I/O with the chip power OFF.

## DC Characteristics

**Table 14. DC Characteristics**

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VCC | Supply voltage | – | 3.00 | 3.3 | 3.60 | V |
| VCC Ramp Up | 0 to 3.3 V | – | 200 | – | – | µs |
| $V_{IH}$ | Input HIGH voltage | – | 2 | – | 5.25 | V |
| $V_{IL}$ | Input LOW voltage | – | –0.5 | – | 0.8 | V |
| $V_{IH\_X}$ | Crystal input HIGH voltage | – | 2 | – | 5.25 | V |
| $V_{IL\_X}$ | Crystal input LOW voltage | – | –0.5 | – | 0.8 | V |
| $I_I$ | Input leakage current | $0< V_{IN} < V_{CC}$ | – | – | ±10 | µA |
| $V_{OH}$ | Output voltage HIGH | $I_{OUT}$ = 4 mA | 2.4 | – | – | V |
| $V_{OL}$ | Output LOW voltage | $I_{OUT}$ = –4 mA | – | – | 0.4 | V |
| $I_{OH}$ | Output current HIGH | – | – | – | 4 | mA |
| $I_{OL}$ | Output current LOW | – | – | – | 4 | mA |
| $C_{IN}$ | Input pin capacitance | Except D+/D– | – | – | 10 | pF |
| | | D+/D– | – | – | 15 | pF |
| $I_{SUSP}$ | Suspend current CY7C68014/CY7C68016 | Connected | – | 300 | 380[18] | µA |
| | | Disconnected | – | 100 | 150[18] | µA |
| | Suspend current CY7C68013/CY7C68015 | Connected | – | 0.5 | 1.2[18] | mA |
| | | Disconnected | – | 0.3 | 1.0[18] | mA |
| $I_{CC}$ | Supply current | 8051 running, connected to USB HS | – | 50 | 85 | mA |
| | | 8051 running, connected to USB FS | – | 35 | 65 | mA |
| $T_{RESET}$ | Reset time after valid power | $V_{CC}$ min = 3.0 V | 5.0 | – | – | ms |
| | Pin reset after powered on | | 200 | – | – | µs |

### USB Transceiver

USB 2.0 compliant in Full Speed and Hi-Speed modes.

**Note**
18. Measured at Max $V_{CC}$, 25 °C.

## Data Memory Write[23]

**Figure 14. Data Memory Write Timing Diagram**

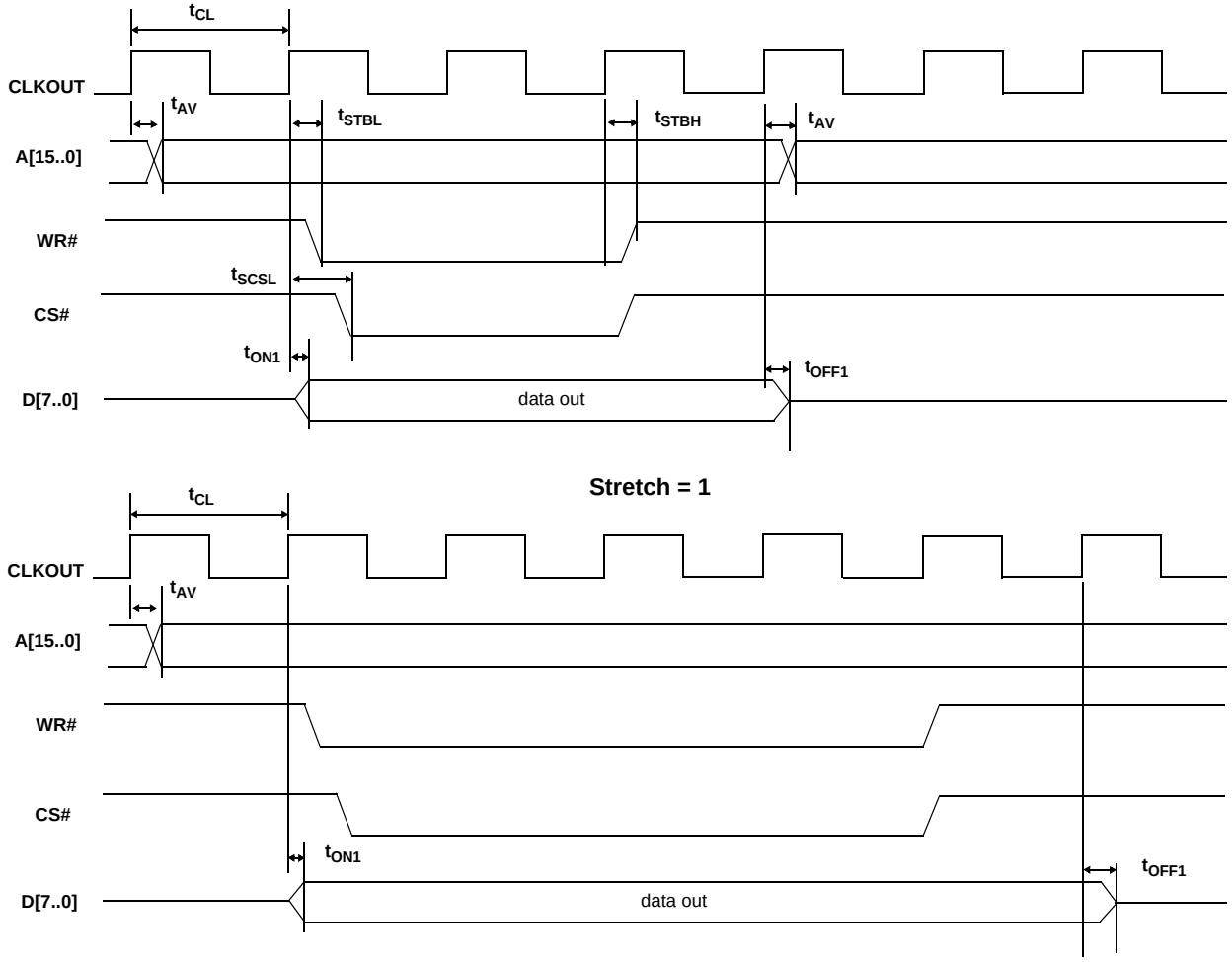



**Table 17. Data Memory Write Parameters**

| Parameter | Description | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $t_{AV}$ | Delay from clock to valid address | 0 | 10.7 | ns | – |
| $t_{STBL}$ | Clock to WR pulse LOW | 0 | 11.2 | ns | – |
| $t_{STBH}$ | Clock to WR pulse HIGH | 0 | 11.2 | ns | – |
| $t_{SCSL}$ | Clock to CS pulse LOW | – | 13.0 | ns | – |
| $t_{ON1}$ | Clock to data turn-on | 0 | 13.1 | ns | – |
| $t_{OFF1}$ | Clock to data hold time | 0 | 13.1 | ns | – |

When using the AUTPOPTR1 or AUTOPTR2 to address external memory, the address of AUTOPTR1 is only active while either RD# or WR# are active. The address of AUTOPTR2 is active throughout the cycle and meets the address valid time for which is based on the stretch value.

**Note**
23. The stretch memory cycle feature enables EZ-USB firmware to adjust the speed of data memory accesses not the program memory accesses. Details including typical strobe width timings can be found in the section 12.1.2 of the Technical Reference Manual. The address cycle width can be interpreted from these.

### Slave FIFO Synchronous Write

**Figure 21. Slave FIFO Synchronous Write Timing Diagram[24]**

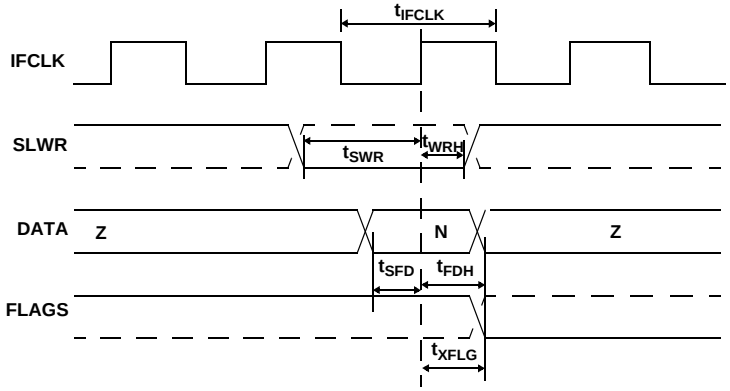



**Table 23. Slave FIFO Synchronous Write Parameters with Internally Sourced IFCLK[25]**

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{IFCLK}$ | IFCLK period | 20.83 | – | ns |
| $t_{SWR}$ | SLWR to clock setup time | 10.4 | – | ns |
| $t_{WRH}$ | Clock to SLWR hold time | 0 | – | ns |
| $t_{SFD}$ | FIFO data to clock setup time | 9.2 | – | ns |
| $t_{FDH}$ | Clock to FIFO data hold time | 0 | – | ns |
| $t_{XFLG}$ | Clock to FLAGS output propagation time | – | 9.5 | ns |

**Table 24. Slave FIFO Synchronous Write Parameters with Externally Sourced IFCLK[25]**

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{IFCLK}$ | IFCLK Period | 20.83 | 200 | ns |
| $t_{SWR}$ | SLWR to clock setup time | 12.1 | – | ns |
| $t_{WRH}$ | Clock to SLWR hold time | 3.6 | – | ns |
| $t_{SFD}$ | FIFO data to clock setup time | 3.2 | – | ns |
| $t_{FDH}$ | Clock to FIFO data hold time | 4.5 | – | ns |
| $t_{XFLG}$ | Clock to FLAGS output propagation time | – | 13.5 | ns |

### Slave FIFO Asynchronous Write

**Figure 22. Slave FIFO Asynchronous Write Timing Diagram[24]**

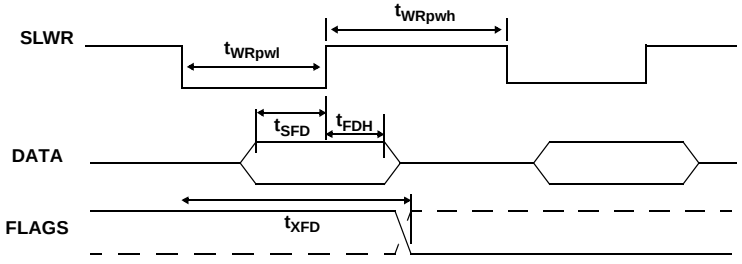


**Table 25. Slave FIFO Asynchronous Write Parameters with Internally Sourced IFCLK[27]**

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{WRpwl}$ | SLWR pulse LOW | 50 | – | ns |
| $t_{WRpwh}$ | SLWR pulse HIGH | 70 | – | ns |
| $t_{SFD}$ | SLWR to FIFO DATA setup time | 10 | – | ns |
| $t_{FDH}$ | FIFO DATA to SLWR hold time | 10 | – | ns |
| $t_{XFD}$ | SLWR to FLAGS output propagation delay | – | 70 | ns |

## Slave FIFO Synchronous Packet End Strobe

**Figure 23. Slave FIFO Synchronous Packet End Strobe Timing Diagram[24]**

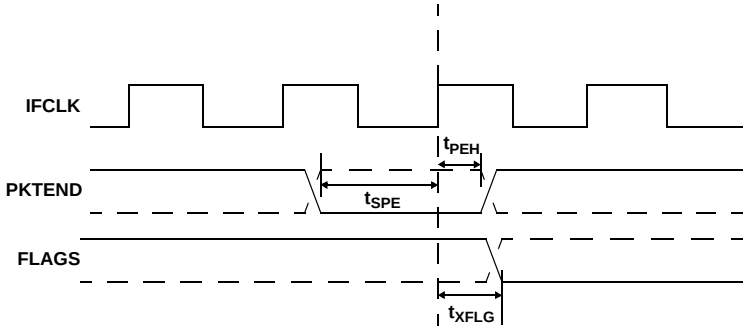



**Table 26. Slave FIFO Synchronous Packet End Strobe Parameters with Internally Sourced IFCLK[25]**

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{IFCLK}$ | IFCLK period | 20.83 | – | ns |
| $t_{SPE}$ | PKTEND to clock setup time | 14.6 | – | ns |
| $t_{PEH}$ | Clock to PKTEND hold time | 0 | – | ns |
| $t_{XFLG}$ | Clock to FLAGS output propagation delay | – | 9.5 | ns |

**Table 27. Slave FIFO Synchronous Packet End Strobe Parameters with Externally Sourced IFCLK[25]**

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $t_{IFCLK}$ | IFCLK period | 20.83 | 200 | ns |
| $t_{SPE}$ | PKTEND to clock setup time | 8.6 | – | ns |
| $t_{PEH}$ | Clock to PKTEND hold time | 2.5 | – | ns |
| $t_{XFLG}$ | Clock to FLAGS output propagation delay | – | 13.5 | ns |

There is no specific timing requirement that should be met for asserting the PKTEND pin to asserting SLWR. PKTEND can be asserted with the last data value clocked into the FIFOs or thereafter. The setup time $t_{SPE}$ and the hold time $t_{PEH}$ must be met.

Although there are no specific timing requirements for PKTEND assertion, there is a specific corner-case condition that needs attention while using the PKTEND pin to commit a one byte or word packet. There is an additional timing requirement that needs to be met when the FIFO is configured to operate in auto mode and it is required to send two packets back to back: a full packet (full defined as the number of bytes in the FIFO meeting the level set in AUTOINLEN register) committed automatically followed by a short one byte or word packet committed manually using the PKTEND pin. In this scenario, the user must ensure to assert PKTEND, at least one clock cycle after the rising edge that caused the last byte or word to be clocked into the previous auto committed packet. Figure 24 shows this scenario. X is the value the AUTOINLEN register is set to when the IN endpoint is configured to be in auto mode.

Figure 24 shows a scenario where two packets are committed. The first packet gets committed automatically when the number of bytes in the FIFO reaches X (value set in AUTOINLEN register) and the second one byte/word short packet being committed manually using PKTEND.

Note that there is at least one IFCLK cycle timing between the assertion of PKTEND and clocking of the last byte of the previous packet (causing the packet to be committed automatically). Failing to adhere to this timing results in the FX2 failing to send the one byte or word short packet.

## Sequence Diagram

*Single and Burst Synchronous Read Example*

**Figure 30. Slave FIFO Synchronous Read Sequence and Timing Diagram**[24]

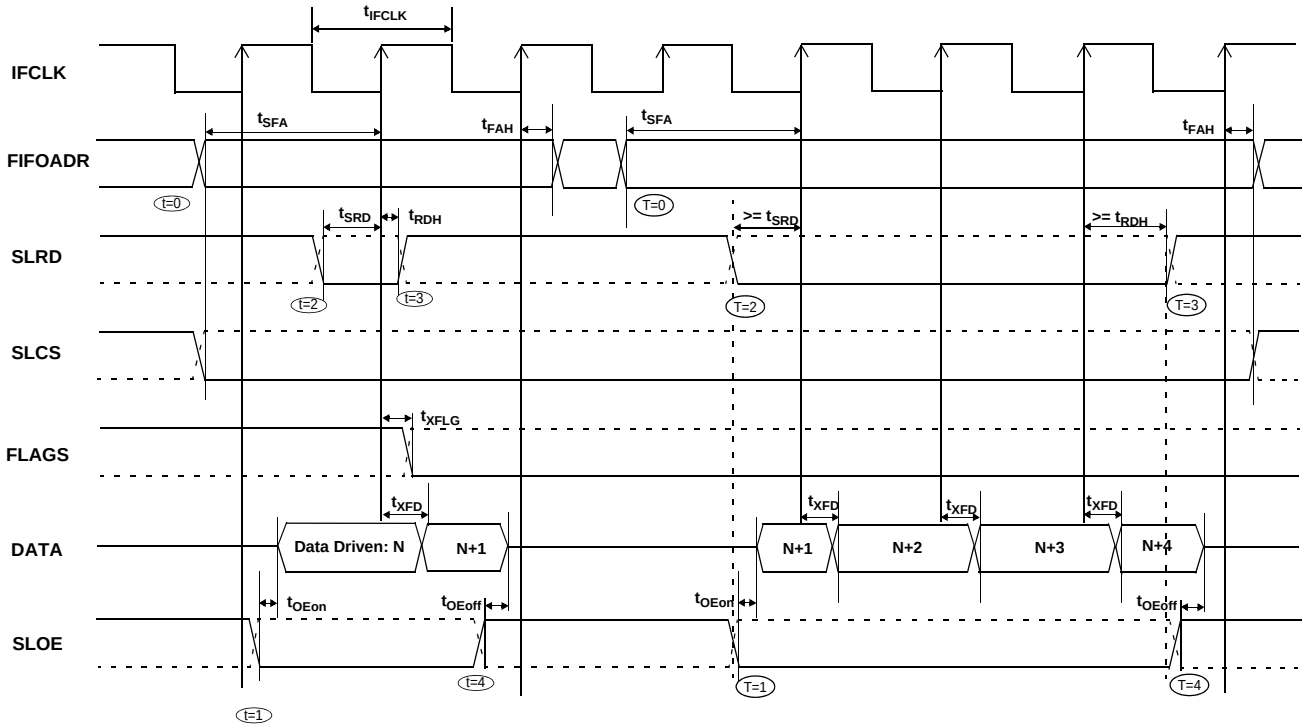



**Figure 31. Slave FIFO Synchronous Sequence of Events Diagram**

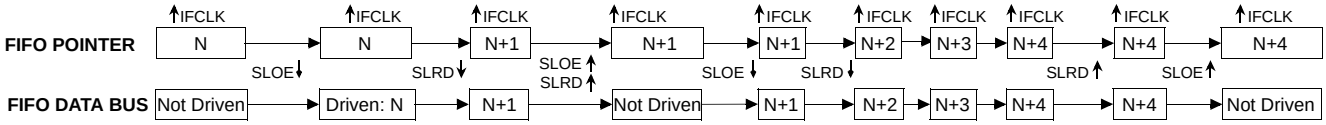



Figure 30 on page 52 shows the timing relationship of the SLAVE FIFO signals during a synchronous FIFO read using IFCLK as the synchronizing clock. The diagram illustrates a single read followed by a burst read.

- At t = 0, the FIFO address is stable and the signal SLCS is asserted (SLCS may be tied LOW in some applications). Note that $t_{SFA}$ has a minimum of 25 ns. This means that when IFCLK is running at 48 MHz, the FIFO address setup time is more than one IFCLK cycle.
- At t = 1, SLOE is asserted. SLOE is an output enable only, whose sole function is to drive the data bus. The data that is driven on the bus is the data that the internal FIFO pointer is currently pointing to. In this example it is the first data value in the FIFO. **Note**: the data is prefetched and is driven on the bus when SLOE is asserted.
- At t = 2, SLRD is asserted. SLRD must meet the setup time of $t_{SRD}$ (time from asserting the SLRD signal to the rising edge of the IFCLK) and maintain a minimum hold time of $t_{RDH}$ (time from the IFCLK edge to the deassertion of the SLRD signal). If the SLCS signal is used, it must be asserted before SLRD is asserted (The SLCS and SLRD signals must both be asserted to start a valid read condition).
- The FIFO pointer is updated on the rising edge of the IFCLK, while SLRD is asserted. This starts the propagation of data from the newly addressed location to the data bus. After a propagation delay of $t_{XFD}$ (measured from the rising edge of IFCLK) the new data value is present. N is the first data value read from the FIFO. To have data on the FIFO data bus, SLOE MUST also be asserted.

The same sequence of events are shown for a burst read and are marked with the time indicators of T = 0 through 5.

**Note** For the burst mode, the SLRD and SLOE are left asserted during the entire duration of the read. In the burst read mode, when SLOE is asserted, data indexed by the FIFO pointer is on the data bus. During the first read cycle, on the rising edge of the clock, the FIFO pointer is updated and incremented to point to address N+1. For each subsequent rising edge of IFCLK, while the SLRD is asserted, the FIFO pointer is incremented and the next data value is placed on the data bus.

*Single and Burst Synchronous Write*

**Figure 32. Slave FIFO Synchronous Write Sequence and Timing Diagram**[24]

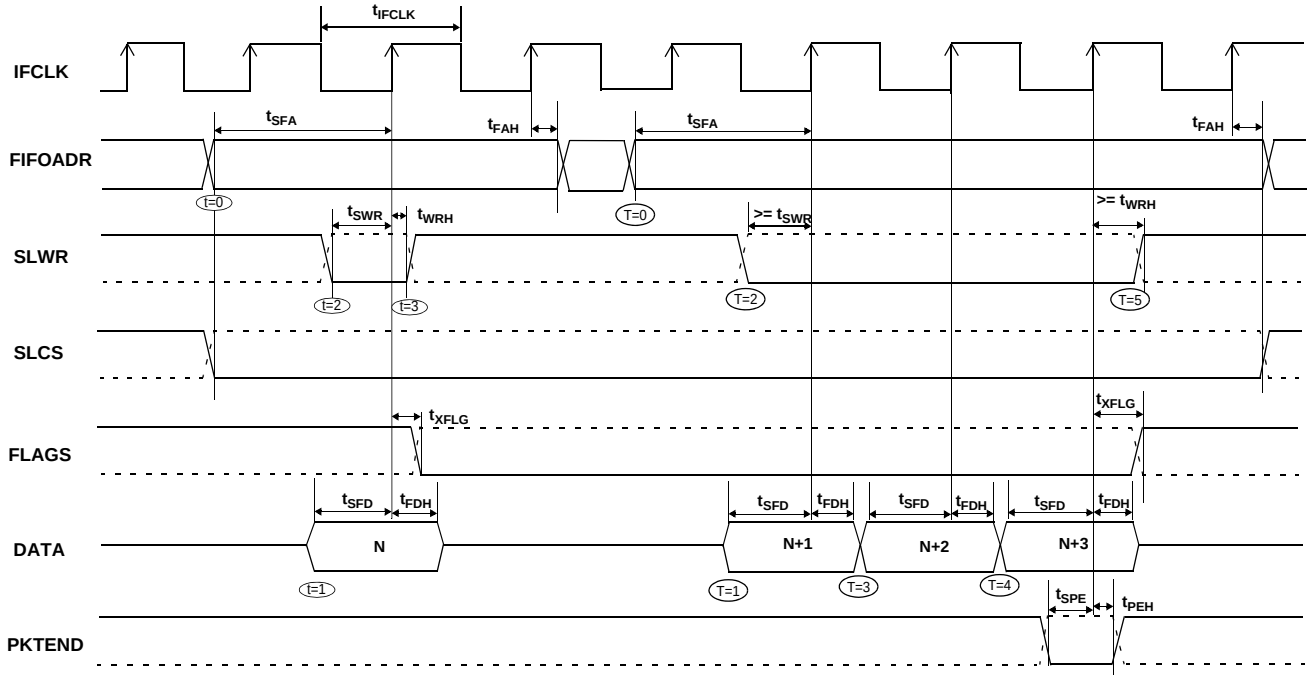



Figure 32 shows the timing relationship of the SLAVE FIFO signals during a synchronous write using IFCLK as the synchronizing clock. The diagram illustrates a single write followed by burst write of three bytes and committing all four bytes as a short packet using the PKTEND pin.

- At t = 0 the FIFO address is stable and the signal SLCS is asserted. (SLCS may be tied LOW in some applications) Note that $t_{SFA}$ has a minimum of 25 ns. This means when IFCLK is running at 48 MHz, the FIFO address setup time is more than one IFCLK cycle.
- At t = 1, the external master/peripheral must outputs the data value onto the data bus with a minimum set up time of $t_{SFD}$ before the rising edge of IFCLK.
- At t = 2, SLWR is asserted. The SLWR must meet the setup time of $t_{SWR}$ (time from asserting the SLWR signal to the rising edge of IFCLK) and maintain a minimum hold time of $t_{WRH}$ (time from the IFCLK edge to the deassertion of the SLWR signal). If the SLCS signal is used, it must be asserted with SLWR or before SLWR is asserted (The SLCS and SLWR signals must both be asserted to start a valid write condition).
- While the SLWR is asserted, data is written to the FIFO and on the rising edge of the IFCLK, the FIFO pointer is incremented. The FIFO flag is also updated after a delay of $t_{XFLG}$ from the rising edge of the clock.

The same sequence of events are also shown for a burst write and are marked with the time indicators of T = 0 through 5.

**Note** For the burst mode, SLWR and SLCS are left asserted for the entire duration of writing all the required data values. In this burst write mode, after the SLWR is asserted, the data on the FIFO data bus is written to the FIFO on every rising edge of IFCLK. The FIFO pointer is updated on each rising edge of IFCLK. In Figure 32, after the four bytes are written to the FIFO, SLWR is deasserted. The short 4 byte packet can be committed to the host by asserting the PKTEND signal.

There is no specific timing requirement that should be met for asserting PKTEND signal with regards to asserting the SLWR signal. PKTEND can be asserted with the last data value or thereafter. The only requirement is that the setup time $t_{SPE}$ and the hold time $t_{PEH}$ must be met. In the scenario of Figure 32, the number of data values committed includes the last value written to the FIFO. In this example, both the data value and the PKTEND signal are clocked on the same rising edge of IFCLK. PKTEND can also be asserted in subsequent clock cycles. The FIFOADDR lines should be held constant during the PKTEND assertion.

Although there are no specific timing requirement for the PKTEND assertion, there is a specific corner-case condition that needs attention while using the PKTEND to commit a one byte/word packet. Additional timing requirements exist when the FIFO is configured to operate in auto mode and it is desired to send two packets: a full packet (‘full’ defined as the number of bytes in the FIFO meeting the level set in the AUTOINLEN register) committed automatically followed by a short one byte or word packet committed manually using the PKTEND pin.

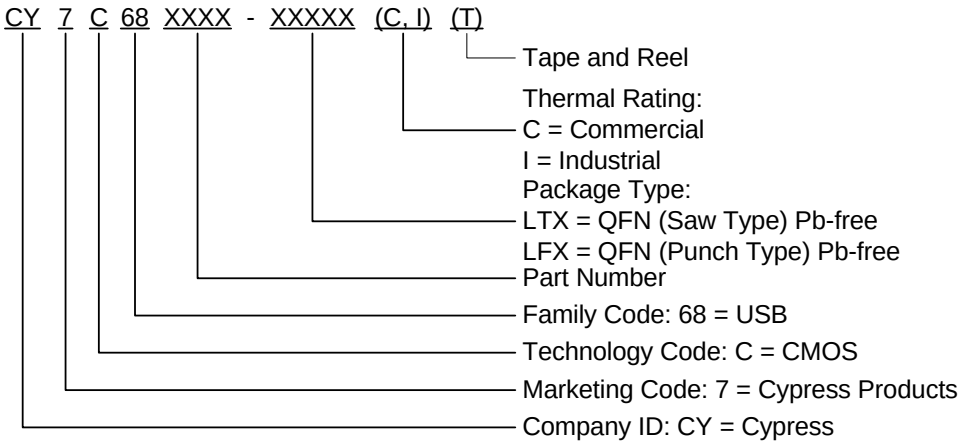
In this case, the external master must ensure to assert the PKTEND pin at least one clock cycle after the rising edge that caused the last byte or word that needs to be clocked into the previous auto committed packet (the packet with the number of bytes equal to what is set in the AUTOINLEN register). Refer to Figure 24 on page 50 for further details on this timing.

## Ordering Information

**Table 33. Ordering Information**

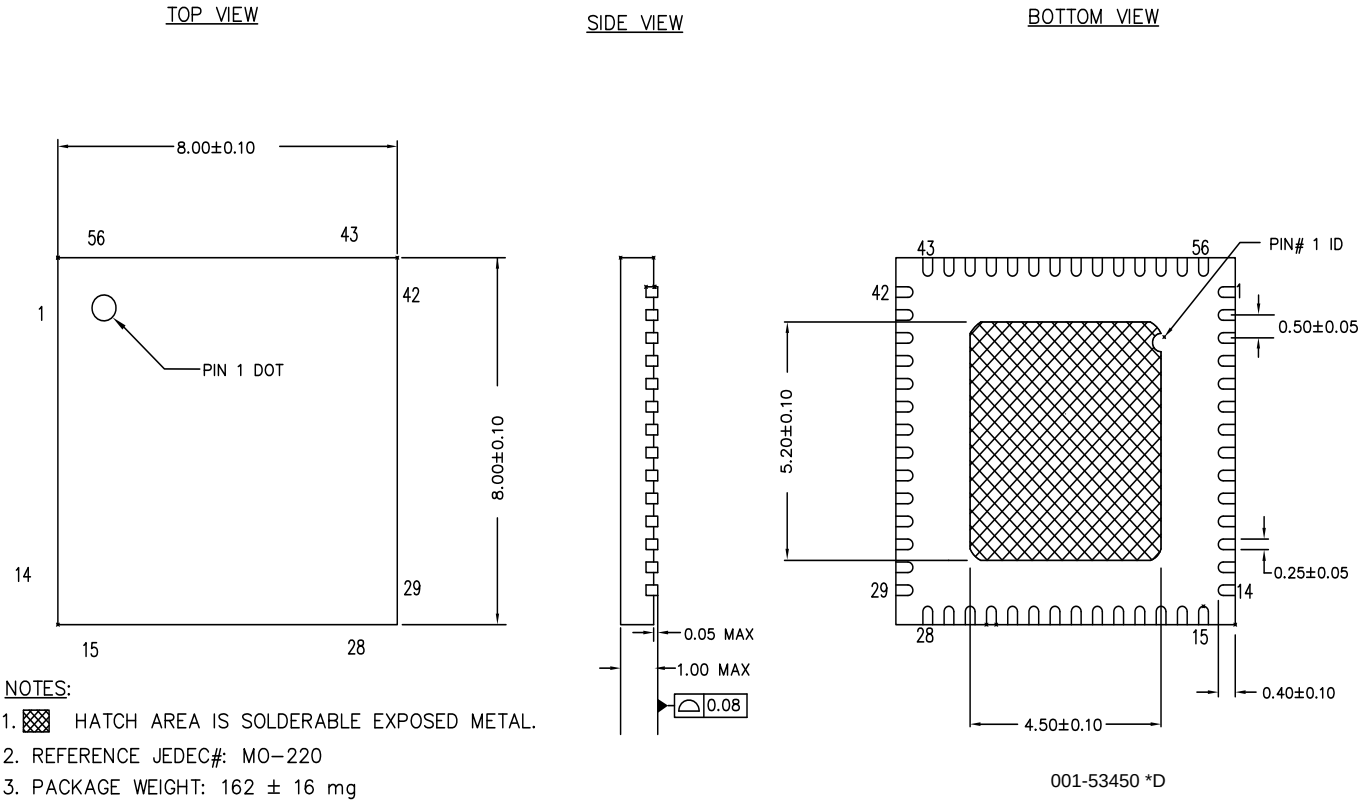
| Ordering Code | Package Type | RAM Size | # Prog I/Os | 8051 Address /Data Bus | Serial Debug[28] |
|---|---|---|---|---|---|
| **Ideal for Battery Powered Applications** | | | | | |
| CY7C68014A-128AXC | 128 TQFP – Pb-free | 16 K | 40 | 16-/8-bit | Y |
| CY7C68014A-100AXC | 100 TQFP – Pb-free | 16 K | 40 | – | Y |
| CY7C68014A-56PVXC | 56 SSOP – Pb-free | 16 K | 24 | – | N |
| CY7C68014A-56LTXC | 56 QFN - Pb-free | 16 K | 24 | – | N |
| CY7C68016A-56LTXC | 56 QFN - Pb-free | 16 K | 26 | – | N |
| CY7C68016A-56LTXCT | 56 QFN - Pb-free | 16 K | 26 | – | N |
| **Ideal for Non Battery Powered Applications** | | | | | |
| CY7C68013A-128AXC | 128 TQFP – Pb-free | 16 K | 40 | 16-/8-bit | Y |
| CY7C68013A-128AXI | 128 TQFP – Pb-free (Industrial) | 16 K | 40 | 16-/8-bit | Y |
| CY7C68013A-100AXC | 100 TQFP – Pb-free | 16 K | 40 | – | Y |
| CY7C68013A-100AXI | 100 TQFP – Pb-free (Industrial) | 16 K | 40 | – | Y |
| CY7C68013A-56PVXC | 56 SSOP – Pb-free | 16 K | 24 | – | N |
| CY7C68013A-56PVXCT | 56 SSOP – Pb-free | 16 K | 24 | – | N |
| CY7C68013A-56PVXI | 56 SSOP – Pb-free (Industrial) | 16 K | 24 | – | N |
| CY7C68013A-56BAXC | 56 VFBGA – Pb-free | 16 K | 24 | – | N |
| CY7C68013A-56BAXCT | 56 VFBGA – Pb-free | 16 K | 24 | – | N |
| CY7C68013A-56LTXC | 56 QFN – Pb-free | 16 K | 24 | – | N |
| CY7C68013A-56LTXCT | 56 QFN – Pb-free | 16 K | 24 | – | N |
| CY7C68013A-56LTXI | 56 QFN – Pb-free (Industrial) | 16 K | 24 | – | N |
| CY7C68015A-56LTXC | 56 QFN – Pb-free | 16 K | 26 | – | N |
| **Development Tool Kit** | | | | | |
| CY3684 | EZ-USB FX2LP development kit | | | | |
| **Reference Design Kit** | | | | | |
| CY4611B | USB 2.0 to ATA/ATAPI reference design using EZ-USB FX2LP | | | | |

### Ordering Code Definitions




**Note**
28. As UART is not available in the 56-pin package of CY7C68013A, serial port debugging using Keil Monitor is not possible.

**Figure 37. 56-Pin QFN 8 × 8 mm Sawn Version (001-53450)**




NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO–220
3. PACKAGE WEIGHT: 162 ± 16 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

**Figure 39. 128-Pin Thin Plastic Quad Flatpack (14 × 20 × 1.4 mm) A128 (51-85101)**

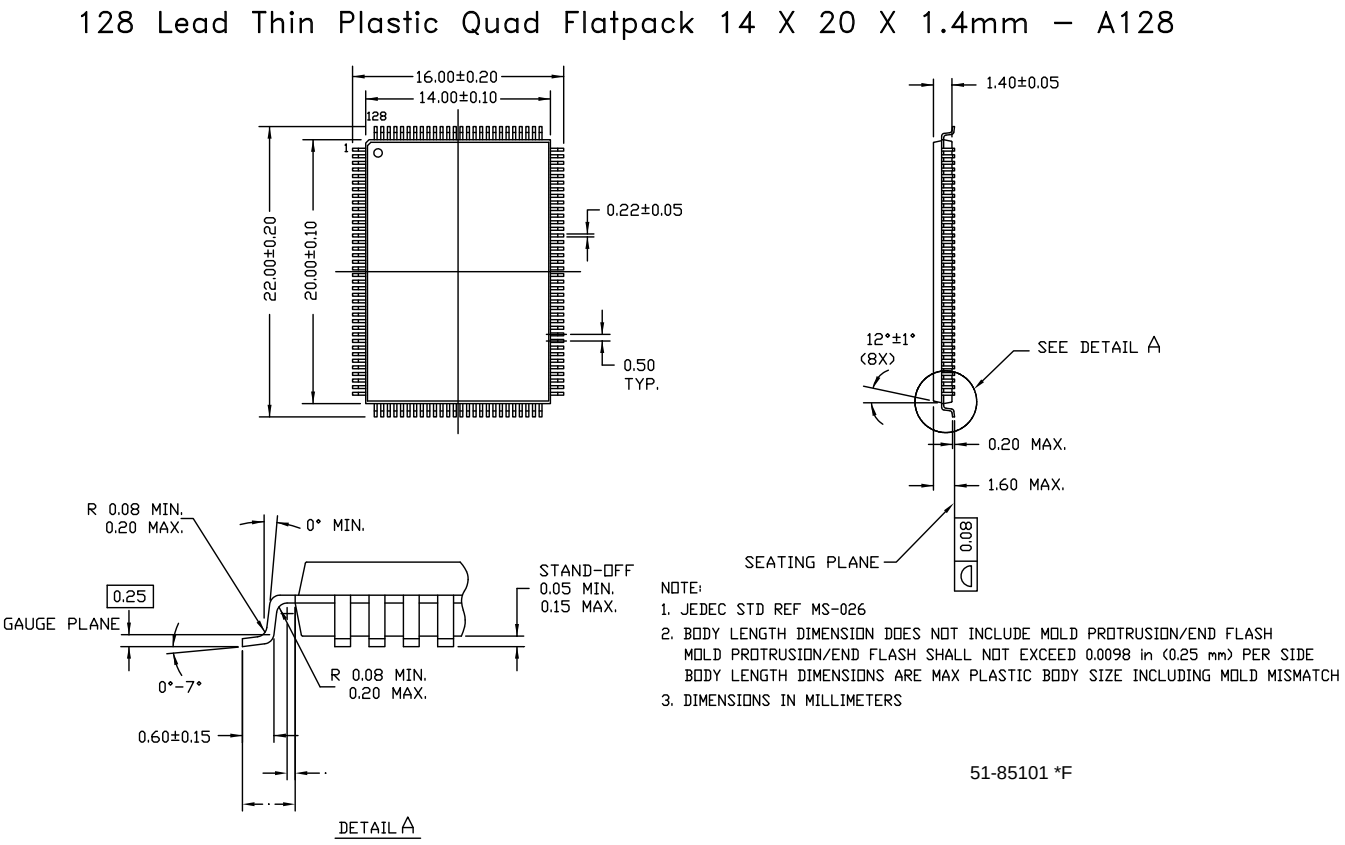
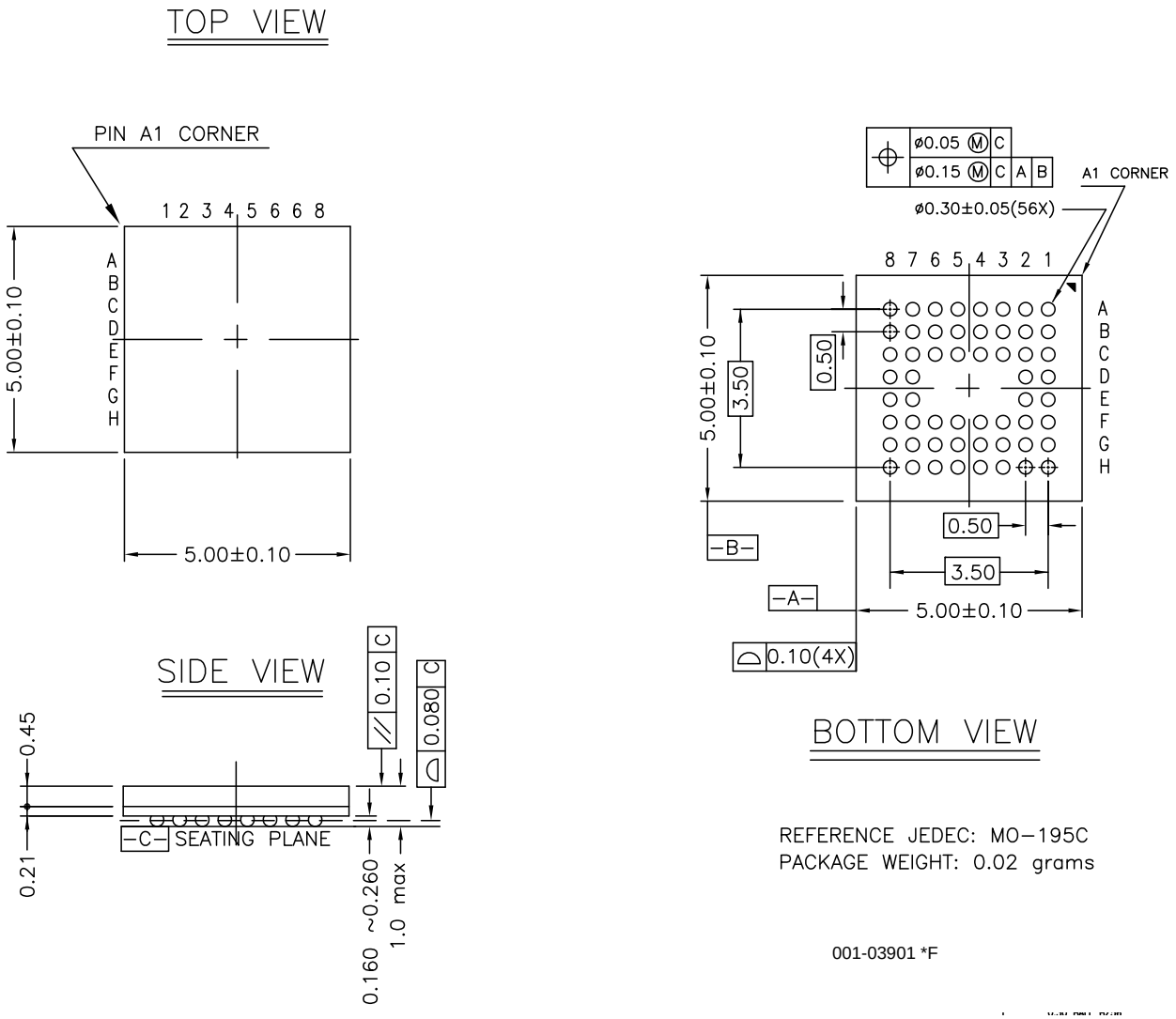


**Figure 40. 56-Pin VFBGA (5 × 5 × 1.0 mm) 0.50 Pitch, 0.30 Ball BZ56 (001-03901)**



# Errata

This section describes the errata for the EZ-USB® FX2LP™ CY7C68013A/14A/15A/16A Rev. B silicon. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

## Part Numbers Affected

| Part Number | Package Type | Operating Range |
|---|---|---|
| CY7C68013A | All | Commercial |
| CY7C68014A | All | Commercial |
| CY7C68015A | All | Commercial |
| CY7C68016A | All | Commercial |

## CY7C68013A/14A/15A/16A Qualification Status

In production

## CY7C68013A/14A/15A/16A Errata Summary

This table defines the errata for available CY7C68013A/14A/15A/16A family devices. An "X" indicates that the errata pertain to the selected device.

| Items | CY7C68013A/14A/15A/16A | Silicon Revision | Fix Status |
|---|---|---|---|
| [1.]. Empty Flag Assertion | X | B | No silicon fix planned currently. Use the workaround. |

### 1. Empty Flag Assertion

**■ Problem Definition**

In Slave FIFO Asynchronous Word Wide mode, if a single word data is transferred from the USB host to EP2, configured as OUT Endpoint (EP) in the first transaction, then the Empty flag behaves incorrectly. This does not happen if the data size is more than one word in the first transaction.

**■ Parameters Affected**

NA

**■ Trigger Condition(S)**

In Slave FIFO Asynchronous Word Wide Mode, after firmware boot and initialization, EP2 OUT endpoint empty flag indicates the status as ‘Empty’. When data is received in EP2, the status changes to ‘Not-Empty’. However, if data transferred to EP2 is a single word, then asserting SLRD with FIFOADR pointing to any other endpoint changes ‘Not-Empty’ status to ‘Empty’ for EP2 even though there is a word data (or it is untouched). This is noticed only when the single word is sent as the first transaction and not if it follows a multi-word packet as the first transaction.

**■ Scope of Impact**

External interface does not see data available in EP2 OUT endpoint and can end up waiting for data to be read.

**■ Workaround**

One of the following workarounds can be used:

- Send a pulse signal to the SLWR pin, with FIFOADR pins pointing to an endpoint other than EP2, after firmware initialization and before or after transferring the data to EP2 from the host
- Set the length of the first data to EP2 to be more than a word
- Prioritize EP2 read from the Master for multiple OUT EPs and single word write to EP2
- Write to an IN EP, if any, from the Master before reading from other OUT EPs (other than EP2) from the Master.

**■ Fix Status**

There is no silicon fix planned for this currently; use the workarounds provided.

## Document History Page

| Document Title: CY7C68013A, CY7C68014A, CY7C68015A, CY7C68016A, EZ-USB® FX2LP™ USB Microcontroller High-Speed USB Peripheral Controller<br>Document Number: 38-08032 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 124316 | VCS | 03/17/03 | New datasheet |
| *A | 128461 | VCS | 09/02/03 | Added PN CY7C68015A throughout datasheet<br>Modified Figure 1 to add ECC block and fix errors<br>Removed word “compatible” where associated with $I^2C$<br>Corrected grammar and formatting in various locations<br>Updated Sections 3.2.1, 3.9, 3.11, Table 9, Section 5.0<br>Added Sections 3.15, 3.18.4, 3.20<br>Modified Figure 5 for clarity<br>Updated Figure 37 to match current spec revision |
| *B | 130335 | KKV | 10/09/03 | Restored PRELIMINARY to header (had been removed in error from rev. *A) |
| *C | 131673 | KKU | 02/12/04 | Section 8.1 changed “certified” to “compliant”<br>Table 14 added parameter $V_{IH\_X}$ and $V_{IL\_X}$<br>Added Sequence diagrams Section 9.16<br>Updated Ordering information with lead-free parts<br>Updated Registry Summary<br>Section 3.12.4:example changed to column 8 from column 9<br>Updated Figure 14 memory write timing Diagram<br>Updated section 3.9 (reset)<br>Updated section 3.15 ECC Generation |
| *D | 230713 | KKU | See ECN | Changed Lead free Marketing part numbers in Table 33 as per spec change in 28-00054. |
| *E | 242398 | TMD | See ECN | Minor Change: datasheet posted to the web, |
| *F | 271169 | MON | See ECN | Added USB-IF Test ID number<br>Added USB 2.0 logo<br>Added values for Isusp, Icc, Power Dissipation, Vih_x, Vil_x<br>Changed VCC from ± 10% to ± 5%<br>Changed PKTEND to FLAGS output propagation delay (asynchronous interface) in Table 28 from a max value of 70 ns to 115 ns |
| *G | 316313 | MON | See ECN | Removed CY7C68013A-56PVXCT part availability<br>Added parts ideal for battery powered applications: CY7C68014A, CY7C68016A<br>Provided additional timing restrictions and requirement about the use of PKETEND pin to commit a short one byte/word packet subsequent to committing a packet automatically (when in auto mode).<br>Added Min Vcc Ramp Up time (0 to 3.3v) |
| *H | 338901 | MON | See ECN | Added information about the AUTOPTR1/AUTOPTR2 address timing with regards to data memory read/write timing diagram.<br>Removed TBD for Min value of Clock to FIFO Data Output Propagation Delay ($t_{XFD}$) for Slave FIFO Synchronous Read<br>Changed Table 33 to include part CY7C68016A-56LFXC in the part listed for battery powered applications<br>Added register GPCR2 in register summary |
| *I | 371097 | MON | See ECN | Added timing for strobing RD#/WR# signals when using PortC strobe feature (Section ) |
| *J | 397239 | MON | See ECN | Removed XTALINSRC register from register summary.<br>Changed Vcc margins to ±10%<br>Added 56-pin VFBGA Pin Package Diagram<br>Added 56-pin VFBGA definition in pin listing<br>Added RDK part number to the Ordering Information table |