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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	USB Microcontroller
Core Processor	8051
Program Memory Type	ROMless
Controller Series	CY7C680xx
RAM Size	16K x 8
Interface	I²C, USB, USART
Number of I/O	24
Voltage - Supply	3V ~ 3.6V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	56-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	56-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c68013a-56pvxi

Table 1. Special Function Registers

x	8x	9x	Ax	Bx	Cx	Dx	Ex	Fx
0	**IOA**	**IOB**	**IOC**	**IOD**	SCON1	PSW	ACC	B
1	SP	**EXIF**	**INT2CLR**	**IOE**	SBUF1	–	–	–
2	DPL0	**MPAGE**	**INT4CLR**	**OEA**	–	–	–	–
3	DPH0	–	–	**OEB**	–	–	–	–
4	**DPL1**	–	–	**OEC**	–	–	–	–
5	**DPH1**	–	–	**OED**	–	–	–	–
6	**DPS**	–	–	**OEE**	–	–	–	–
7	PCON	–	–	–	–	–	–	–
8	TCON	SCON0	IE	IP	T2CON	**EICON**	**EIE**	**EIP**
9	TMOD	SBUF0	–	–	–	–	–	–
A	TL0	**AUTOPTRH1**	**EP2468STAT**	**EP01STAT**	RCAP2L	–	–	–
B	TL1	**AUTOPTRL1**	**EP24FIFOFLGS**	**GPIFTRIG**	RCAP2H	–	–	–
C	TH0	**reserved**	**EP68FIFOFLGS**		TL2	–	–	–
D	TH1	**AUTOPTRH2**	–	**GPIFSGLDATH**	TH2	–	–	–
E	**CKCON**	**AUTOPTRL2**	–	**GPIFSGLDATLX**	–	–	–	–
F	–	**reserved**	**AUTOPTRSET-UP**	**GPIFSGLDATLNOX**	–	–	–	–

USB Boot Methods

During the power-up sequence, internal logic checks the I^2C port for the connection of an EEPROM whose first byte is either 0xC0 or 0xC2. If found, it uses the VID/PID/DID values in the EEPROM in place of the internally stored values (0xC0), or it boot-loads the EEPROM contents into internal RAM (0xC2). If no EEPROM is detected, FX2LP enumerates using internally stored descriptors. The default ID values for FX2LP are VID/PID/DID (0x04B4, 0x8613, 0xAxxx where xxx = Chip revision).[2]

Table 2. Default ID Values for FX2LP

Default VID/PID/DID		
Vendor ID	0x04B4	Cypress Semiconductor
Product ID	0x8613	EZ-USB FX2LP
Device release	0xAnnn	Depends on chip revision (nnn = chip revision where first silicon = 001)

ReNumeration

Because the FX2LP's configuration is soft, one chip can take on the identities of multiple distinct USB devices.

When first plugged into USB, the FX2LP enumerates automatically and downloads firmware and USB descriptor tables over the USB cable. Next, the FX2LP enumerates again, this time as a device defined by the downloaded information. This patented two step process called ReNumeration™ happens instantly when the device is plugged in, without a hint that the initial download step has occurred.

Two control bits in the USBCS (USB Control and Status) register control the ReNumeration process: DISCON and RENUM. To simulate a USB disconnect, the firmware sets DISCON to 1. To reconnect, the firmware clears DISCON to 0.

Before reconnecting, the firmware sets or clears the RENUM bit to indicate whether the firmware or the Default USB Device handles device requests over endpoint zero: if RENUM = 0, the Default USB Device handles device requests; if RENUM = 1, the firmware services the requests.

Bus-Powered Applications

The FX2LP fully supports bus-powered designs by enumerating with less than 100 mA as required by the USB 2.0 specification.

Interrupt System

INT2 Interrupt Request and Enable Registers

FX2LP implements an autovector feature for INT2 and INT4. There are 27 INT2 (USB) vectors, and 14 INT4 (FIFO/GPIF) vectors. See EZ-USB Technical Reference Manual (TRM) for more details.

USB Interrupt Autovectors

The main USB interrupt is shared by 27 interrupt sources. To save the code and processing time that is required to identify the individual USB interrupt source, the FX2LP provides a second level of interrupt vectoring, called Autovectoring. When a USB interrupt is asserted, the FX2LP pushes the program counter to its stack, and then jumps to the address 0x0043 where it expects to find a "jump" instruction to the USB interrupt service routine.

Note
2. The I^2C bus SCL and SDA pins must be pulled up, even if an EEPROM is not connected. Otherwise this detection method does not work properly.

Table 4. Individual FIFO/GPIF Interrupt Sources

Priority	INT4VEC Value	Source	Notes
1	80	EP2PF	Endpoint 2 programmable flag
2	84	EP4PF	Endpoint 4 programmable flag
3	88	EP6PF	Endpoint 6 programmable flag
4	8C	EP8PF	Endpoint 8 programmable flag
5	90	EP2EF	Endpoint 2 empty flag [3]
6	94	EP4EF	Endpoint 4 empty flag
7	98	EP6EF	Endpoint 6 empty flag
8	9C	EP8EF	Endpoint 8 empty flag
9	A0	EP2FF	Endpoint 2 full flag
10	A4	EP4FF	Endpoint 4 full flag
11	A8	EP6FF	Endpoint 6 full flag
12	AC	EP8FF	Endpoint 8 full flag
13	B0	GPIFDONE	GPIF operation complete
14	B4	GPIFWF	GPIF waveform

If Autovectoring is enabled (AV4EN = 1 in the INTSET-UP register), the FX 2LP substitutes its INT4VEC byte. Therefore, if the high byte (“page”) of a jump-table address is preloaded at location 0x0054, the automatically inserted INT4VEC byte at 0x0055 directs the jump to the correct address out of the 14 addresses within the page. When the ISR occurs, the FX2LP pushes the program counter to its stack then jumps to address 0x0053, where it expects to find a “jump” instruction to the interrupt service routine (ISR).

Note
3. Errata: In Slave FIFO Asynchronous Word Wide mode, if a single word data is transferred from the USB host to EP2, configured as OUT Endpoint (EP) in the first transaction, then the Empty flag behaves incorrectly. This does not happen if the data size is more than one word in the first transaction. For more information, see the “Errata” on page 65.

Program/Data RAM

SizeThe FX2LP has 16 KB of internal program/data RAM, where PSEN#/RD# signals are internally ORed to enable the 8051 to access it as both program and data memory. No USB control registers appears in this space.

Two memory maps are shown in the following diagrams:

Figure 3 on page 10 shows the Internal Code Memory, EA = 0.

Figure 4 on page 11 shows the External Code Memory, EA = 1.

Internal Code Memory, EA = 0

This mode implements the internal 16 KB block of RAM (starting at 0) as combined code and data memory. When external RAM or ROM is added, the external read and write strobes are suppressed for memory spaces that exist inside the chip. This enables the user to connect a 64 KB memory without requiring address decodes to keep clear of internal memory spaces.

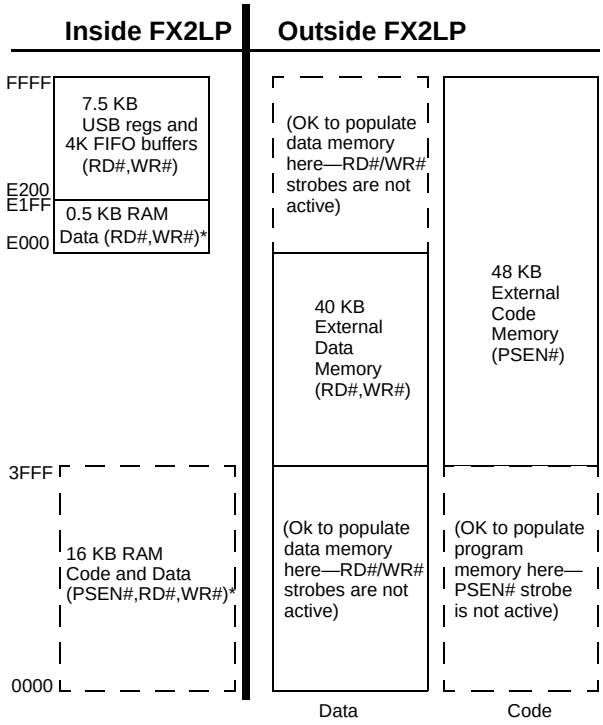
Only the internal 16 KB and scratch pad 0.5 KB RAM spaces have the following access:

- USB download
- USB upload
- Setup data pointer
- I^2C interface boot load

External Code Memory, EA = 1

The bottom 16 KB of program memory is external and therefore the bottom 16 KB of internal RAM is accessible only as a data memory.

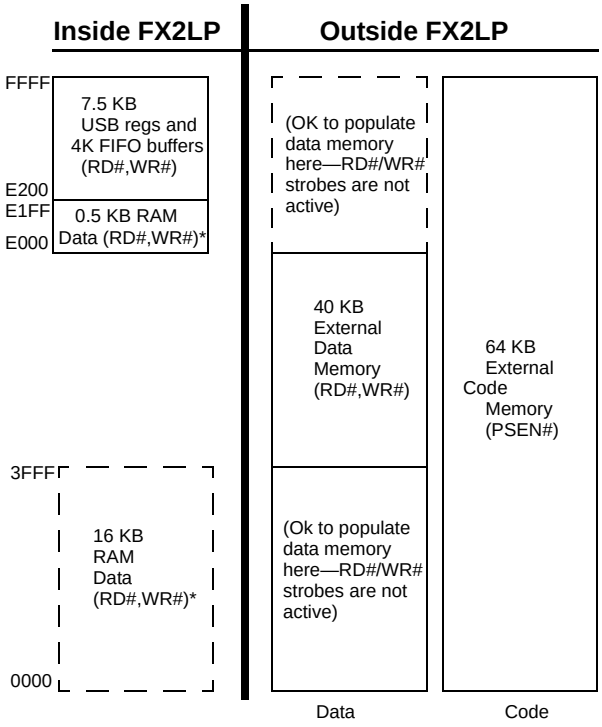
Figure 3. Internal Code Memory, EA = 0



*SUDPTR, USB upload/download, I^2C interface boot access

Note
4. If the external clock is powered at the same time as the CY7C680xxA and has a stabilization wait period, it must be added to the 200 µs.

Figure 4. External Code Memory, EA = 1



*SUDPTR, USB upload/download, I^2C interface boot access

Register Addresses

FFFF F000	4 KB EP2-EP8 buffers (8 x 512)
EFFF E800	2 KB RESERVED
E7FF E7C0	64 BEP1IN
E7BF E780	64 Bytes EP1OUT
E77F E740	64 Bytes EP0 IN/OUT
E73F E700	64 Bytes RESERVED
E6FF E500	8051 Addressable Registers (512)
E4FF E480	Reserved (128)
E47F E400	128 Bytes GPIF Waveforms
E3FF E200	Reserved (512)
E1FF E000	512 Bytes 8051 xdata RAM

Endpoint RAM

Size

- 3 × 64 bytes (Endpoints 0 and 1)
- 8 × 512 bytes (Endpoints 2, 4, 6, 8)

Organization

- EP0
- Bidirectional endpoint zero, 64-byte buffer
- EP1IN, EP1OUT
- 64 byte buffers, bulk or interrupt
- EP2, 4, 6, 8
- Eight 512-byte buffers, bulk, interrupt, or isochronous. EP4 and EP8 can be double buffered; EP2 and 6 can be either double, triple, or quad buffered. For Hi-Speed endpoint configuration options, see Figure 5.

Setup Data Buffer

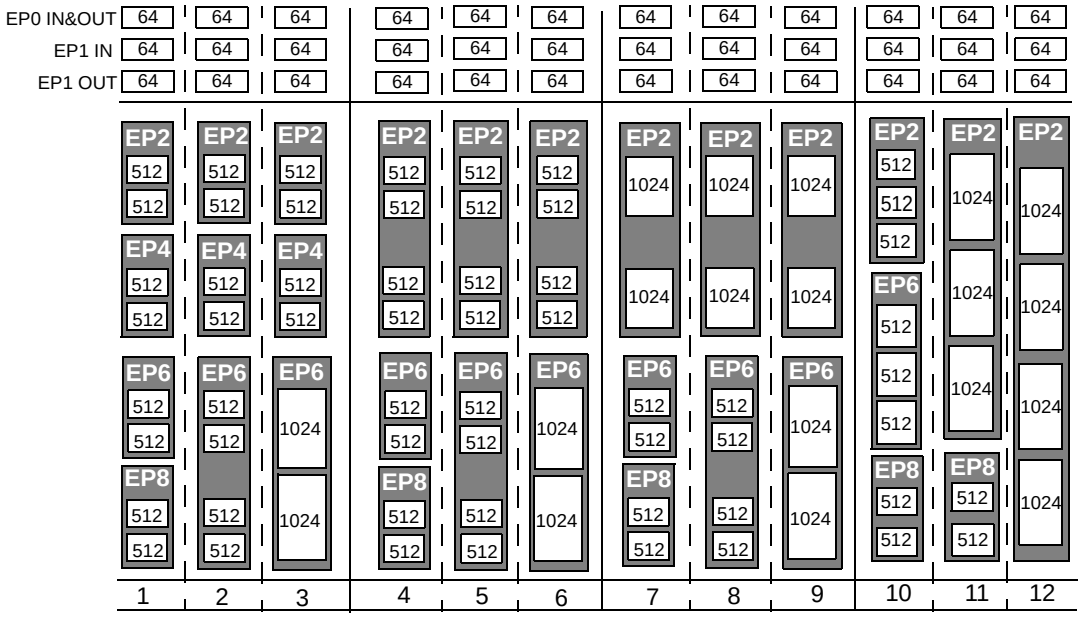
A separate 8-byte buffer at 0xE6B8-0xE6BF holds the setup data from a CONTROL transfer.

Endpoint Configurations (Hi-Speed Mode)

Endpoints 0 and 1 are the same for every configuration. Endpoint 0 is the only CONTROL endpoint, and endpoint 1 can be either BULK or INTERRUPT.

The endpoint buffers can be configured in any 1 of the 12 configurations shown in the vertical columns. When operating in the Full-Speed BULK mode, only the first 64 bytes of each buffer are used. For example, in Hi-Speed mode, the max packet size is 512 bytes, but in Full-Speed mode, it is 64 bytes. Even though a buffer is configured to a 512-byte buffer, in Full-Speed mode, only the first 64 bytes are used. The unused endpoint buffer space is not available for other operations. An example endpoint configuration is the EP2–1024 double-buffered; EP6–512 quad-buffered (column 8).

Figure 5. Endpoint Configuration



Default Full-Speed Alternate Settings

Table 6. Default Full Speed Alternate Settings[5, 6]

Alternate Setting	0	1	2	3
ep0	64	64	64	64
ep1out	0	64 bulk	64 int	64 int
ep1in	0	64 bulk	64 int	64 int
ep2	0	64 bulk out (2×)	64 int out (2×)	64 iso out (2×)
ep4	0	64 bulk out (2×)	64 bulk out (2×)	64 bulk out (2×)
ep6	0	64 bulk in (2×)	64 int in (2×)	64 iso in (2×)
ep8	0	64 bulk in (2×)	64 bulk in (2×)	64 bulk in (2×)

Default High Speed Alternate Settings

Table 7. Default Hi-Speed Alternate Settings[5, 6]

Alternate Setting	0	1	2	3
ep0	64	64	64	64
ep1out	0	512 bulk[7]	64 int	64 int
ep1in	0	512 bulk[7]	64 int	64 int
ep2	0	512 bulk out (2×)	512 int out (2×)	512 iso out (2×)
ep4	0	512 bulk out (2×)	512 bulk out (2×)	512 bulk out (2×)
ep6	0	512 bulk in (2×)	512 int in (2×)	512 iso in (2×)
ep8	0	512 bulk in (2×)	512 bulk in (2×)	512 bulk in (2×)

External FIFO Interface

Architecture

The FX2LP slave FIFO architecture has eight 512-byte blocks in the endpoint RAM that directly serve as FIFO memories and are controlled by FIFO control signals (such as IFCLK, SLCS#, SLRD, SLWR, SLOE, PKTEND, and flags).

In operation, some of the eight RAM blocks fill or empty from the SIE, while the others are connected to the I/O transfer logic. The transfer logic takes two forms: the GPIF for internally generated control signals and the slave FIFO interface for externally controlled transfers.

Master/Slave Control Signals

The FX2LP endpoint FIFOs are implemented as eight physically distinct 256×16 RAM blocks. The 8051/SIE can switch any of the RAM blocks between two domains, the USB (SIE) domain and the 8051-I/O Unit domain. This switching is done virtually instantaneously, giving essentially zero transfer time between "USB FIFOs" and "Slave FIFOs." Because they are physically the same memory, no bytes are actually transferred between buffers.

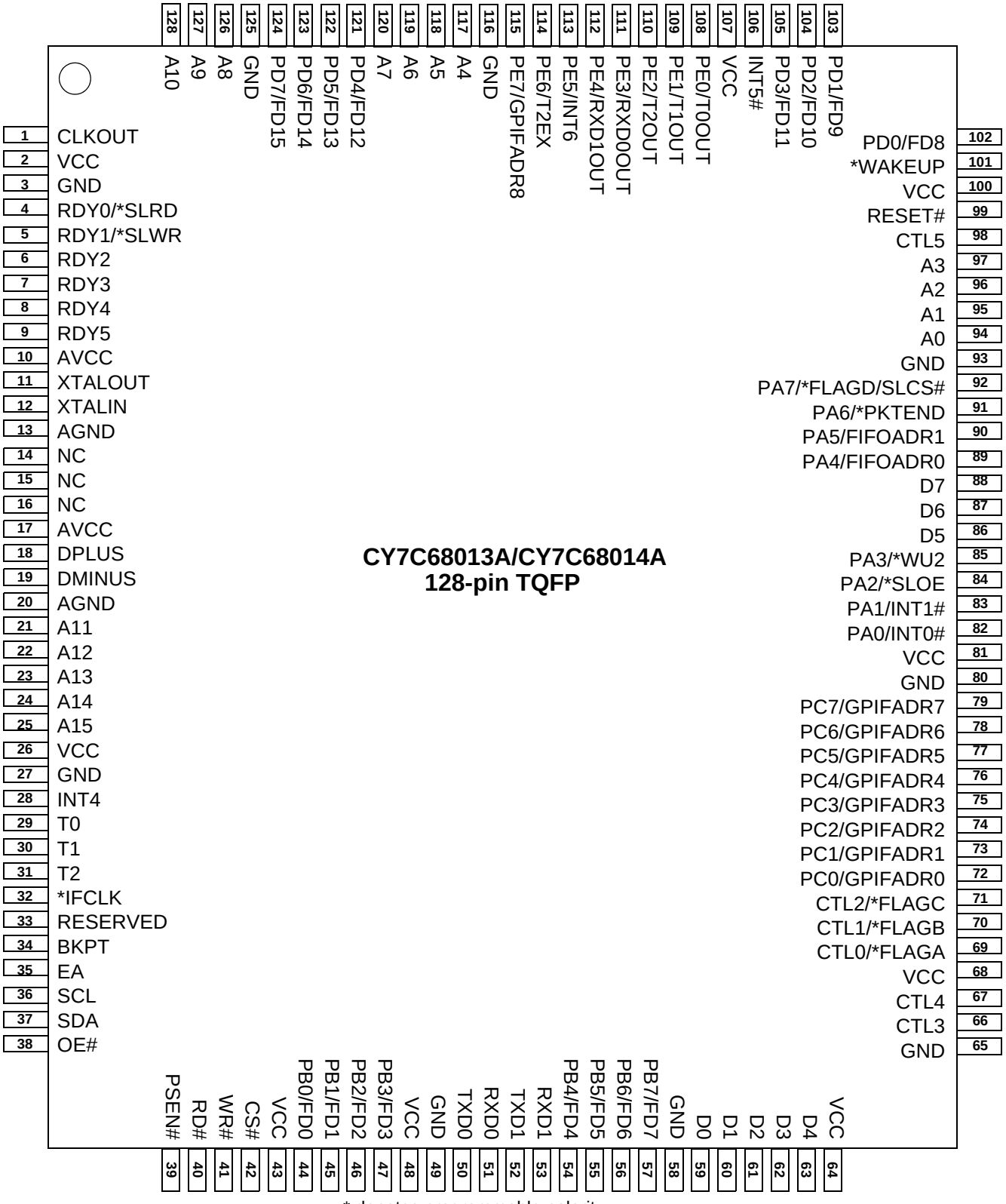
At any time, some RAM blocks are filling/emptying with the USB data under SIE control, while other RAM blocks are available to the 8051, the I/O control unit, or both. The RAM blocks operates as single-port in the USB domain, and dual-port in the 8051-I/O domain. The blocks can be configured as single-, double-, triple-, or quad-buffered as previously shown.

The I/O control unit implements either an internal master (M for Master) or external master (S for Slave) interface.

In Master (M) mode, the GPIF internally controls FIFOADR[1..0] to select a FIFO. The RDY pins (two in the 56-pin package, six in the 100-pin and 128-pin packages) can be used as flag inputs from an external FIFO or other logic if desired. The GPIF can be run from either an internally derived clock or externally supplied clock (IFCLK), at a rate that transfers data up to 96 MBytes/s (48

Notes
5. "0" means "not implemented."
6. "2×" means "double buffered."
7. Even though these buffers are 64 bytes, they are reported as 512 for USB 2.0 compliance. The user must never transfer packets larger than 64 bytes to EP1.

Figure 7. CY7C68013A/CY7C68014A 128-Pin TQFP Pin Assignment



* denotes programmable polarity

Table 11. FX2LP Pin Descriptions[11] (continued)

128 TQFP	100 TQFP	56 SSOP	56 QFN	56 VFBGA	Name	Type	Default	Reset[12]	Description
PORT D									
102	80	52	45	8A	PD0 or FD[8]	I/O/Z	I (PD0)	Z (PD0)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[8]** is the bidirectional FIFO/GPIF data bus.
103	81	53	46	7A	PD1 or FD[9]	I/O/Z	I (PD1)	Z (PD1)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[9]** is the bidirectional FIFO/GPIF data bus.
104	82	54	47	6B	PD2 or FD[10]	I/O/Z	I (PD2)	Z (PD2)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[10]** is the bidirectional FIFO/GPIF data bus.
105	83	55	48	6A	PD3 or FD[11]	I/O/Z	I (PD3)	Z (PD3)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[11]** is the bidirectional FIFO/GPIF data bus.
121	95	56	49	3B	PD4 or FD[12]	I/O/Z	I (PD4)	Z (PD4)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[12]** is the bidirectional FIFO/GPIF data bus.
122	96	1	50	3A	PD5 or FD[13]	I/O/Z	I (PD5)	Z (PD5)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[13]** is the bidirectional FIFO/GPIF data bus.
123	97	2	51	3C	PD6 or FD[14]	I/O/Z	I (PD6)	Z (PD6)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[14]** is the bidirectional FIFO/GPIF data bus.
124	98	3	52	2A	PD7 or FD[15]	I/O/Z	I (PD7)	Z (PD7)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[15]** is the bidirectional FIFO/GPIF data bus.
Port E									
108	86	–	–	–	PE0 or T0OUT	I/O/Z	I (PE0)	Z (PE0)	Multiplexed pin whose function is selected by the PORTECFG.0 bit. **PE0** is a bidirectional I/O port pin. **T0OUT** is an active-HIGH signal from 8051 Timer-counter0. T0OUT outputs a high level for one CLKOUT clock cycle when Timer0 overflows. If Timer0 is operated in Mode 3 (two separate timer/counters), T0OUT is active when the low byte timer/counter overflows.
109	87	–	–	–	PE1 or T1OUT	I/O/Z	I (PE1)	Z (PE1)	Multiplexed pin whose function is selected by the PORTECFG.1 bit. **PE1** is a bidirectional I/O port pin. **T1OUT** is an active HIGH signal from 8051 Timer-counter1. T1OUT outputs a high level for one CLKOUT clock cycle when Timer1 overflows. If Timer1 is operated in Mode 3 (two separate timer/counters), T1OUT is active when the low byte timer/counter overflows.

Table 11. FX2LP Pin Descriptions[11] (continued)

128 TQFP	100 TQFP	56 SSOP	56 QFN	56 VFBGA	Name	Type	Default	Reset[12]	Description
100	78	50	43	5B	VCC	Power	N/A	N/A	**VCC**. Connect to the 3.3-V power source.
107	85	–	–	–	VCC	Power	N/A	N/A	**VCC**. Connect to the 3.3-V power source.
3	2	7	56	4B	GND	Ground	N/A	N/A	**Ground**
27	21	19	12	1H	GND	Ground	N/A	N/A	**Ground**
49	39	–	–	–	GND	Ground	N/A	N/A	**Ground**
58	48	33	26	7D	GND	Ground	N/A	N/A	**Ground**
65	50	35	28	8D	GND	Ground	N/A	N/A	**Ground**
80	65	–	–	–	GND	Ground	N/A	N/A	**Ground**
93	75	48	41	4C	GND	Ground	N/A	N/A	**Ground**
116	94	–	–	–	GND	Ground	N/A	N/A	**Ground**
125	99	4	53	4A	GND	Ground	N/A	N/A	**Ground**
14	13	–	–	–	NC	N/A	N/A	N/A	**No Connect**. This pin must be left open.
15	14	–	–	–	NC	N/A	N/A	N/A	**No Connect**. This pin must be left open.
16	15	–	–	–	NC	N/A	N/A	N/A	**No Connect**. This pin must be left open.

Table 12. FX2LP Register Summary (continued)

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
E62B	1	ECC1B1	ECC1 Byte 1 Address	LINE7	LINE6	LINE5	LINE4	LINE3	LINE2	LINE1	LINE0	00000000	R
E62C	1	ECC1B2	ECC1 Byte 2 Address	COL5	COL4	COL3	COL2	COL1	COL0	LINE17	LINE16	00000000	R
E62D	1	ECC2B0	ECC2 Byte 0 Address	LINE15	LINE14	LINE13	LINE12	LINE11	LINE10	LINE9	LINE8	00000000	R
E62E	1	ECC2B1	ECC2 Byte 1 Address	LINE7	LINE6	LINE5	LINE4	LINE3	LINE2	LINE1	LINE0	00000000	R
E62F	1	ECC2B2	ECC2 Byte 2 Address	COL5	COL4	COL3	COL2	COL1	COL0	0	0	00000000	R
E630 H.S.	1	EP2FIFOPFH[13]	Endpoint 2 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	IN:PKTS[2] OUT:PFC12	IN:PKTS[1] OUT:PFC11	IN:PKTS[0] OUT:PFC10	0	PFC9	PFC8	10001000	bbbbbrbb
E630 F.S.	1	EP2FIFOPFH[13]	Endpoint 2 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	OUT:PFC12	OUT:PFC11	OUT:PFC10	0	PFC9	IN:PKTS[2] OUT:PFC8	10001000	bbbbbrbb
E631 H.S.	1	EP2FIFOPFL[13]	Endpoint 2 / slave FIFO Programmable Flag L	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E631 F.S	1	EP2FIFOPFL[13]	Endpoint 2 / slave FIFO Programmable Flag L	IN:PKTS[1] OUT:PFC7	IN:PKTS[0] OUT:PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E632 H.S.	1	EP4FIFOPFH[13]	Endpoint 4 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	0	IN: PKTS[1] OUT:PFC10	IN: PKTS[0] OUT:PFC9	0	0	PFC8	10001000	bbrbbrrb
E632 F.S	1	EP4FIFOPFH[13]	Endpoint 4 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	0	OUT:PFC10	OUT:PFC9	0	0	PFC8	10001000	bbrbbrrb
E633 H.S.	1	EP4FIFOPFL[13]	Endpoint 4 / slave FIFO Programmable Flag L	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E633 F.S	1	EP4FIFOPFL[13]	Endpoint 4 / slave FIFO Programmable Flag L	IN: PKTS[1] OUT:PFC7	IN: PKTS[0] OUT:PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E634 H.S.	1	EP6FIFOPFH[13]	Endpoint 6 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	IN:PKTS[2] OUT:PFC12	IN:PKTS[1] OUT:PFC11	IN:PKTS[0] OUT:PFC10	0	PFC9	PFC8	00001000	bbbbbrbb
E634 F.S	1	EP6FIFOPFH[13]	Endpoint 6 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	OUT:PFC12	OUT:PFC11	OUT:PFC10	0	PFC9	IN:PKTS[2] OUT:PFC8	00001000	bbbbbrbb
E635 H.S.	1	EP6FIFOPFL[13]	Endpoint 6 / slave FIFO Programmable Flag L	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E635 F.S	1	EP6FIFOPFL[13]	Endpoint 6 / slave FIFO Programmable Flag L	IN:PKTS[1] OUT:PFC7	IN:PKTS[0] OUT:PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E636 H.S.	1	EP8FIFOPFH[13]	Endpoint 8 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	0	IN: PKTS[1] OUT:PFC10	IN: PKTS[0] OUT:PFC9	0	0	PFC8	00001000	bbrbbrrb
E636 F.S	1	EP8FIFOPFH[13]	Endpoint 8 / slave FIFO Programmable Flag H	DECIS	PKTSTAT	0	OUT:PFC10	OUT:PFC9	0	0	PFC8	00001000	bbrbbrrb
E637 H.S.	1	EP8FIFOPFL[13]	Endpoint 8 / slave FIFO Programmable Flag L	PFC7	PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
E637 F.S	1	EP8FIFOPFL[13]	Endpoint 8 / slave FIFO Programmable Flag L	IN: PKTS[1] OUT:PFC7	IN: PKTS[0] OUT:PFC6	PFC5	PFC4	PFC3	PFC2	PFC1	PFC0	00000000	RW
	8	reserved											
E640	1	EP2ISOINPKTS	EP2 (if ISO) IN Packets per frame (1-3)	AADJ	0	0	0	0	0	INPPF1	INPPF0	00000001	brrrrrbb
E641	1	EP4ISOINPKTS	EP4 (if ISO) IN Packets per frame (1-3)	AADJ	0	0	0	0	0	INPPF1	INPPF0	00000001	brrrrrrr
E642	1	EP6ISOINPKTS	EP6 (if ISO) IN Packets per frame (1-3)	AADJ	0	0	0	0	0	INPPF1	INPPF0	00000001	brrrrrbb
E643	1	EP8ISOINPKTS	EP8 (if ISO) IN Packets per frame (1-3)	AADJ	0	0	0	0	0	INPPF1	INPPF0	00000001	brrrrrrr
E644	4	reserved											
E648	1	INPKTEND[13]	Force IN Packet End	Skip	0	0	0	EP3	EP2	EP1	EP0	xxxxxxxx	W
E649	7	OUTPKTEND[13]	Force OUT Packet End	Skip	0	0	0	EP3	EP2	EP1	EP0	xxxxxxxx	W
		INTERRUPTS											
E650	1	EP2FIFOIE[13]	Endpoint 2 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGEPF	PF	EF	FF	00000000	RW
E651	1	EP2FIFOIRQ[13,14]	Endpoint 2 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000000	rrrrrbbb
E652	1	EP4FIFOIE[13]	Endpoint 4 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGEPF	PF	EF	FF	00000000	RW
E653	1	EP4FIFOIRQ[13,14]	Endpoint 4 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000000	rrrrrbbb
E654	1	EP6FIFOIE[13]	Endpoint 6 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGEPF	PF	EF	FF	00000000	RW
E655	1	EP6FIFOIRQ[13,14]	Endpoint 6 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000000	rrrrrbbb
E656	1	EP8FIFOIE[13]	Endpoint 8 slave FIFO Flag Interrupt Enable	0	0	0	0	EDGEPF	PF	EF	FF	00000000	RW
E657	1	EP8FIFOIRQ[13,14]	Endpoint 8 slave FIFO Flag Interrupt Request	0	0	0	0	0	PF	EF	FF	00000000	rrrrrbbb
E658	1	IBNIE	IN-BULK-NAK Interrupt Enable	0	0	EP8	EP6	EP4	EP2	EP1	EP0	00000000	RW
E659	1	IBNIRQ[14]	IN-BULK-NAK interrupt Request	0	0	EP8	EP6	EP4	EP2	EP1	EP0	00xxxxxx	rrbbbbbb
E65A	1	NAKIE	Endpoint Ping-NAK / IBN Interrupt Enable	EP8	EP6	EP4	EP2	EP1	EP0	0	IBN	00000000	RW
E65B	1	NAKIRQ[14]	Endpoint Ping-NAK / IBN Interrupt Request	EP8	EP6	EP4	EP2	EP1	EP0	0	IBN	xxxxxx0x	bbbbbbrb
E65C	1	USBIE	USB Int Enables	0	EP0ACK	HSGRANT	URES	SUSP	SUTOK	SOF	SUDAV	00000000	RW

Note
14. The register can only be reset; it cannot be set.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power supplied (commercial)..... 0 °C to +70 °C

Ambient temperature with power supplied (industrial)..... –40 °C to + 105 °C

Supply voltage to ground potential .....–0.5 V to +4.0 V

DC input voltage to any input pin[17] ..... 5.25 V

DC voltage applied to outputs in high Z state ..... –0.5 V to V_{CC} + 0.5 V

Power dissipation ..... 300 mW

Static discharge voltage..... .....>2000 V

Max output current, per I/O port ..... 10 mA

Max output current, all five I/O ports (128-pin and 100-pin packages)..... 50 mA

Operating Conditions

T_A (ambient temperature under bias) Commercial ..... 0 °C to +70 °C

T_A (ambient temperature under bias) Industrial ..... –40 °C to +105 °C

Supply voltage .....+3.00 V to +3.60 V

Ground voltage ..... 0 V

F_{OSC} (oscillator or crystal frequency) ..... 24 MHz ± 100 ppm, parallel resonant

Thermal Characteristics

The following table displays the thermal characteristics of various packages:

Table 13. Thermal Characteristics

Package	Ambient Temperature (°C)	θ_{Jc} Junction to Case Thermal Resistance (°C/W)	θ_{Ja} Junction to Ambient Thermal Resistance (°C/W)
56 SSOP	70	24.4	47.7
100 TQFP	70	11.9	45.9
128 TQFP	70	15.5	43.2
56 QFN	70	10.6	25.2
56 VFBGA	70	30.9	58.6

The junction temperature θ_j, can be calculated using the following equation: $\theta_j = P*\theta_{Ja} + \theta_a$

Where,

P = Power

θ_{Ja} = Junction to ambient temperature ($\theta_{Jc} + \theta_{Ca}$)

θ_a = Ambient temperature (70 °C)

The case temperature θ_c, can be calculated using the following equation: $\theta_c = P*\theta_{Ca} + \theta_a$

where,

P = Power

θ_{Ca} = Case to ambient temperature

θ_a = Ambient temperature (70 °C)

Note
17. Do not power I/O with the chip power OFF.

Data Memory Write[23]

Figure 14. Data Memory Write Timing Diagram

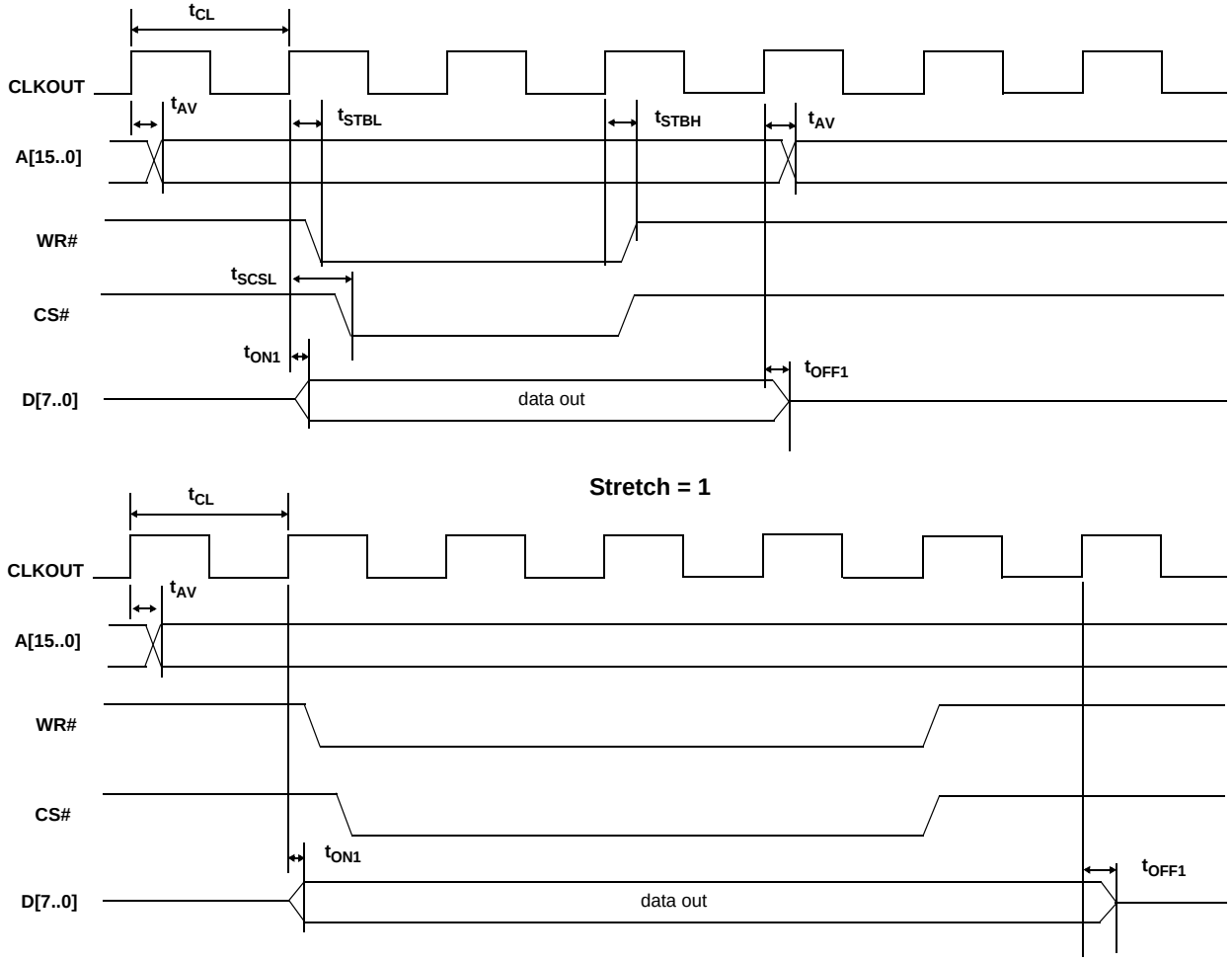


Table 17. Data Memory Write Parameters

Parameter	Description	Min	Max	Unit	Notes
t_{AV}	Delay from clock to valid address	0	10.7	ns	–
t_{STBL}	Clock to WR pulse LOW	0	11.2	ns	–
t_{STBH}	Clock to WR pulse HIGH	0	11.2	ns	–
t_{SCSL}	Clock to CS pulse LOW	–	13.0	ns	–
t_{ON1}	Clock to data turn-on	0	13.1	ns	–
t_{OFF1}	Clock to data hold time	0	13.1	ns	–

When using the AUTPOPTR1 or AUTOPTR2 to address external memory, the address of AUTOPTR1 is only active while either RD# or WR# are active. The address of AUTOPTR2 is active throughout the cycle and meets the address valid time for which is based on the stretch value.

Note
23. The stretch memory cycle feature enables EZ-USB firmware to adjust the speed of data memory accesses not the program memory accesses. Details including typical strobe width timings can be found in the section 12.1.2 of the Technical Reference Manual. The address cycle width can be interpreted from these.

Slave FIFO Synchronous Read

Figure 19. Slave FIFO Synchronous Read Timing Diagram[24]

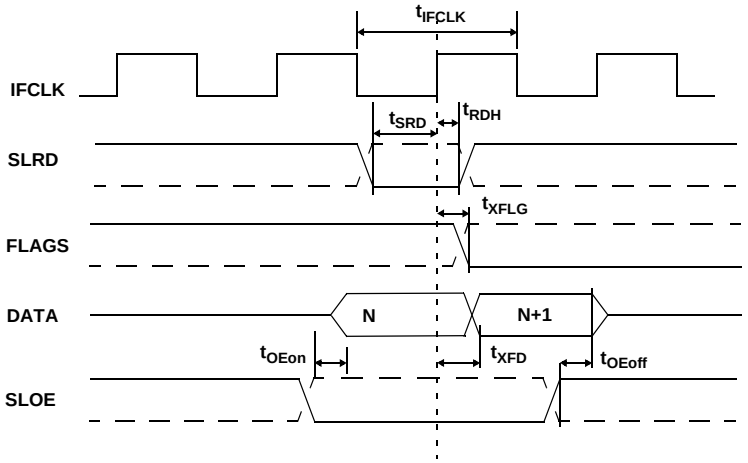


Table 20. Slave FIFO Synchronous Read Parameters with Internally Sourced IFCLK[25]

Parameter	Description	Min	Max	Typ		Unit
				Min	Max	
t_{IFCLK}	IFCLK period	20.83	–	–	–	ns
t_{SRD}	SLRD to clock setup time	18.7	–	–	–	ns
t_{RDH}	Clock to SLRD hold time	0	–	–	–	ns
t_{OEon}	SLOE turn on to FIFO data valid	–	10.5	–	–	ns
t_{OEoff}	SLOE turn off to FIFO data hold	–	10.5	–	–	ns
t_{XFLG}	Clock to FLAGS output propagation delay	–	9.5	–	–	ns
t_{XFD}	Clock to FIFO data output propagation delay	–	11	–	–	ns
t_{IFCLKR}	IFCLK rise time	–	–	–	900	ps
t_{IFCLKF}	IFCLK fall time	–	–	–	900	ps
$t_{IFCLKOD}$	IFCLK output duty cycle	–	–	49	51	%
t_{IFCLKJ}	IFCLK jitter peak to peak	–	–	–	300	ps

Table 21. Slave FIFO Synchronous Read Parameters with Externally Sourced IFCLK[25]

Parameter	Description	Min	Max	Unit
t_{IFCLK}	IFCLK period	20.83	200	ns
t_{SRD}	SLRD to clock setup time	12.7	–	ns
t_{RDH}	Clock to SLRD hold time	3.7	–	ns
t_{OEon}	SLOE turn on to FIFO data valid	–	10.5	ns
t_{OEoff}	SLOE turn off to FIFO data hold	–	10.5	ns
t_{XFLG}	Clock to FLAGS output propagation delay	–	13.5	ns
t_{XFD}	Clock to FIFO data output propagation delay	–	15	ns

Slave FIFO Asynchronous Read

Figure 20. Slave FIFO Asynchronous Read Timing Diagram[24]

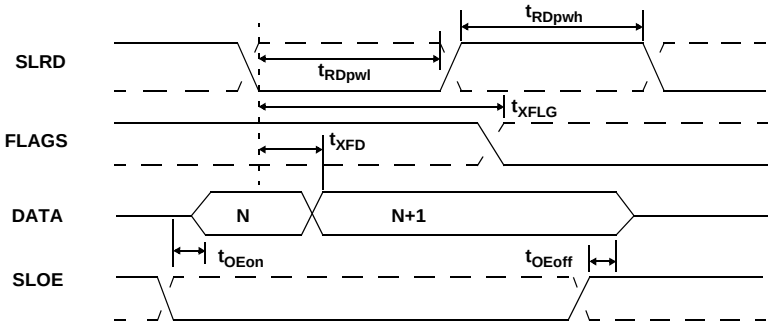


Table 22. Slave FIFO Asynchronous Read Parameters[27]

Parameter	Description	Min	Max	Unit
t_{RDpwl}	SLRD pulse width LOW	50	–	ns
t_{RDpwh}	SLRD pulse width HIGH	50	–	ns
t_{XFLG}	SLRD to FLAGS output propagation delay	–	70	ns
t_{XFD}	SLRD to FIFO data output propagation delay	–	15	ns
t_{OEon}	SLOE turn-on to FIFO data valid	–	10.5	ns
t_{OEoff}	SLOE turn-off to FIFO data hold	–	10.5	ns

Note
27. Slave FIFO asynchronous parameter values use internal IFCLK setting at 48 MHz.

Slave FIFO Synchronous Write

Figure 21. Slave FIFO Synchronous Write Timing Diagram[24]

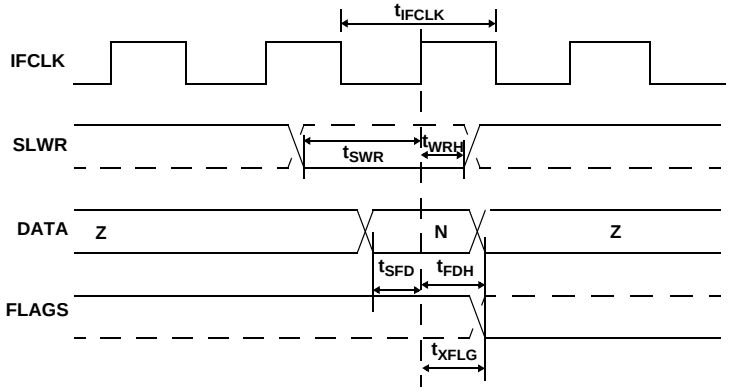


Table 23. Slave FIFO Synchronous Write Parameters with Internally Sourced IFCLK[25]

Parameter	Description	Min	Max	Unit
t_{IFCLK}	IFCLK period	20.83	–	ns
t_{SWR}	SLWR to clock setup time	10.4	–	ns
t_{WRH}	Clock to SLWR hold time	0	–	ns
t_{SFD}	FIFO data to clock setup time	9.2	–	ns
t_{FDH}	Clock to FIFO data hold time	0	–	ns
t_{XFLG}	Clock to FLAGS output propagation time	–	9.5	ns

Table 24. Slave FIFO Synchronous Write Parameters with Externally Sourced IFCLK[25]

Parameter	Description	Min	Max	Unit
t_{IFCLK}	IFCLK Period	20.83	200	ns
t_{SWR}	SLWR to clock setup time	12.1	–	ns
t_{WRH}	Clock to SLWR hold time	3.6	–	ns
t_{SFD}	FIFO data to clock setup time	3.2	–	ns
t_{FDH}	Clock to FIFO data hold time	4.5	–	ns
t_{XFLG}	Clock to FLAGS output propagation time	–	13.5	ns

Slave FIFO Asynchronous Write

Figure 22. Slave FIFO Asynchronous Write Timing Diagram[24]

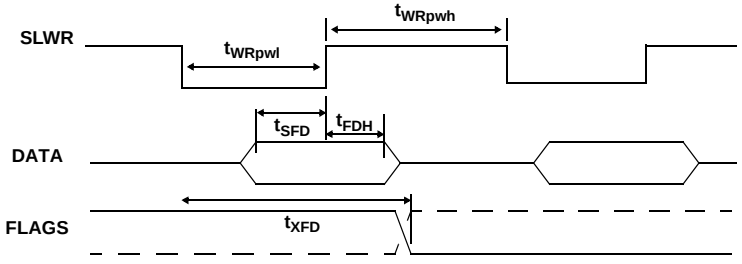


Table 25. Slave FIFO Asynchronous Write Parameters with Internally Sourced IFCLK[27]

Parameter	Description	Min	Max	Unit
t_{WRpwl}	SLWR pulse LOW	50	–	ns
t_{WRpwh}	SLWR pulse HIGH	70	–	ns
t_{SFD}	SLWR to FIFO DATA setup time	10	–	ns
t_{FDH}	FIFO DATA to SLWR hold time	10	–	ns
t_{XFD}	SLWR to FLAGS output propagation delay	–	70	ns

Slave FIFO Synchronous Packet End Strobe

Figure 23. Slave FIFO Synchronous Packet End Strobe Timing Diagram[24]

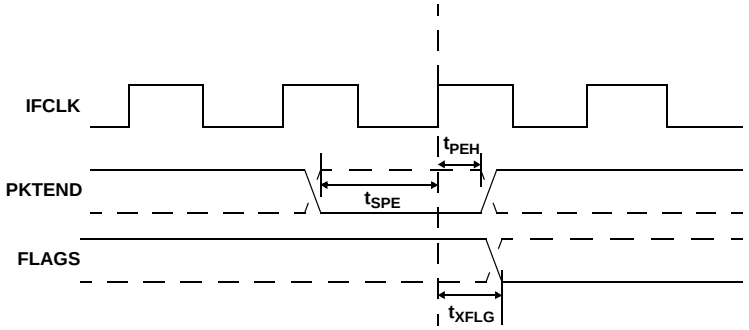


Table 26. Slave FIFO Synchronous Packet End Strobe Parameters with Internally Sourced IFCLK[25]

Parameter	Description	Min	Max	Unit
t_{IFCLK}	IFCLK period	20.83	–	ns
t_{SPE}	PKTEND to clock setup time	14.6	–	ns
t_{PEH}	Clock to PKTEND hold time	0	–	ns
t_{XFLG}	Clock to FLAGS output propagation delay	–	9.5	ns

Table 27. Slave FIFO Synchronous Packet End Strobe Parameters with Externally Sourced IFCLK[25]

Parameter	Description	Min	Max	Unit
t_{IFCLK}	IFCLK period	20.83	200	ns
t_{SPE}	PKTEND to clock setup time	8.6	–	ns
t_{PEH}	Clock to PKTEND hold time	2.5	–	ns
t_{XFLG}	Clock to FLAGS output propagation delay	–	13.5	ns

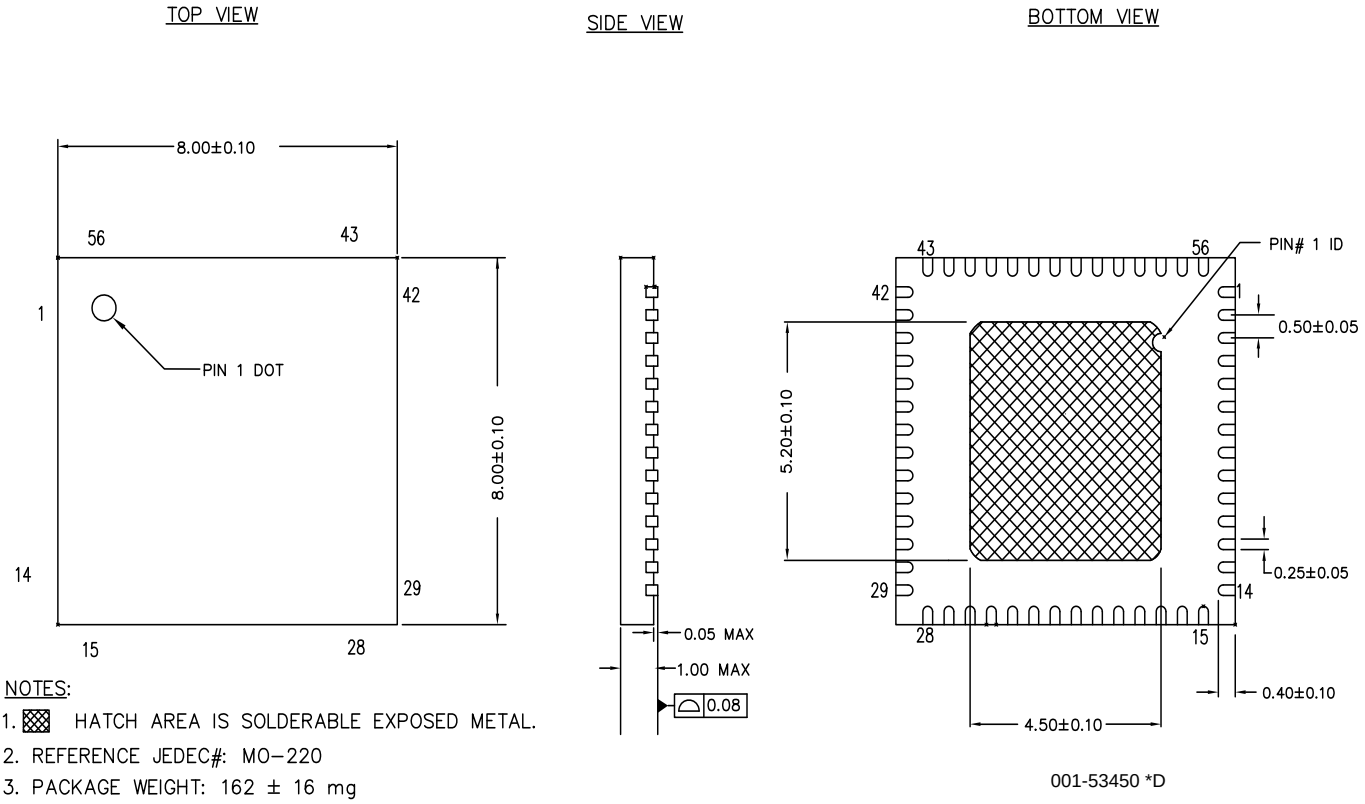
There is no specific timing requirement that should be met for asserting the PKTEND pin to asserting SLWR. PKTEND can be asserted with the last data value clocked into the FIFOs or thereafter. The setup time t_{SPE} and the hold time t_{PEH} must be met.

Although there are no specific timing requirements for PKTEND assertion, there is a specific corner-case condition that needs attention while using the PKTEND pin to commit a one byte or word packet. There is an additional timing requirement that needs to be met when the FIFO is configured to operate in auto mode and it is required to send two packets back to back: a full packet (full defined as the number of bytes in the FIFO meeting the level set in AUTOINLEN register) committed automatically followed by a short one byte or word packet committed manually using the PKTEND pin. In this scenario, the user must ensure to assert PKTEND, at least one clock cycle after the rising edge that caused the last byte or word to be clocked into the previous auto committed packet. Figure 24 shows this scenario. X is the value the AUTOINLEN register is set to when the IN endpoint is configured to be in auto mode.

Figure 24 shows a scenario where two packets are committed. The first packet gets committed automatically when the number of bytes in the FIFO reaches X (value set in AUTOINLEN register) and the second one byte/word short packet being committed manually using PKTEND.

Note that there is at least one IFCLK cycle timing between the assertion of PKTEND and clocking of the last byte of the previous packet (causing the packet to be committed automatically). Failing to adhere to this timing results in the FX2 failing to send the one byte or word short packet.

Figure 37. 56-Pin QFN 8 × 8 mm Sawn Version (001-53450)



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO–220
3. PACKAGE WEIGHT: 162 ± 16 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

Figure 38. 100-Pin Thin Plastic Quad Flatpack (14 × 20 × 1.4 mm) A100RA (51-85050)

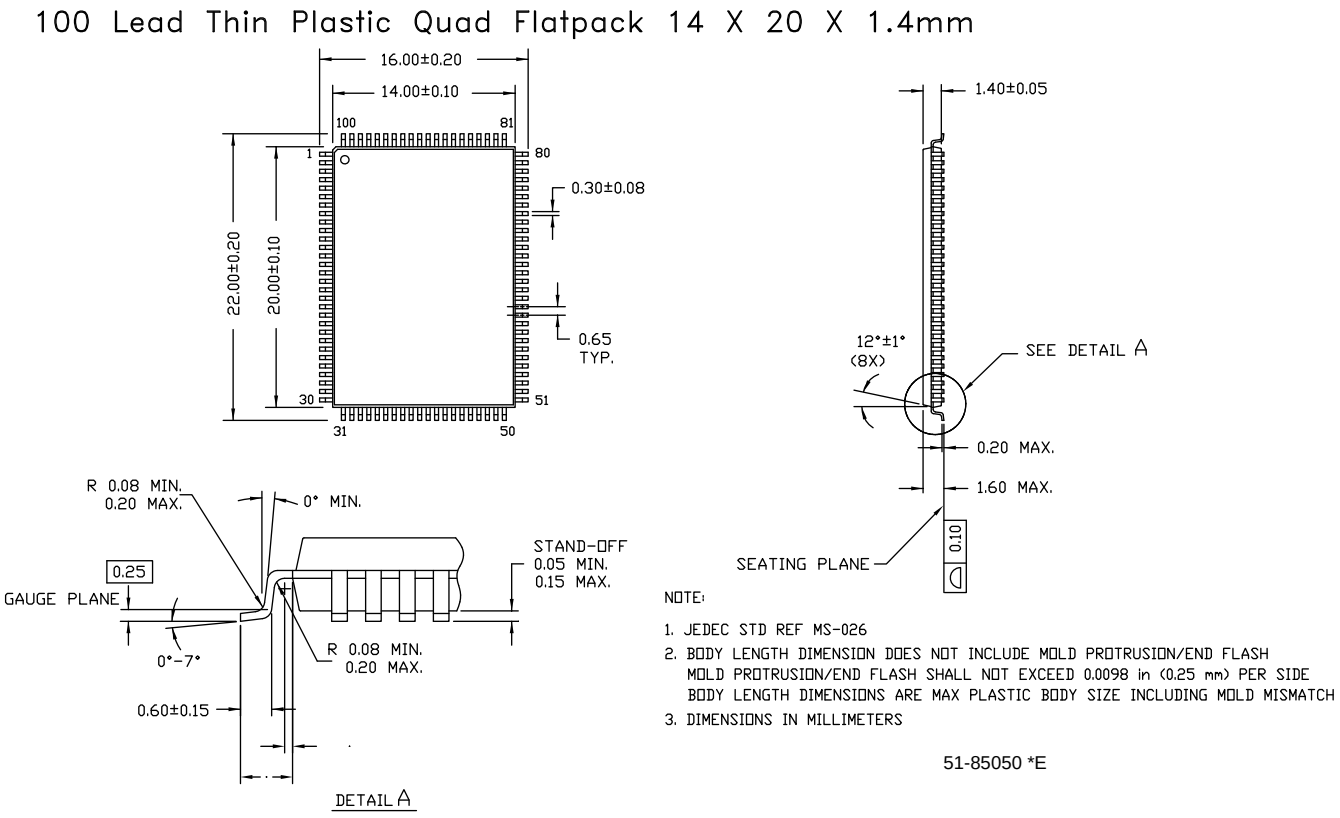
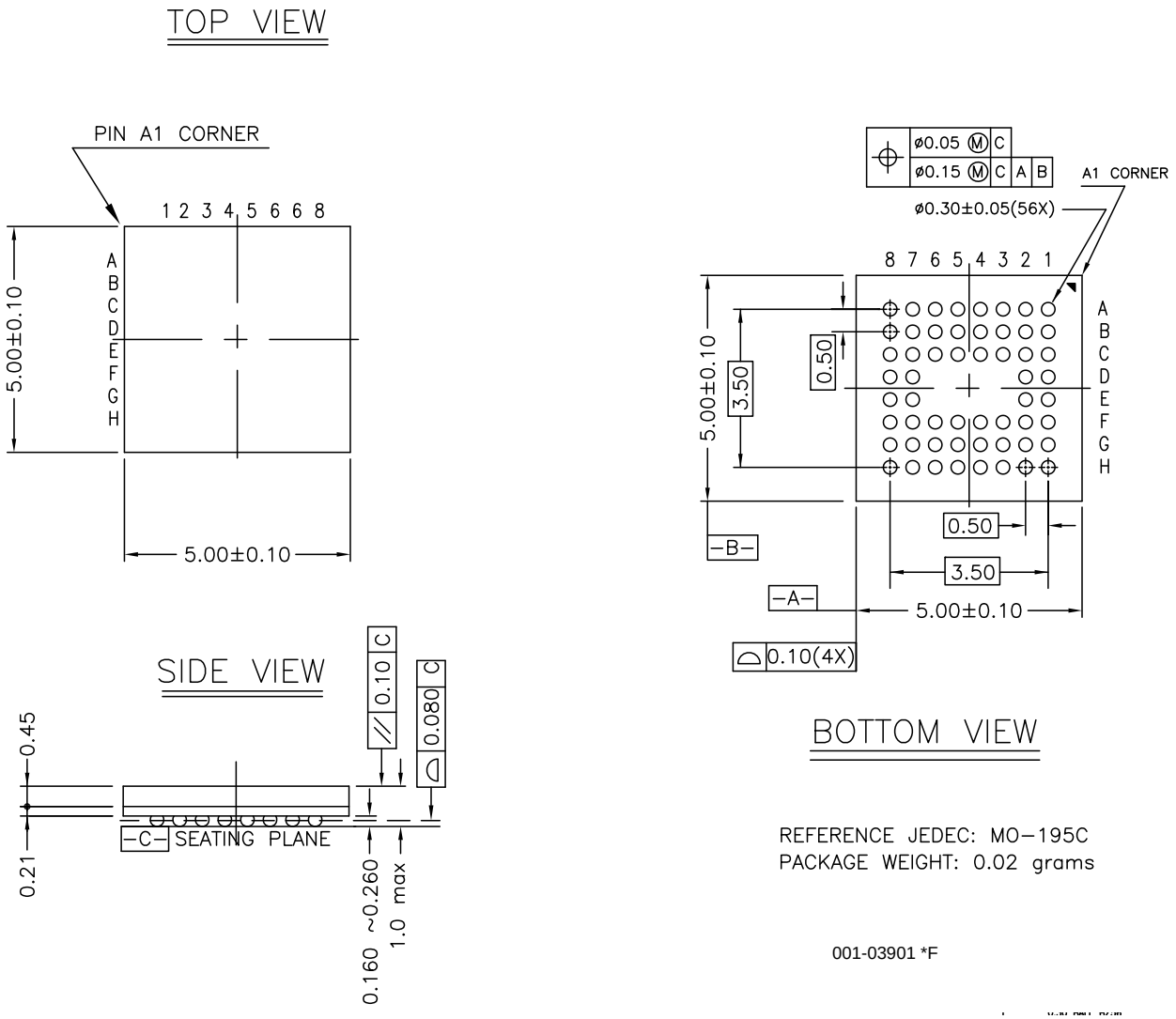


Figure 40. 56-Pin VFBGA (5 × 5 × 1.0 mm) 0.50 Pitch, 0.30 Ball BZ56 (001-03901)



Document History Page (continued)

Document Title: CY7C68013A, CY7C68014A, CY7C68015A, CY7C68016A, EZ-USB® FX2LP™ USB Microcontroller High-Speed USB Peripheral Controller Document Number: 38-08032				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*W	3998554	GAYA	07/19/2013	Added Errata footnote (Note 3). Updated Functional Overview: Updated Interrupt System: Updated FIFO/GPIF Interrupt (INT4): Added Note 3 and referred the same note in “Endpoint 2 empty flag” in Table 4. Updated Package Diagrams: spec 51-85062 – Changed revision from *E to *F. spec 001-53450 – Changed revision from *B to *C. Added Errata. Updated in new template.
*X	4617527	GAYA	01/15/2015	Updated Figure 13 Added a note to sections Data Memory Read[21] and Data Memory Write[23] sections Updated template to include the More Information section Updated Figure 37, Figure 38, Figure 39 Updated Table 11 with Reset state information for pins Sunset Review
*Y	5317277	ODC	06/28/2016	Updated CY Logo and Sales Disclaimer.