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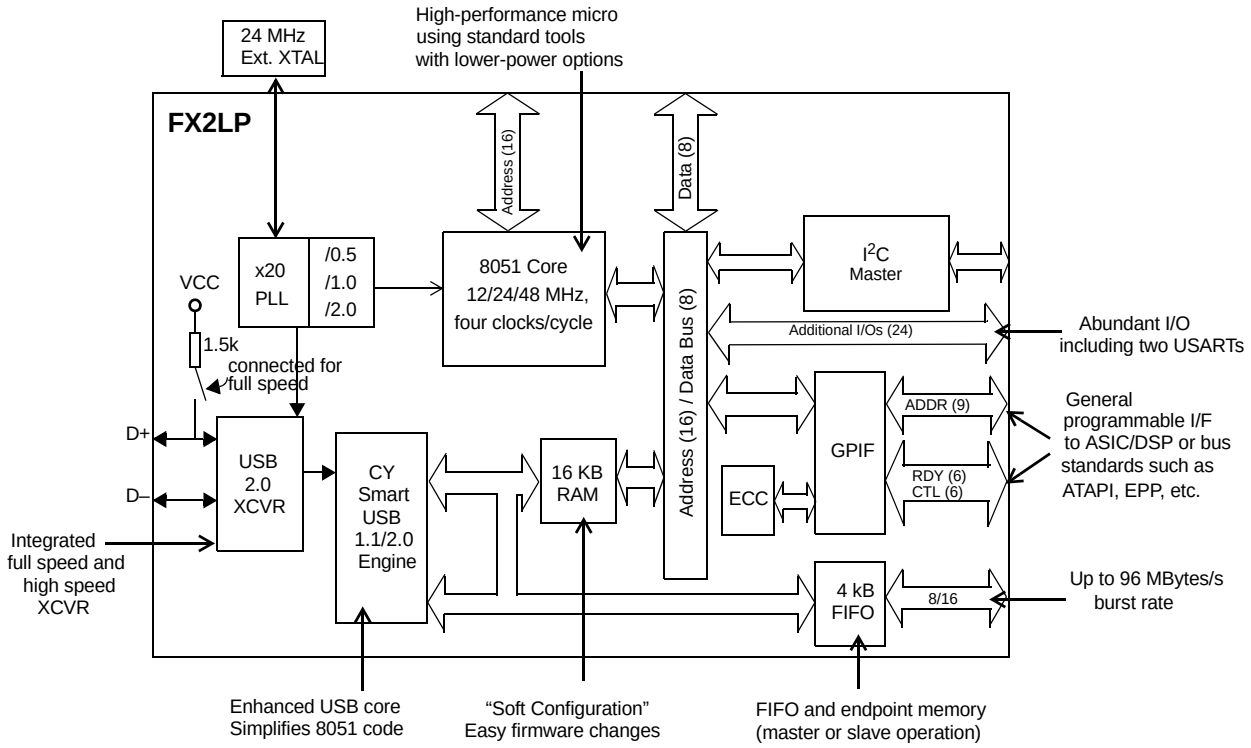
What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	USB Microcontroller
Core Processor	8051
Program Memory Type	ROMless
Controller Series	CY7C680xx
RAM Size	16K x 8
Interface	I²C, USB, USART
Number of I/O	24
Voltage - Supply	3V ~ 3.6V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	56-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	56-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c68014a-56pvxc

Logic Block Diagram



Cypress's EZ-USB® FX2LP™ (CY7C68013A/14A) is a low-power version of the EZ-USB FX2™ (CY7C68013), which is a highly integrated, low-power USB 2.0 microcontroller. By integrating the USB 2.0 transceiver, serial interface engine (SIE), enhanced 8051 microcontroller, and a programmable peripheral interface in a single chip, Cypress has created a cost-effective solution that provides superior time-to-market advantages with low power to enable bus-powered applications.

The ingenious architecture of FX2LP results in data transfer rates of over 53 Mbytes per second (the maximum allowable USB 2.0 bandwidth), while still using a low-cost 8051 microcontroller in a package as small as a 56 VFBGA (5 mm x 5 mm). Because it incorporates the USB 2.0 transceiver, the FX2LP is more economical, providing a smaller-footprint solution than a USB 2.0 SIE or external transceiver implementations.

With EZ-USB FX2LP, the Cypress Smart SIE handles most of the USB 1.1 and 2.0 protocol in hardware, freeing the embedded microcontroller for application-specific functions and decreasing the development time to ensure USB compatibility.

The general programmable interface (GPIF) and Master/Slave Endpoint FIFO (8-bit or 16-bit data bus) provide an easy and glueless interface to popular interfaces such as ATA, UTOPIA, EPP, PCMCIA, and most DSP/processors.

The FX2LP draws less current than the FX2 (CY7C68013), has double the on-chip code/data RAM, and is fit, form, and function compatible with the 56-, 100-, and 128-pin FX2.

Five packages are defined for the family: 56 VFBGA, 56 SSOP, 56 QFN, 100 TQFP, and 128 TQFP.

Contents

The FX2LP jump instruction is encoded as follows:.

Table 3. INT2 USB Interrupts

USB INTERRUPT TABLE FOR INT2			
Priority	**INT2VEC Value**	**Source**	**Notes**
1	00	SUDAV	Setup data available
2	04	SOF	Start of frame (or microframe)
3	08	SUTOK	Setup token received
4	0C	SUSPEND	USB suspend request
5	10	USB RESET	Bus reset
6	14	HISPEED	Entered high speed operation
7	18	EP0ACK	FX2LP ACK'd the CONTROL Handshake
8	1C		reserved
9	20	EP0-IN	EP0-IN ready to be loaded with data
10	24	EP0-OUT	EP0-OUT has USB data
11	28	EP1-IN	EP1-IN ready to be loaded with data
12	2C	EP1-OUT	EP1-OUT has USB data
13	30	EP2	IN: buffer available. OUT: buffer has data
14	34	EP4	IN: buffer available. OUT: buffer has data
15	38	EP6	IN: buffer available. OUT: buffer has data
16	3C	EP8	IN: buffer available. OUT: buffer has data
17	40	IBN	IN-Bulk-NAK (any IN endpoint)
18	44		reserved
19	48	EP0PING	EP0 OUT was pinged and it NAK'd
20	4C	EP1PING	EP1 OUT was pinged and it NAK'd
21	50	EP2PING	EP2 OUT was pinged and it NAK'd
22	54	EP4PING	EP4 OUT was pinged and it NAK'd
23	58	EP6PING	EP6 OUT was pinged and it NAK'd
24	5C	EP8PING	EP8 OUT was pinged and it NAK'd
25	60	ERRLIMIT	Bus errors exceeded the programmed limit
26	64	–	–
27	68	–	Reserved
28	6C	–	Reserved
29	70	EP2ISOERR	ISO EP2 OUT PID sequence error
30	74	EP4ISOERR	ISO EP4 OUT PID sequence error
31	78	EP6ISOERR	ISO EP6 OUT PID sequence error
32	7C	EP8ISOERR	ISO EP8 OUT PID sequence error

If Autovectoring is enabled (AV2EN = 1 in the INTSET-UP register), the FX2LP substitutes its INT2VEC byte. Therefore, if the high byte ("page") of a jump table address is preloaded at the location 0x0044, the automatically inserted INT2VEC byte at 0x0045 directs the jump to the correct address out of the 27 addresses within the page.

FIFO/GPIF Interrupt (INT4)

Just as the USB Interrupt is shared among 27 individual USB interrupt sources, the FIFO/GPIF interrupt is shared among 14 individual FIFO/GPIF sources. The FIFO/GPIF Interrupt, similar to the USB Interrupt, can employ autovectoring.

Table 4 on page 8 shows the priority and INT4VEC values for the 14 FIFO/GPIF interrupt sources.

Reset and Wakeup

Reset Pin

The input pin, RESET#, resets the FX2LP when asserted. This pin has hysteresis and is active LOW. When a crystal is used with the CY7C680xxA, the reset period must enable stabilization of the crystal and the PLL. This reset period must be approximately 5 ms after VCC reaches 3.0 V. If the crystal input pin is driven by a clock signal, the internal PLL stabilizes in 200 µs after VCC has reached 3.0 V[4].

Figure 2 on page 9 shows a power-on reset condition and a reset applied during operation. A power-on reset is defined as the time reset that is asserted while power is being applied to the circuit. A powered reset is when the FX2LP is powered on and operating and the RESET# pin is asserted.

Cypress provides an application note which describes and recommends power-on reset implementation. For more information about reset implementation for the FX2 family of products, visit http://www.cypress.com.

Figure 2. Reset Timing Plots

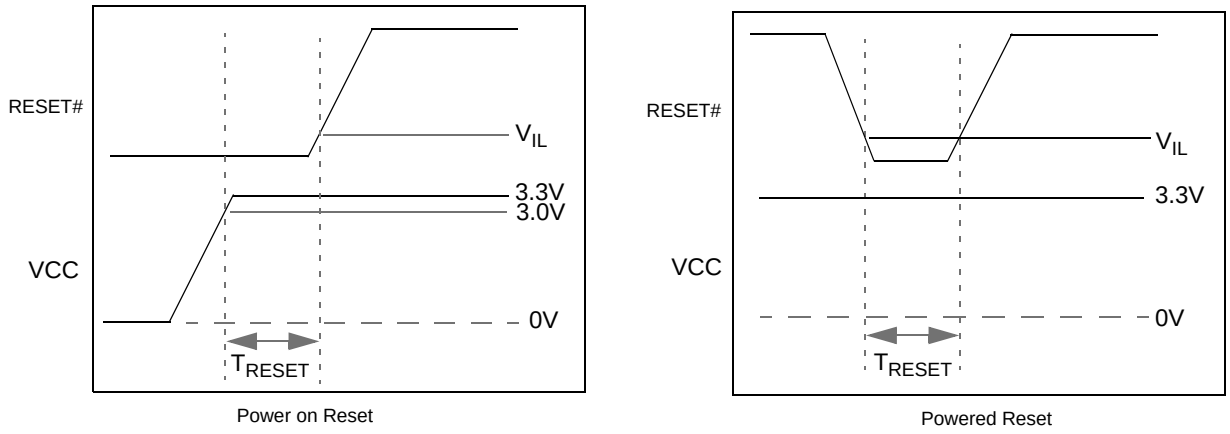


Table 5. Reset Timing Values

Condition	T_{RESET}
Power-on reset with crystal	5 ms
Power-on reset with external clock	200 µs + clock stability time
Powered reset	200 µs

Wakeup Pins

The 8051 puts itself and the rest of the chip into a power-down mode by setting PCON.0 = 1. This stops the oscillator and PLL. When WAKEUP is asserted by external logic, the oscillator restarts after the PLL stabilizes, and the 8051 receives a wakeup interrupt. This applies irrespective of whether FX2LP is connected to the USB.

The FX2LP exits the power-down (USB suspend) state by using one of the following methods:

- USB bus activity (if D+/D– lines are left floating, noise on these lines may indicate activity to the FX2LP and initiate a wakeup)
- External logic asserts the WAKEUP pin
- External logic asserts the PA3/WU2 pin

The second wakeup pin, WU2, can also be configured as a general-purpose I/O pin. This enables a simple external R-C network to be used as a periodic wakeup source. WAKEUP is by default active LOW.

Autopointer Access

FX2LP provides two identical autopointers. They are similar to the internal 8051 data pointers but with an additional feature: they can optionally increment after every memory access. This capability is available to and from both internal and external RAM. Autopointers are available in external FX2LP registers under the control of a mode bit (AUTOPTRSET-UP.0). Using the external FX2LP autopointer access (at 0xE67B – 0xE67C) enables the autopointer to access all internal and external RAM to the part.

Also, autopointers can point to any FX2LP register or endpoint buffer space. When the autopointer access to external memory is enabled, locations 0xE67B and 0xE67C in XDATA and code space cannot be used.

I²C Controller

FX2LP has one I²C port that is driven by two internal controllers, the one that automatically operates at boot time to load VID/PID/DID and configuration information, and another that the 8051 uses when running to control external I²C devices. The I²C port operates in master mode only.

I²C Port Pins

The I²C pins SCL and SDA must have external 2.2-kΩ pull-up resistors even if no EEPROM is connected to the FX2LP. External EEPROM device address pins must be configured properly. See Table 8 for configuring the device address pins.

Table 8. Strap Boot EEPROM Address Lines to These Values

Bytes	Example EEPROM	A2	A1	A0
16	24LC00[10]	N/A	N/A	N/A
128	24LC01	0	0	0
256	24LC02	0	0	0
4K	24LC32	0	0	1
8K	24LC64	0	0	1
16K	24LC128	0	0	1

I²C Interface Boot Load Access

At power-on reset, the I²C interface boot loader loads the VID/PID/DID configuration bytes and up to 16 KB of program/data. The available RAM spaces are 16 KB from 0x0000–0x3FFF and 512 bytes from 0xE000–0xE1FF. The 8051 is in reset. I²C interface boot loads only occur after power-on reset.

I²C Interface General-Purpose Access

The 8051 can control peripherals connected to the I²C bus using the I2CTL and I2DAT registers. FX2LP provides I²C master control only; it is never an I²C slave.

Compatible with Previous Generation EZ-USB FX2

The EZ-USB FX2LP is form-, fit-, and with minor exceptions, functionally-compatible with its predecessor, the EZ-USB FX2.

This makes for an easy transition for designers wanting to upgrade their systems from the FX2 to the FX2LP. The pinout and package selection are identical and a vast majority of firmware previously developed for the FX2 functions in the FX2LP.

For designers migrating from the FX2 to the FX2LP, a change in the bill of material and review of the memory allocation (due to increased internal memory) is required. For more information about migrating from EZ-USB FX2 to EZ-USB FX2LP, see the application note titled *Migrating from EZ-USB FX2 to EZ-USB FX2LP* available in the Cypress web site.

Table 9. Part Number Conversion Table

EZ-USB FX2 Part Number	EZ-USB FX2LP Part Number	Package Description
CY7C68013-56PVC	CY7C68013A-56PVXC or CY7C68014A-56PVXC	56-pin SSOP
CY7C68013-56PVCT	CY7C68013A-56PVXCT or CY7C68014A-56PVXCT	56-pin SSOP – Tape and Reel
CY7C68013-56LFC	CY7C68013A-56LFXC or CY7C68014A-56LFXC	56-pin QFN
CY7C68013-100AC	CY7C68013A-100AXC or CY7C68014A-100AXC	100-pin TQFP
CY7C68013-128AC	CY7C68013A-128AXC or CY7C68014A-128AXC	128-pin TQFP

CY7C68013A/14A and CY7C68015A/16A Differences

CY7C68013A is identical to CY7C68014A in form, fit, and functionality. CY7C68015A is identical to CY7C68016A in form, fit, and functionality. CY7C68014A and CY7C68016A have a lower suspend current than CY7C68013A and CY7C68015A respectively and are ideal for power-sensitive battery applications.

CY7C68015A and CY7C68016A are available in 56-pin QFN package only. Two additional GPIO signals are available on the CY7C68015A and CY7C68016A to provide more flexibility when neither IFCLK or CLKOUT are needed in the 56-pin package.

USB developers wanting to convert their FX2 56-pin application to a bus-powered system directly benefit from these additional signals. The two GPIOs give developers the signals they need for the power-control circuitry of their bus-powered application without pushing them to a high-pincount version of FX2LP.

The CY7C68015A is only available in the 56-pin QFN package

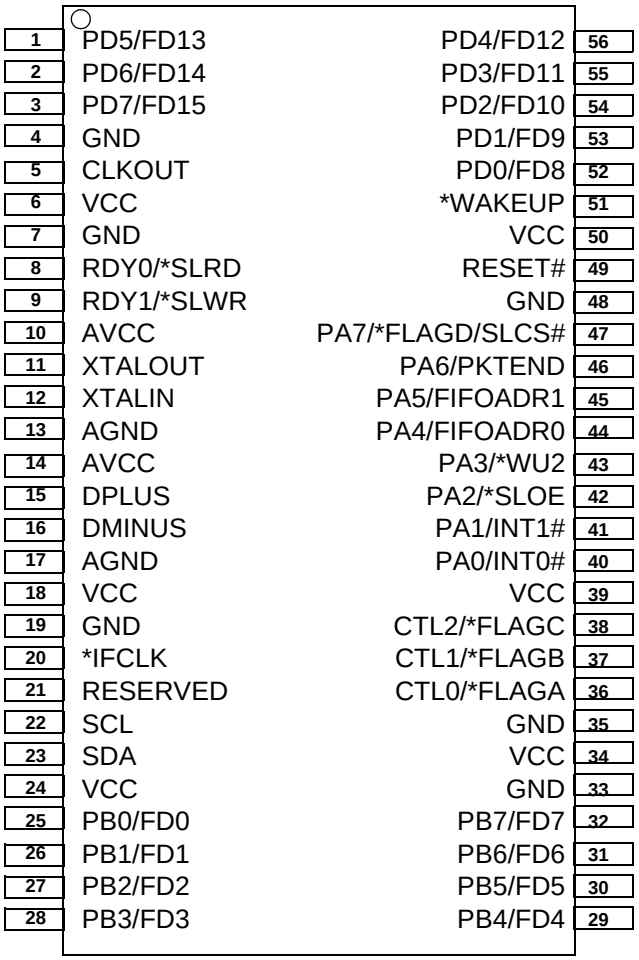
Table 10. CY7C68013A/14A and CY7C68015A/16A Pin Differences

CY7C68013A/CY7C68014A	CY7C68015A/CY7C68016A
IFCLK	PE0
CLKOUT	PE1

Note
10. This EEPROM does not have address pins.

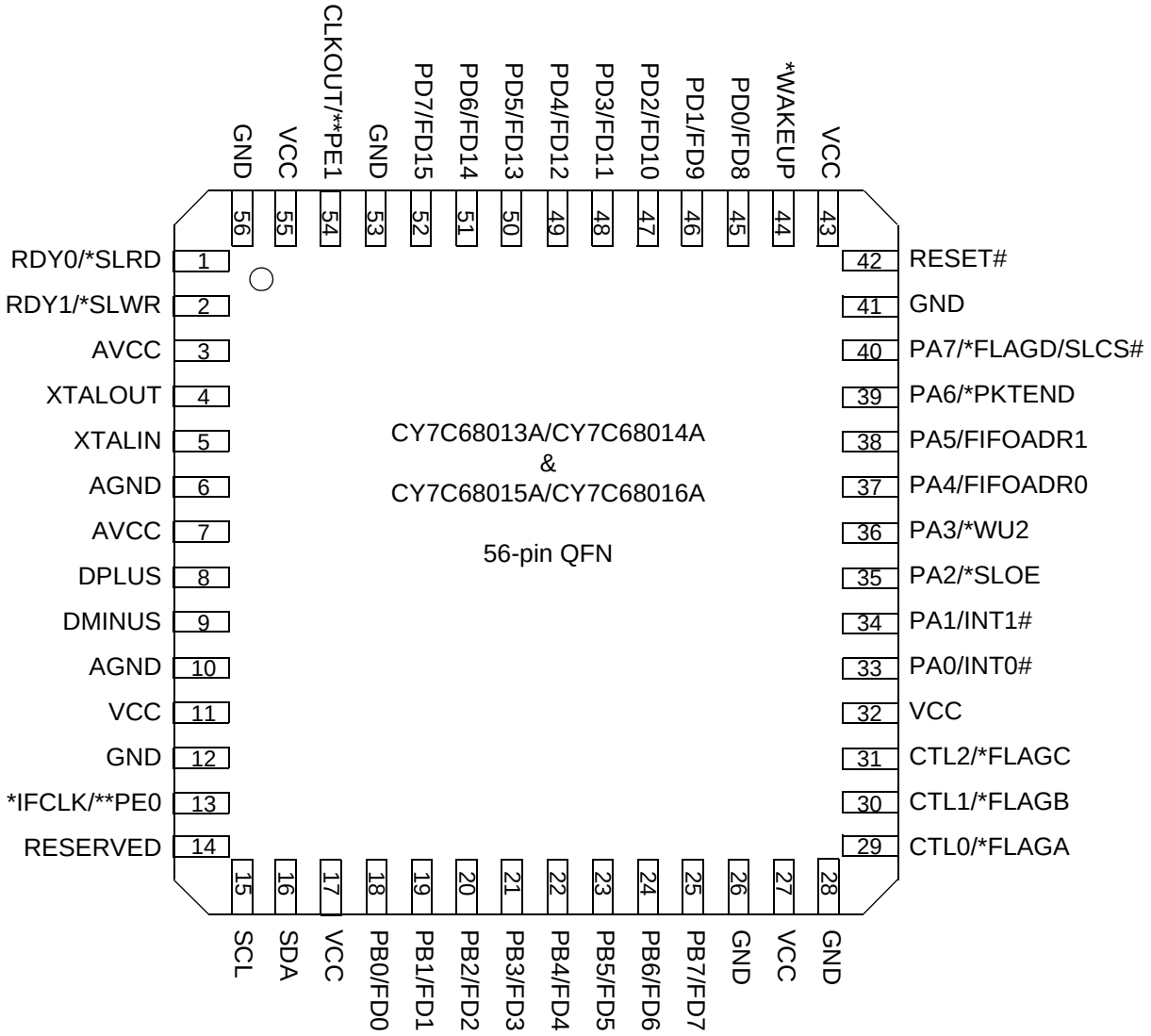
Figure 9. CY7C68013A/CY7C68014A 56-Pin SSOP Pin Assignment

CY7C68013A/CY7C68014A
56-pin SSOP



* denotes programmable polarity

Figure 10. CY7C68013A/14A/15A/16A 56-Pin QFN Pin Assignment



* denotes programmable polarity
** denotes CY7C68015A/CY7C68016A pinout

Table 11. FX2LP Pin Descriptions[11] (continued)

128 TQFP	100 TQFP	56 SSOP	56 QFN	56 VFBGA	Name	Type	Default	Reset[12]	Description
34	28	–	–		BKPT	Output	L	L	**Breakpoint**. This pin goes active (HIGH) when the 8051 address bus matches the BPADDRH/L registers and breakpoints are enabled in the BREAKPT register (BPEN = 1). If the BPPULSE bit in the BREAKPT register is HIGH, this signal pulses HIGH for eight 12-/24-/48-MHz clocks. If the BPPULSE bit is LOW, the signal remains HIGH until the 8051 clears the BREAK bit (by writing 1 to it) in the BREAKPT register.
99	77	49	42	8B	RESET#	Input	N/A	N/A	**Active LOW Reset**. Resets the entire chip. See section "Reset and Wakeup" on page 9 for more details.
35	–	–	–	–	EA	Input	N/A	N/A	**External Access**. This pin determines where the 8051 fetches code between addresses 0x0000 and 0x3FFF. If EA = 0 the 8051 fetches this code from its internal RAM. IF EA = 1 the 8051 fetches this code from external memory.
12	11	12	5	1C	XTALIN	Input	N/A	N/A	**Crystal Input**. Connect this signal to a 24-MHz parallel-resonant, fundamental mode crystal and load capacitor to GND. It is also correct to drive XTALIN with an external 24-MHz square wave derived from another clock source. When driving from an external source, the driving signal should be a 3.3-V square wave.
11	10	11	4	2C	XTALOUT	Output	N/A	N/A	**Crystal Output**. Connect this signal to a 24-MHz parallel-resonant, fundamental mode crystal and load capacitor to GND. If an external clock is used to drive XTALIN, leave this pin open.
1	100	5	54	2B	CLKOUT on CY7C68013A and CY7C68014A ---------- PE1 on CY7C68015A and CY7C68016A	O/Z ---------- I/O/Z	12 MHz ---------- I	Clock Driven ---------- Z	**CLKOUT:** 12-, 24- or 48-MHz clock, phase-locked to the 24-MHz input clock. The 8051 defaults to 12-MHz operation. The 8051 may three-state this output by setting CPUCS.1 = 1. ---------- ------**PE1** is a bidirectional I/O port pin.
Port A									
82	67	40	33	8G	PA0 or INT0#	I/O/Z	I (PA0)	Z (PA0)	Multiplexed pin whose function is selected by PORTACFG.0 **PA0** is a bidirectional I/O port pin. **INT0#** is the active-LOW 8051 INT0 interrupt input signal, which is either edge-triggered (IT0 = 1) or level-triggered (IT0 = 0).
83	68	41	34	6G	PA1 or INT1#	I/O/Z	I (PA1)	Z (PA1)	Multiplexed pin whose function is selected by: PORTACFG.1 **PA1** is a bidirectional I/O port pin. **INT1#** is the active-LOW 8051 INT1 interrupt input signal, which is either edge-triggered (IT1 = 1) or level-triggered (IT1 = 0).

Table 11. FX2LP Pin Descriptions[11] (continued)

128 TQFP	100 TQFP	56 SSOP	56 QFN	56 VFBGA	Name	Type	Default	Reset[12]	Description
100	78	50	43	5B	VCC	Power	N/A	N/A	**VCC**. Connect to the 3.3-V power source.
107	85	–	–	–	VCC	Power	N/A	N/A	**VCC**. Connect to the 3.3-V power source.
3	2	7	56	4B	GND	Ground	N/A	N/A	**Ground**
27	21	19	12	1H	GND	Ground	N/A	N/A	**Ground**
49	39	–	–	–	GND	Ground	N/A	N/A	**Ground**
58	48	33	26	7D	GND	Ground	N/A	N/A	**Ground**
65	50	35	28	8D	GND	Ground	N/A	N/A	**Ground**
80	65	–	–	–	GND	Ground	N/A	N/A	**Ground**
93	75	48	41	4C	GND	Ground	N/A	N/A	**Ground**
116	94	–	–	–	GND	Ground	N/A	N/A	**Ground**
125	99	4	53	4A	GND	Ground	N/A	N/A	**Ground**
14	13	–	–	–	NC	N/A	N/A	N/A	**No Connect**. This pin must be left open.
15	14	–	–	–	NC	N/A	N/A	N/A	**No Connect**. This pin must be left open.
16	15	–	–	–	NC	N/A	N/A	N/A	**No Connect**. This pin must be left open.

Table 12. FX2LP Register Summary (continued)

Hex	Size	Name	Description	b7	b6	b5	b4	b3	b2	b1	b0	Default	Access
E65D	1	USBIRQ[14]	USB Interrupt Requests	0	EP0ACK	HSGRANT	URES	SUSP	SUTOK	SOF	SUDAV	0xxxxxxx	rbbbbbbb
E65E	1	EPIE	Endpoint Interrupt Enables	EP8	EP6	EP4	EP2	EP1OUT	EP1IN	EP0OUT	EP0IN	00000000	RW
E65F	1	EPIRQ[14]	Endpoint Interrupt Requests	EP8	EP6	EP4	EP2	EP1OUT	EP1IN	EP0OUT	EP0IN	0	RW
E660	1	GPIFIE[13]	GPIF Interrupt Enable	0	0	0	0	0	0	GPIFWF	GPIFDONE	00000000	RW
E661	1	GPIFIRQ[13]	GPIF Interrupt Request	0	0	0	0	0	0	GPIFWF	GPIFDONE	000000xx	RW
E662	1	USBERRIE	USB Error Interrupt Enables	ISOEP8	ISOEP6	ISOEP4	ISOEP2	0	0	0	ERRLIMIT	00000000	RW
E663	1	USBERRIRQ[14]	USB Error Interrupt Requests	ISOEP8	ISOEP6	ISOEP4	ISOEP2	0	0	0	ERRLIMIT	0000000x	bbbbrrrb
E664	1	ERRCNTLIM	USB Error counter and limit	EC3	EC2	EC1	EC0	LIMIT3	LIMIT2	LIMIT1	LIMIT0	xxxx0100	rrrrbbbb
E665	1	CLRERRCNT	Clear Error Counter EC3:0	x	x	x	x	x	x	x	x	xxxxxxxx	W
E666	1	INT2IVEC	Interrupt 2 (USB) Autovector	0	I2V4	I2V3	I2V2	I2V1	I2V0	0	0	00000000	R
E667	1	INT4IVEC	Interrupt 4 (slave FIFO & GPIF) Autovector	1	0	I4V3	I4V2	I4V1	I4V0	0	0	10000000	R
E668	1	INTSET-UP	Interrupt 2&4 setup	0	0	0	0	AV2EN	0	INT4SRC	AV4EN	00000000	RW
E669	7	reserved											
		INPUT / OUTPUT											
E670	1	PORTACFG	I/O PORTA Alternate Configuration	FLAGD	SLCS	0	0	0	0	INT1	INT0	00000000	RW
E671	1	PORTCCFG	I/O PORTC Alternate Configuration	GPIFA7	GPIFA6	GPIFA5	GPIFA4	GPIFA3	GPIFA2	GPIFA1	GPIFA0	00000000	RW
E672	1	PORTECFG	I/O PORTE Alternate Configuration	GPIFA8	T2EX	INT6	RXD1OUT	RXD0OUT	T2OUT	T1OUT	T0OUT	00000000	RW
E673	4	reserved											
E677	1	reserved											
E678	1	I^2CS	I²C Bus Control & Status	START	STOP	LASTRD	ID1	ID0	BERR	ACK	DONE	000xx000	bbbrrrrr
E679	1	I2DAT	I²C Bus Data	d7	d6	d5	d4	d3	d2	d1	d0	xxxxxxxx	RW
E67A	1	I^2CTL	I²C Bus Control	0	0	0	0	0	0	STOPIE	400KHZ	00000000	RW
E67B	1	XAUTODAT1	Autoptr1 MOVX access, when APTREN=1	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
E67C	1	XAUTODAT2	Autoptr2 MOVX access, when APTREN=1	D7	D6	D5	D4	D3	D2	D1	D0	xxxxxxxx	RW
		UDMA CRC											
E67D	1	UDMACRCH[13]	UDMA CRC MSB	CRC15	CRC14	CRC13	CRC12	CRC11	CRC10	CRC9	CRC8	01001010	RW
E67E	1	UDMACRCL[13]	UDMA CRC LSB	CRC7	CRC6	CRC5	CRC4	CRC3	CRC2	CRC1	CRC0	10111010	RW
E67F	1	UDMACRC-QUALIFIER	UDMA CRC Qualifier	QENABLE	0	0	0	QSTATE	QSIGNAL2	QSIGNAL1	QSIGNAL0	00000000	brrrbbbb
		USB CONTROL											
E680	1	USBCS	USB Control & Status	HSM	0	0	0	DISCON	NOSYNSOF	RENUM	SIGRSUME	x0000000	rrrrbbbb
E681	1	SUSPEND	Put chip into suspend	x	x	x	x	x	x	x	x	xxxxxxxx	W
E682	1	WAKEUPCS	Wakeup Control & Status	WU2	WU	WU2POL	WUPOL	0	DPEN	WU2EN	WUEN	xx000101	bbbbrbbb
E683	1	TOGCTL	Toggle Control	Q	S	R	I/O	EP3	EP2	EP1	EP0	x0000000	rrrbbbbb
E684	1	USBFRAMEH	USB Frame count H	0	0	0	0	0	FC10	FC9	FC8	00000xxx	R
E685	1	USBFRAMEL	USB Frame count L	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0	xxxxxxxx	R
E686	1	MICROFRAME	Microframe count, 0-7	0	0	0	0	0	MF2	MF1	MF0	00000xxx	R
E687	1	FNADDR	USB Function address	0	FA6	FA5	FA4	FA3	FA2	FA1	FA0	0xxxxxxx	R
E688	2	reserved											
		ENDPOINTS											
E68A	1	EP0BCH[13]	Endpoint 0 Byte Count H	(BC15)	(BC14)	(BC13)	(BC12)	(BC11)	(BC10)	(BC9)	(BC8)	xxxxxxxx	RW
E68B	1	EP0BCL[13]	Endpoint 0 Byte Count L	(BC7)	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E68C	1	reserved											
E68D	1	EP1OUTBC	Endpoint 1 OUT Byte Count	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	0xxxxxxx	RW
E68E	1	reserved											
E68F	1	EP1INBC	Endpoint 1 IN Byte Count	0	BC6	BC5	BC4	BC3	BC2	BC1	BC0	0xxxxxxx	RW
E690	1	EP2BCH[13]	Endpoint 2 Byte Count H	0	0	0	0	0	BC10	BC9	BC8	00000xxx	RW
E691	1	EP2BCL[13]	Endpoint 2 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E692	2	reserved											
E694	1	EP4BCH[13]	Endpoint 4 Byte Count H	0	0	0	0	0	0	BC9	BC8	000000xx	RW
E695	1	EP4BCL[13]	Endpoint 4 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E696	2	reserved											
E698	1	EP6BCH[13]	Endpoint 6 Byte Count H	0	0	0	0	0	BC10	BC9	BC8	00000xxx	RW
E699	1	EP6BCL[13]	Endpoint 6 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E69A	2	reserved											
E69C	1	EP8BCH[13]	Endpoint 8 Byte Count H	0	0	0	0	0	0	BC9	BC8	000000xx	RW
E69D	1	EP8BCL[13]	Endpoint 8 Byte Count L	BC7/SKIP	BC6	BC5	BC4	BC3	BC2	BC1	BC0	xxxxxxxx	RW
E69E	2	reserved											

GPIF Synchronous Signals

Figure 18. GPIF Synchronous Signals Timing Diagram[24]

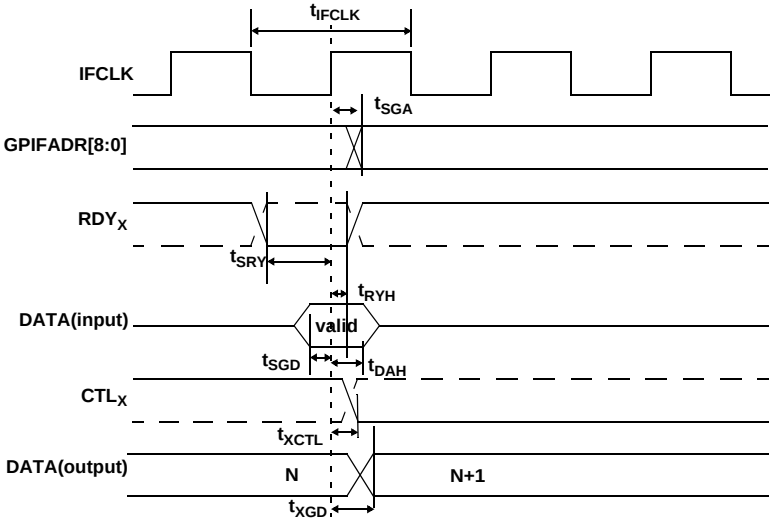


Table 18. GPIF Synchronous Signals Parameters with Internally Sourced IFCLK[24, 25]

Parameter	Description	Min	Max	Typ		Unit
				Min	Max	
t_{IFCLK}	IFCLK Period	20.83	–	–	–	ns
t_{SRY}	RDY_X to clock setup time	8.9	–	–	–	ns
t_{RYH}	Clock to RDY_X	0	–	–	–	ns
t_{SGD}	GPIF data to clock setup time	9.2	–	–	–	ns
t_{DAH}	GPIF data hold time	0	–	–	–	ns
t_{SGA}	Clock to GPIF address propagation delay	–	7.5	–	–	ns
t_{XGD}	Clock to GPIF data output propagation delay	–	11	–	–	ns
t_{XCTL}	Clock to CTL_X output propagation delay	–	6.7	–	–	ns
t_{IFCLKR}	IFCLK rise time	–	–	–	900	ps
t_{IFCLKF}	IFCLK fall time	–	–	–	900	ps
$t_{IFCLKOD}$	IFCLK output duty cycle	–	–	49	51	%
t_{IFCLKJ}	IFCLK jitter peak to peak	–	–	–	300	ps

Table 19. GPIF Synchronous Signals Parameters with Externally Sourced IFCLK[25]

Parameter	Description	Min	Max	Unit
t_{IFCLK}	IFCLK period[26]	20.83	200	ns
t_{SRY}	RDY_X to clock setup time	2.9	–	ns
t_{RYH}	Clock to RDY_X	3.7	–	ns
t_{SGD}	GPIF data to clock setup time	3.2	–	ns
t_{DAH}	GPIF data hold time	4.5	–	ns
t_{SGA}	Clock to GPIF address propagation delay	–	11.5	ns
t_{XGD}	Clock to GPIF data output propagation delay	–	15	ns
t_{XCTL}	Clock to CTL_X output propagation delay	–	10.7	ns

Notes
24. Dashed lines denote signals with programmable polarity.
25. GPIF asynchronous RDY_x signals have a minimum setup time of 50 ns when using the internal 48-MHz IFCLK.
26. IFCLK must not exceed 48 MHz.

Slave FIFO Synchronous Read

Figure 19. Slave FIFO Synchronous Read Timing Diagram[24]

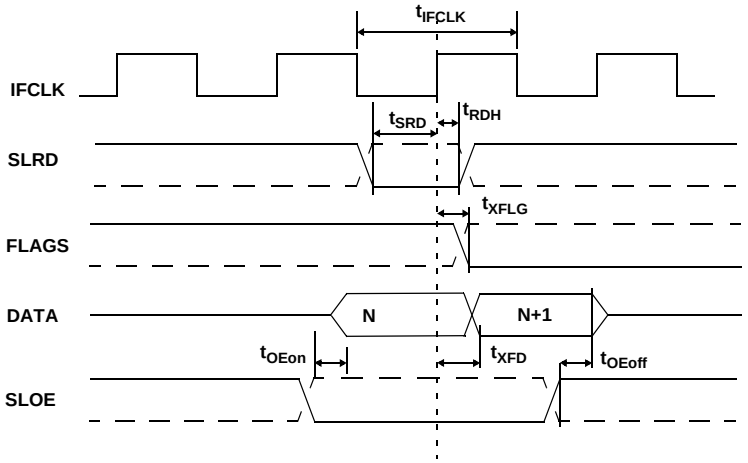


Table 20. Slave FIFO Synchronous Read Parameters with Internally Sourced IFCLK[25]

Parameter	Description	Min	Max	Typ		Unit
				Min	Max	
t_{IFCLK}	IFCLK period	20.83	–	–	–	ns
t_{SRD}	SLRD to clock setup time	18.7	–	–	–	ns
t_{RDH}	Clock to SLRD hold time	0	–	–	–	ns
t_{OEon}	SLOE turn on to FIFO data valid	–	10.5	–	–	ns
t_{OEoff}	SLOE turn off to FIFO data hold	–	10.5	–	–	ns
t_{XFLG}	Clock to FLAGS output propagation delay	–	9.5	–	–	ns
t_{XFD}	Clock to FIFO data output propagation delay	–	11	–	–	ns
t_{IFCLKR}	IFCLK rise time	–	–	–	900	ps
t_{IFCLKF}	IFCLK fall time	–	–	–	900	ps
$t_{IFCLKOD}$	IFCLK output duty cycle	–	–	49	51	%
t_{IFCLKJ}	IFCLK jitter peak to peak	–	–	–	300	ps

Slave FIFO Synchronous Write

Figure 21. Slave FIFO Synchronous Write Timing Diagram[24]

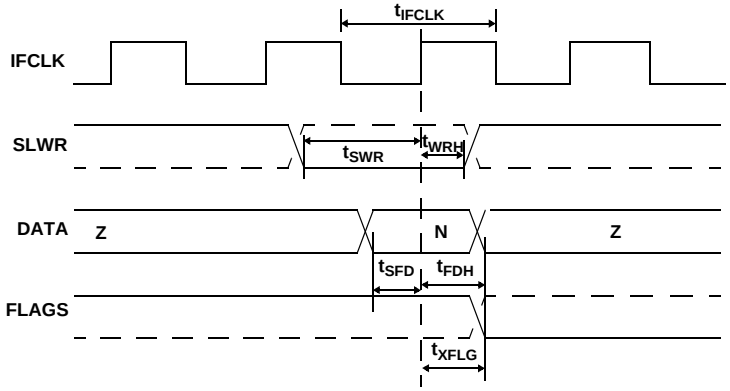


Table 23. Slave FIFO Synchronous Write Parameters with Internally Sourced IFCLK[25]

Parameter	Description	Min	Max	Unit
t_{IFCLK}	IFCLK period	20.83	–	ns
t_{SWR}	SLWR to clock setup time	10.4	–	ns
t_{WRH}	Clock to SLWR hold time	0	–	ns
t_{SFD}	FIFO data to clock setup time	9.2	–	ns
t_{FDH}	Clock to FIFO data hold time	0	–	ns
t_{XFLG}	Clock to FLAGS output propagation time	–	9.5	ns

Table 24. Slave FIFO Synchronous Write Parameters with Externally Sourced IFCLK[25]

Parameter	Description	Min	Max	Unit
t_{IFCLK}	IFCLK Period	20.83	200	ns
t_{SWR}	SLWR to clock setup time	12.1	–	ns
t_{WRH}	Clock to SLWR hold time	3.6	–	ns
t_{SFD}	FIFO data to clock setup time	3.2	–	ns
t_{FDH}	Clock to FIFO data hold time	4.5	–	ns
t_{XFLG}	Clock to FLAGS output propagation time	–	13.5	ns

Slave FIFO Asynchronous Write

Figure 22. Slave FIFO Asynchronous Write Timing Diagram[24]

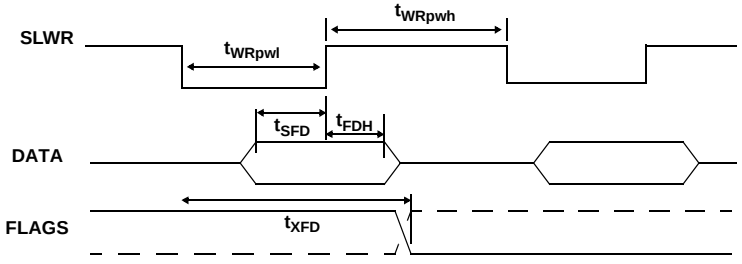


Table 25. Slave FIFO Asynchronous Write Parameters with Internally Sourced IFCLK[27]

Parameter	Description	Min	Max	Unit
t_{WRpwl}	SLWR pulse LOW	50	–	ns
t_{WRpwh}	SLWR pulse HIGH	70	–	ns
t_{SFD}	SLWR to FIFO DATA setup time	10	–	ns
t_{FDH}	FIFO DATA to SLWR hold time	10	–	ns
t_{XFD}	SLWR to FLAGS output propagation delay	–	70	ns

Slave FIFO Synchronous Packet End Strobe

Figure 23. Slave FIFO Synchronous Packet End Strobe Timing Diagram[24]

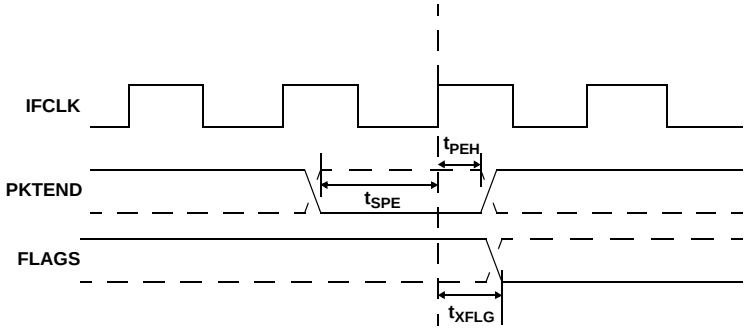


Table 26. Slave FIFO Synchronous Packet End Strobe Parameters with Internally Sourced IFCLK[25]

Parameter	Description	Min	Max	Unit
t_{IFCLK}	IFCLK period	20.83	–	ns
t_{SPE}	PKTEND to clock setup time	14.6	–	ns
t_{PEH}	Clock to PKTEND hold time	0	–	ns
t_{XFLG}	Clock to FLAGS output propagation delay	–	9.5	ns

Table 27. Slave FIFO Synchronous Packet End Strobe Parameters with Externally Sourced IFCLK[25]

Parameter	Description	Min	Max	Unit
t_{IFCLK}	IFCLK period	20.83	200	ns
t_{SPE}	PKTEND to clock setup time	8.6	–	ns
t_{PEH}	Clock to PKTEND hold time	2.5	–	ns
t_{XFLG}	Clock to FLAGS output propagation delay	–	13.5	ns

There is no specific timing requirement that should be met for asserting the PKTEND pin to asserting SLWR. PKTEND can be asserted with the last data value clocked into the FIFOs or thereafter. The setup time t_{SPE} and the hold time t_{PEH} must be met.

Although there are no specific timing requirements for PKTEND assertion, there is a specific corner-case condition that needs attention while using the PKTEND pin to commit a one byte or word packet. There is an additional timing requirement that needs to be met when the FIFO is configured to operate in auto mode and it is required to send two packets back to back: a full packet (full defined as the number of bytes in the FIFO meeting the level set in AUTOINLEN register) committed automatically followed by a short one byte or word packet committed manually using the PKTEND pin. In this scenario, the user must ensure to assert PKTEND, at least one clock cycle after the rising edge that caused the last byte or word to be clocked into the previous auto committed packet. Figure 24 shows this scenario. X is the value the AUTOINLEN register is set to when the IN endpoint is configured to be in auto mode.

Figure 24 shows a scenario where two packets are committed. The first packet gets committed automatically when the number of bytes in the FIFO reaches X (value set in AUTOINLEN register) and the second one byte/word short packet being committed manually using PKTEND.

Note that there is at least one IFCLK cycle timing between the assertion of PKTEND and clocking of the last byte of the previous packet (causing the packet to be committed automatically). Failing to adhere to this timing results in the FX2 failing to send the one byte or word short packet.

Sequence Diagram

Single and Burst Synchronous Read Example

Figure 30. Slave FIFO Synchronous Read Sequence and Timing Diagram[24]

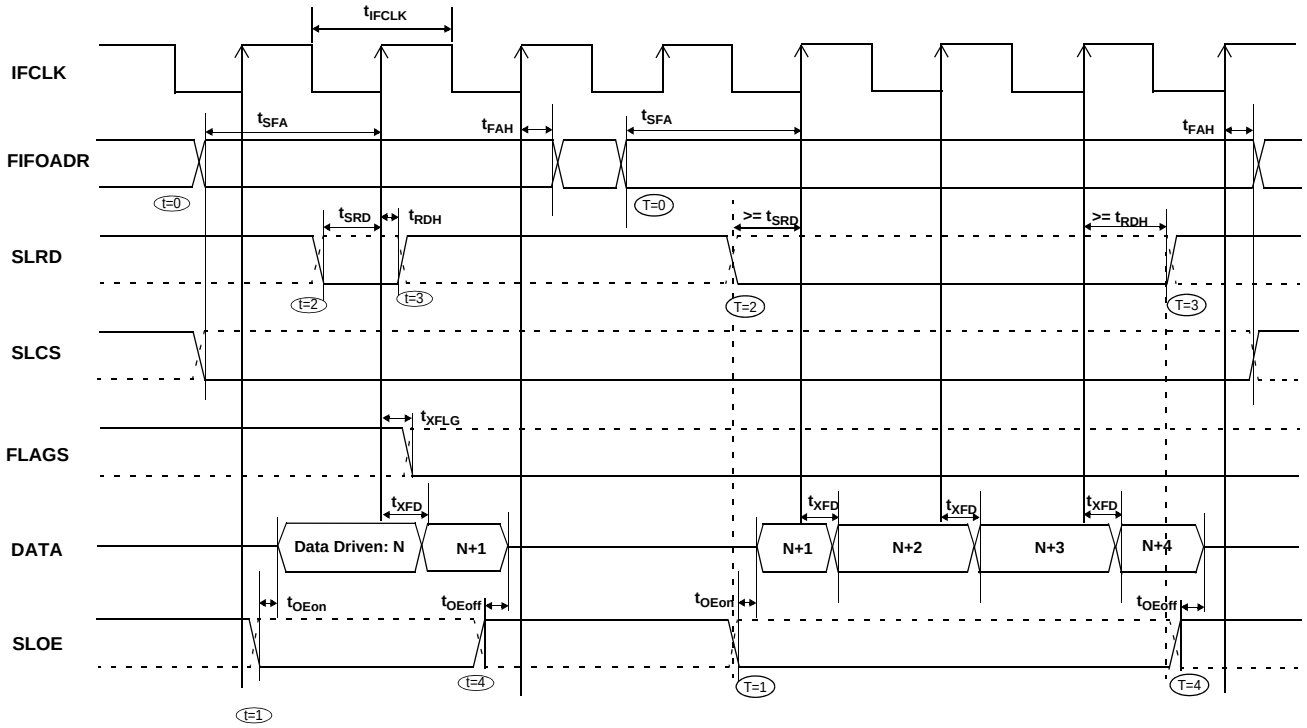


Figure 31. Slave FIFO Synchronous Sequence of Events Diagram

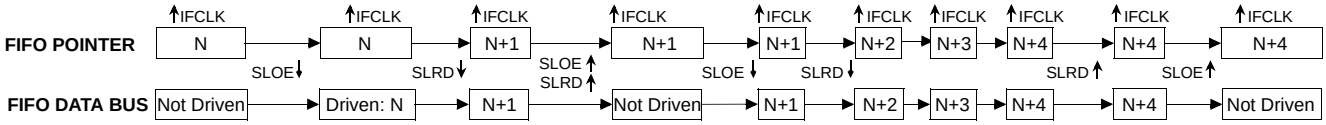


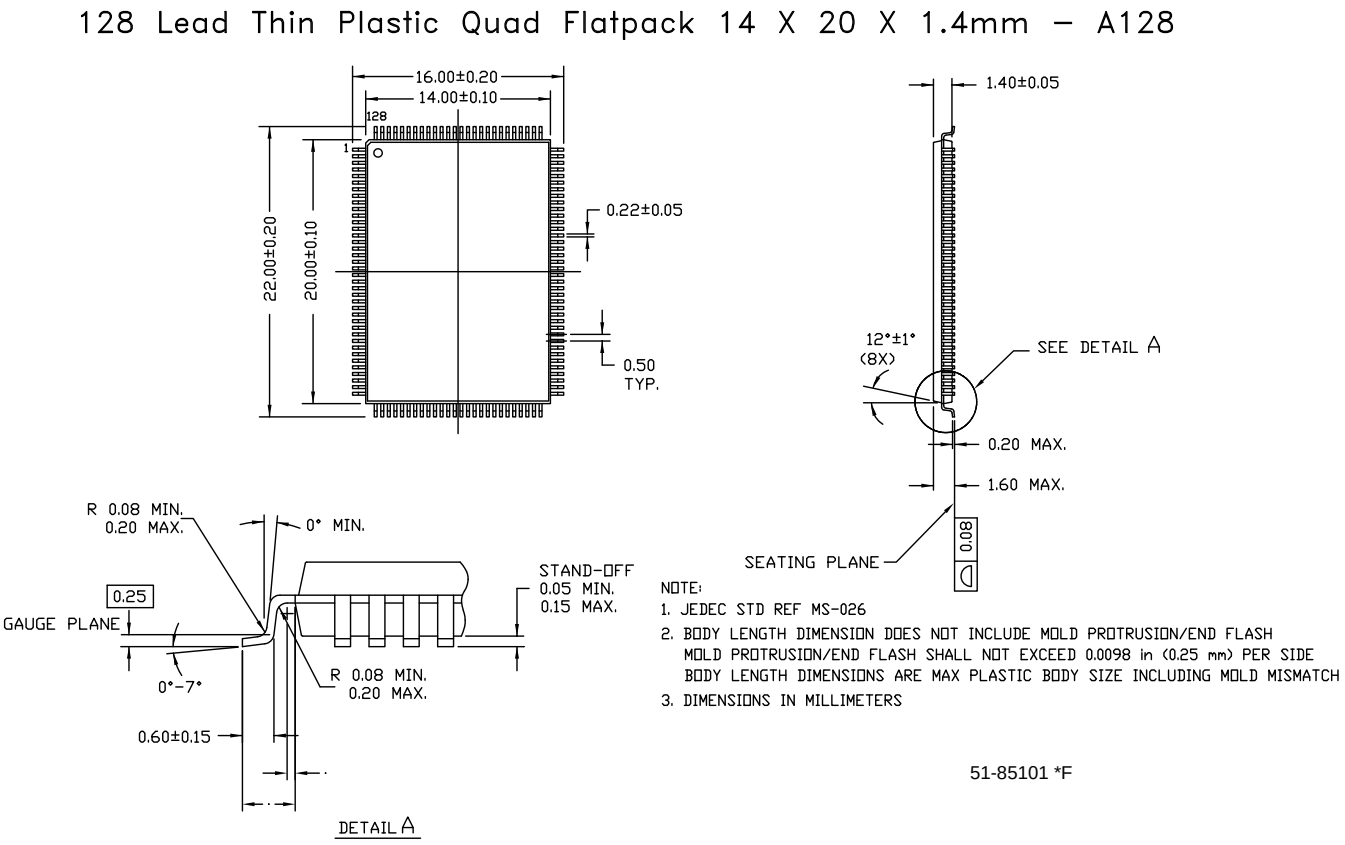
Figure 30 on page 52 shows the timing relationship of the SLAVE FIFO signals during a synchronous FIFO read using IFCLK as the synchronizing clock. The diagram illustrates a single read followed by a burst read.

- At t = 0, the FIFO address is stable and the signal SLCS is asserted (SLCS may be tied LOW in some applications). Note that t_{SFA} has a minimum of 25 ns. This means that when IFCLK is running at 48 MHz, the FIFO address setup time is more than one IFCLK cycle.
- At t = 1, SLOE is asserted. SLOE is an output enable only, whose sole function is to drive the data bus. The data that is driven on the bus is the data that the internal FIFO pointer is currently pointing to. In this example it is the first data value in the FIFO. **Note**: the data is prefetched and is driven on the bus when SLOE is asserted.
- At t = 2, SLRD is asserted. SLRD must meet the setup time of t_{SRD} (time from asserting the SLRD signal to the rising edge of the IFCLK) and maintain a minimum hold time of t_{RDH} (time from the IFCLK edge to the deassertion of the SLRD signal). If the SLCS signal is used, it must be asserted before SLRD is asserted (The SLCS and SLRD signals must both be asserted to start a valid read condition).
- The FIFO pointer is updated on the rising edge of the IFCLK, while SLRD is asserted. This starts the propagation of data from the newly addressed location to the data bus. After a propagation delay of t_{XFD} (measured from the rising edge of IFCLK) the new data value is present. N is the first data value read from the FIFO. To have data on the FIFO data bus, SLOE MUST also be asserted.

The same sequence of events are shown for a burst read and are marked with the time indicators of T = 0 through 5.

Note For the burst mode, the SLRD and SLOE are left asserted during the entire duration of the read. In the burst read mode, when SLOE is asserted, data indexed by the FIFO pointer is on the data bus. During the first read cycle, on the rising edge of the clock, the FIFO pointer is updated and incremented to point to address N+1. For each subsequent rising edge of IFCLK, while the SLRD is asserted, the FIFO pointer is incremented and the next data value is placed on the data bus.

Figure 39. 128-Pin Thin Plastic Quad Flatpack (14 × 20 × 1.4 mm) A128 (51-85101)



PCB Layout Recommendations

Follow these recommendations to ensure reliable high performance operation:[29]

- Four-layer, impedance-controlled boards are required to maintain signal quality.
- Specify impedance targets (ask your board vendor what they can achieve).
- To control impedance, maintain trace widths and trace spacing.
- Minimize stubs to minimize reflected signals.
- Connections between the USB connector shell and signal ground must be near the USB connector.
- Bypass and flyback caps on VBUS, near connector, are recommended.
- DPLUS and DMINUS trace lengths should be kept to within 2 mm of each other in length, with preferred length of 20 to 30 mm.
- Maintain a solid ground plane under the DPLUS and DMINUS traces. Do not allow the plane to split under these traces.
- Do not place vias on the DPLUS or DMINUS trace routing.
- Isolate the DPLUS and DMINUS traces from all other signal traces by no less than 10 mm.

Note
29. Source for recommendations: *EZ-USB FX2™PCB Design Recommendations*, http://www.cypress.com and *High Speed USB Platform Design Guidelines*, http://www.usb.org/developers/docs/hs_usb_pdg_r1_0.pdf.

Acronyms

Table 34. Acronyms Used in this Document

Acronym	Description
ASIC	application-specific integrated circuit
ATA	advanced technology attachment
DID	device identifier
DSL	digital service line
DSP	digital signal processor
ECC	error correction code
EEPROM	electrically erasable programmable read only memory
EPP	enhanced parallel port
FIFO	first in first out
GPIF	general programmable interface
GPIO	general purpose input output
I/O	input output
LAN	local area network
MPEG	moving picture experts group
PCMCIA	personal computer memory card international association
PID	product identifier
PLL	phase locked loop
QFN	quad flat no leads
RAM	random access memory
SIE	serial interface engine
SOF	start of frame
SSOP	super small outline package
TQFP	thin quad flat pack
USART	universal serial asynchronous receiver/transmitter
USB	universal serial bus
UTOPIA	universal test and operations physical-layer interface
VFBGA	very fine ball grid array
VID	vendor identifier

Document Conventions

Units of Measure

Table 35. Units of Measure

Symbol	Unit of Measure
kHz	kilohertz
mA	milliamperes
Mbps	megabits per second
MBPs	megabytes per second
MHz	megahertz
uA	microamperes
V	volts

Document History Page

Document Title: CY7C68013A, CY7C68014A, CY7C68015A, CY7C68016A, EZ-USB® FX2LP™ USB Microcontroller High-Speed USB Peripheral Controller Document Number: 38-08032				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	124316	VCS	03/17/03	New datasheet
*A	128461	VCS	09/02/03	Added PN CY7C68015A throughout datasheet Modified Figure 1 to add ECC block and fix errors Removed word “compatible” where associated with I^2C Corrected grammar and formatting in various locations Updated Sections 3.2.1, 3.9, 3.11, Table 9, Section 5.0 Added Sections 3.15, 3.18.4, 3.20 Modified Figure 5 for clarity Updated Figure 37 to match current spec revision
*B	130335	KKV	10/09/03	Restored PRELIMINARY to header (had been removed in error from rev. *A)
*C	131673	KKU	02/12/04	Section 8.1 changed “certified” to “compliant” Table 14 added parameter V_{IH_X} and V_{IL_X} Added Sequence diagrams Section 9.16 Updated Ordering information with lead-free parts Updated Registry Summary Section 3.12.4:example changed to column 8 from column 9 Updated Figure 14 memory write timing Diagram Updated section 3.9 (reset) Updated section 3.15 ECC Generation
*D	230713	KKU	See ECN	Changed Lead free Marketing part numbers in Table 33 as per spec change in 28-00054.
*E	242398	TMD	See ECN	Minor Change: datasheet posted to the web,
*F	271169	MON	See ECN	Added USB-IF Test ID number Added USB 2.0 logo Added values for Isusp, Icc, Power Dissipation, Vih_x, Vil_x Changed VCC from ± 10% to ± 5% Changed PKTEND to FLAGS output propagation delay (asynchronous interface) in Table 28 from a max value of 70 ns to 115 ns
*G	316313	MON	See ECN	Removed CY7C68013A-56PVXCT part availability Added parts ideal for battery powered applications: CY7C68014A, CY7C68016A Provided additional timing restrictions and requirement about the use of PKETEND pin to commit a short one byte/word packet subsequent to committing a packet automatically (when in auto mode). Added Min Vcc Ramp Up time (0 to 3.3v)
*H	338901	MON	See ECN	Added information about the AUTOPTR1/AUTOPTR2 address timing with regards to data memory read/write timing diagram. Removed TBD for Min value of Clock to FIFO Data Output Propagation Delay (t_{XFD}) for Slave FIFO Synchronous Read Changed Table 33 to include part CY7C68016A-56LFXC in the part listed for battery powered applications Added register GPCR2 in register summary
*I	371097	MON	See ECN	Added timing for strobing RD#/WR# signals when using PortC strobe feature (Section)
*J	397239	MON	See ECN	Removed XTALINSRC register from register summary. Changed Vcc margins to ±10% Added 56-pin VFBGA Pin Package Diagram Added 56-pin VFBGA definition in pin listing Added RDK part number to the Ordering Information table

Document History Page (continued)

Document Title: CY7C68013A, CY7C68014A, CY7C68015A, CY7C68016A, EZ-USB® FX2LP™ USB Microcontroller High-Speed USB Peripheral Controller Document Number: 38-08032				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*W	3998554	GAYA	07/19/2013	Added Errata footnote (Note 3). Updated Functional Overview: Updated Interrupt System: Updated FIFO/GPIF Interrupt (INT4): Added Note 3 and referred the same note in “Endpoint 2 empty flag” in Table 4. Updated Package Diagrams: spec 51-85062 – Changed revision from *E to *F. spec 001-53450 – Changed revision from *B to *C. Added Errata. Updated in new template.
*X	4617527	GAYA	01/15/2015	Updated Figure 13 Added a note to sections Data Memory Read[21] and Data Memory Write[23] sections Updated template to include the More Information section Updated Figure 37, Figure 38, Figure 39 Updated Table 11 with Reset state information for pins Sunset Review
*Y	5317277	ODC	06/28/2016	Updated CY Logo and Sales Disclaimer.