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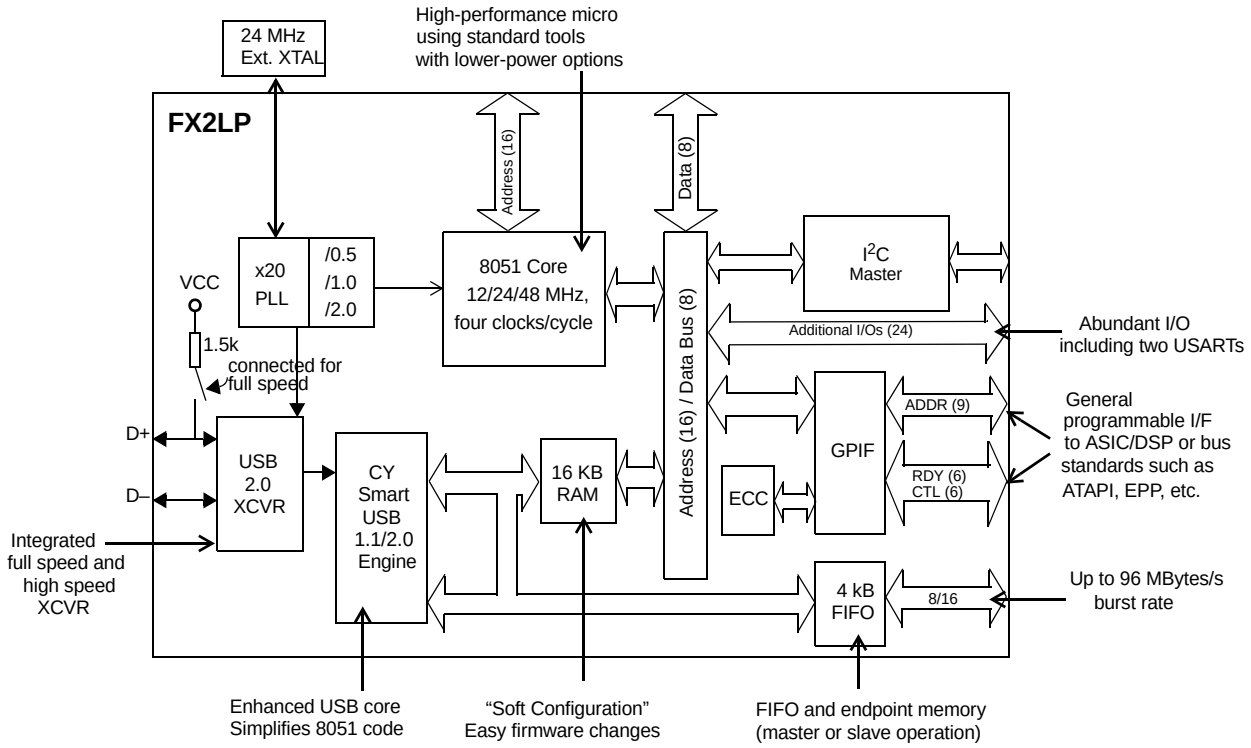
What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	USB Microcontroller
Core Processor	8051
Program Memory Type	ROMless
Controller Series	CY7C680xx
RAM Size	16K x 8
Interface	I²C, USB, USART
Number of I/O	26
Voltage - Supply	3V ~ 3.6V
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	56-VFQFN Exposed Pad
Supplier Device Package	56-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy7c68016a-56lfxct

Logic Block Diagram



Cypress's EZ-USB® FX2LP™ (CY7C68013A/14A) is a low-power version of the EZ-USB FX2™ (CY7C68013), which is a highly integrated, low-power USB 2.0 microcontroller. By integrating the USB 2.0 transceiver, serial interface engine (SIE), enhanced 8051 microcontroller, and a programmable peripheral interface in a single chip, Cypress has created a cost-effective solution that provides superior time-to-market advantages with low power to enable bus-powered applications.

The ingenious architecture of FX2LP results in data transfer rates of over 53 Mbytes per second (the maximum allowable USB 2.0 bandwidth), while still using a low-cost 8051 microcontroller in a package as small as a 56 VFBGA (5 mm x 5 mm). Because it incorporates the USB 2.0 transceiver, the FX2LP is more economical, providing a smaller-footprint solution than a USB 2.0 SIE or external transceiver implementations.

With EZ-USB FX2LP, the Cypress Smart SIE handles most of the USB 1.1 and 2.0 protocol in hardware, freeing the embedded microcontroller for application-specific functions and decreasing the development time to ensure USB compatibility.

The general programmable interface (GPIF) and Master/Slave Endpoint FIFO (8-bit or 16-bit data bus) provide an easy and glueless interface to popular interfaces such as ATA, UTOPIA, EPP, PCMCIA, and most DSP/processors.

The FX2LP draws less current than the FX2 (CY7C68013), has double the on-chip code/data RAM, and is fit, form, and function compatible with the 56-, 100-, and 128-pin FX2.

Five packages are defined for the family: 56 VFBGA, 56 SSOP, 56 QFN, 100 TQFP, and 128 TQFP.

Applications

- Portable video recorder
- MPEG/TV conversion
- DSL modems
- ATA interface
- Memory card readers
- Legacy conversion devices
- Cameras
- Scanners
- Wireless LAN
- MP3 players
- Networking

The “Reference Designs” section of the Cypress web site provides additional tools for typical USB 2.0 applications. Each reference design comes complete with firmware source and object code, schematics, and documentation. Visit www.cypress.com for more information.

Functional Overview

USB Signaling Speed

FX2LP operates at two of the three rates defined in the USB Specification Revision 2.0, dated April 27, 2000:

- Full speed, with a signaling bit rate of 12 Mbps
- High speed, with a signaling bit rate of 480 Mbps

FX2LP does not support the Low Speed signaling mode of 1.5 Mbps.

8051 Microprocessor

The 8051 microprocessor embedded in the FX2LP family has 256 bytes of register RAM, an expanded interrupt system, three timer/counters, and two USARTs.

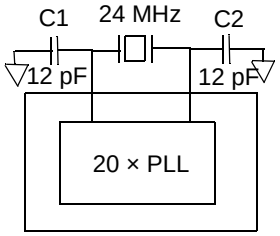
8051 Clock Frequency

FX2LP has an on-chip oscillator circuit that uses an external 24-MHz (±100 ppm) crystal with the following characteristics:

- Parallel resonant
- Fundamental mode
- 500-µW drive level
- 12-pF (5% tolerance) load capacitors

An on-chip PLL multiplies the 24-MHz oscillator up to 480 MHz, as required by the transceiver/PHY; internal counters divide it down for use as the 8051 clock. The default 8051 clock frequency is 12 MHz. The clock frequency of the 8051 can be changed by the 8051 through the CPUCS register, dynamically.

Figure 1. Crystal Configuration



12-pF capacitor values assume a trace capacitance of 3 pF per side on a four-layer FR4 PCA

The CLKOUT pin, which can be three-stated and inverted using internal control bits, outputs the 50% duty cycle 8051 clock, at the selected 8051 clock frequency: 48 MHz, 24 MHz, or 12 MHz.

USARTs

FX2LP contains two standard 8051 USARTs, addressed through Special Function Register (SFR) bits. The USART interface pins are available on separate I/O pins, and are not multiplexed with port pins.

UART0 and UART1 can operate using an internal clock at 230 KBaud with no more than 1% baud rate error. 230 KBaud operation is achieved by an internally derived clock source that generates overflow pulses at the appropriate time. The internal clock adjusts for the 8051 clock rate (48 MHz, 24 MHz, and 12 MHz) such that it always presents the correct frequency for the 230-KBaud operation.[1]

Special Function Registers

Certain 8051 SFR addresses are populated to provide fast access to critical FX2LP functions. These SFR additions are shown in Table 1 on page 6. Bold type indicates nonstandard, enhanced 8051 registers. The two SFR rows that end with “0” and “8” contain bit-addressable registers. The four I/O ports A to D use the SFR addresses used in the standard 8051 for ports 0 to 3, which are not implemented in FX2LP. Because of the faster and more efficient SFR addressing, the FX2LP I/O ports are not addressable in external RAM space (using the MOVX instruction).

I^2C Bus

FX2LP supports the I^2C bus as a master only at 100/400 kHz. SCL and SDA pins have open-drain outputs and hysteresis inputs. These signals must be pulled up to 3.3 V, even if no I^2C device is connected.

Buses

All packages, 8-bit or 16-bit “FIFO” bidirectional data bus, multiplexed on I/O ports B and D. 128-pin package: adds 16-bit output-only 8051 address bus, 8-bit bidirectional data bus.

Note
1. 115-KBaud operation is also possible by programming the 8051 SMOD0 or SMOD1 bits to a “1” for UART0, UART1, or both respectively.

Endpoint RAM

Size

- 3 × 64 bytes (Endpoints 0 and 1)
- 8 × 512 bytes (Endpoints 2, 4, 6, 8)

Organization

- EP0
- Bidirectional endpoint zero, 64-byte buffer
- EP1IN, EP1OUT
- 64 byte buffers, bulk or interrupt
- EP2, 4, 6, 8
- Eight 512-byte buffers, bulk, interrupt, or isochronous. EP4 and EP8 can be double buffered; EP2 and 6 can be either double, triple, or quad buffered. For Hi-Speed endpoint configuration options, see Figure 5.

Setup Data Buffer

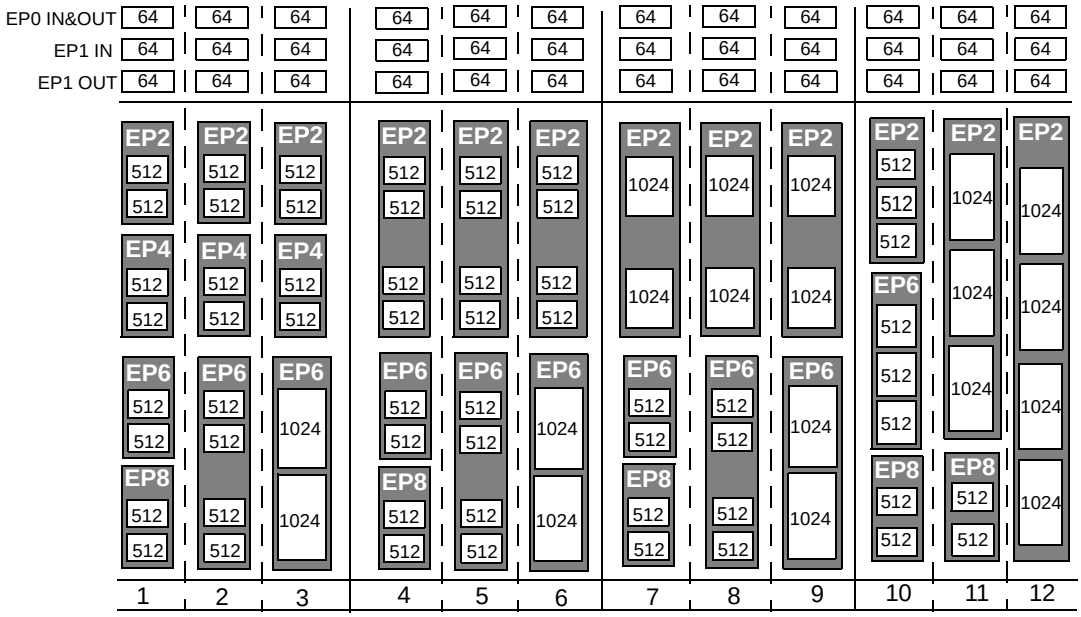
A separate 8-byte buffer at 0xE6B8-0xE6BF holds the setup data from a CONTROL transfer.

Endpoint Configurations (Hi-Speed Mode)

Endpoints 0 and 1 are the same for every configuration. Endpoint 0 is the only CONTROL endpoint, and endpoint 1 can be either BULK or INTERRUPT.

The endpoint buffers can be configured in any 1 of the 12 configurations shown in the vertical columns. When operating in the Full-Speed BULK mode, only the first 64 bytes of each buffer are used. For example, in Hi-Speed mode, the max packet size is 512 bytes, but in Full-Speed mode, it is 64 bytes. Even though a buffer is configured to a 512-byte buffer, in Full-Speed mode, only the first 64 bytes are used. The unused endpoint buffer space is not available for other operations. An example endpoint configuration is the EP2–1024 double-buffered; EP6–512 quad-buffered (column 8).

Figure 5. Endpoint Configuration



Default Full-Speed Alternate Settings

Table 6. Default Full Speed Alternate Settings[5, 6]

Alternate Setting	0	1	2	3
ep0	64	64	64	64
ep1out	0	64 bulk	64 int	64 int
ep1in	0	64 bulk	64 int	64 int
ep2	0	64 bulk out (2×)	64 int out (2×)	64 iso out (2×)
ep4	0	64 bulk out (2×)	64 bulk out (2×)	64 bulk out (2×)
ep6	0	64 bulk in (2×)	64 int in (2×)	64 iso in (2×)
ep8	0	64 bulk in (2×)	64 bulk in (2×)	64 bulk in (2×)

Default High Speed Alternate Settings

Table 7. Default Hi-Speed Alternate Settings[5, 6]

Alternate Setting	0	1	2	3
ep0	64	64	64	64
ep1out	0	512 bulk[7]	64 int	64 int
ep1in	0	512 bulk[7]	64 int	64 int
ep2	0	512 bulk out (2×)	512 int out (2×)	512 iso out (2×)
ep4	0	512 bulk out (2×)	512 bulk out (2×)	512 bulk out (2×)
ep6	0	512 bulk in (2×)	512 int in (2×)	512 iso in (2×)
ep8	0	512 bulk in (2×)	512 bulk in (2×)	512 bulk in (2×)

External FIFO Interface

Architecture

The FX2LP slave FIFO architecture has eight 512-byte blocks in the endpoint RAM that directly serve as FIFO memories and are controlled by FIFO control signals (such as IFCLK, SLCS#, SLRD, SLWR, SLOE, PKTEND, and flags).

In operation, some of the eight RAM blocks fill or empty from the SIE, while the others are connected to the I/O transfer logic. The transfer logic takes two forms: the GPIF for internally generated control signals and the slave FIFO interface for externally controlled transfers.

Master/Slave Control Signals

The FX2LP endpoint FIFOs are implemented as eight physically distinct 256×16 RAM blocks. The 8051/SIE can switch any of the RAM blocks between two domains, the USB (SIE) domain and the 8051-I/O Unit domain. This switching is done virtually instantaneously, giving essentially zero transfer time between "USB FIFOs" and "Slave FIFOs." Because they are physically the same memory, no bytes are actually transferred between buffers.

At any time, some RAM blocks are filling/emptying with the USB data under SIE control, while other RAM blocks are available to the 8051, the I/O control unit, or both. The RAM blocks operates as single-port in the USB domain, and dual-port in the 8051-I/O domain. The blocks can be configured as single-, double-, triple-, or quad-buffered as previously shown.

The I/O control unit implements either an internal master (M for Master) or external master (S for Slave) interface.

In Master (M) mode, the GPIF internally controls FIFOADR[1..0] to select a FIFO. The RDY pins (two in the 56-pin package, six in the 100-pin and 128-pin packages) can be used as flag inputs from an external FIFO or other logic if desired. The GPIF can be run from either an internally derived clock or externally supplied clock (IFCLK), at a rate that transfers data up to 96 MBytes/s (48

Notes
5. "0" means "not implemented."
6. "2×" means "double buffered."
7. Even though these buffers are 64 bytes, they are reported as 512 for USB 2.0 compliance. The user must never transfer packets larger than 64 bytes to EP1.

In the Slave (S) mode, FX2LP accepts either an internally derived clock or externally supplied clock (IFCLK, max frequency 48 MHz) and SLCS#, SLRD, SLWR, SLOE, PKTEND signals from external logic. When using an external IFCLK, the external clock must be present before switching to the external clock with the IFCLKSRC bit. Each endpoint can individually be selected for byte or word operation by an internal configuration bit and a Slave FIFO Output Enable signal (SLOE) that enables data of the selected width. External logic must ensure that the output enable signal is inactive when writing data to a slave FIFO. The slave interface can also operate asynchronously, where the SLRD and SLWR signals act directly as strobes, rather than a clock qualifier as in synchronous mode. The signals SLRD, SLWR, SLOE, and PKTEND are gated by the signal SLCS#.

GPIF and FIFO Clock Rates

An 8051 register bit selects one of two frequencies for the internally supplied interface clock: 30 MHz and 48 MHz. Alternatively, an externally supplied clock of 5 MHz–48 MHz feeding the IFCLK pin can be used as the interface clock. IFCLK can be configured to function as an output clock when the GPIF and FIFOs are internally clocked. An output enable bit in the IFCONFIG register turns this clock output off, if desired. Another bit within the IFCONFIG register inverts the IFCLK signal whether internally or externally sourced.

GPIF

The GPIF is a flexible 8-bit or 16-bit parallel interface driven by a user-programmable finite state machine. It enables the CY7C68013A/15A to perform local bus mastering and can implement a wide variety of protocols such as ATA interface, printer parallel port, and Utopia.

The GPIF has six programmable control outputs (CTL), nine address outputs (GPIFADRx), and six general-purpose ready inputs (RDY). The data bus width can be 8 or 16 bits. Each GPIF vector defines the state of the control outputs, and determines what state a ready input (or multiple inputs) must be before proceeding. The GPIF vector can be programmed to advance a FIFO to the next data value, advance an address, etc. A sequence of the GPIF vectors make up a single waveform that is executed to perform the desired data move between the FX2LP and the external device.

Six Control OUT Signals

The 100-pin and 128-pin packages bring out all six Control Output pins (CTL0-CTL5). The 8051 programs the GPIF unit to define the CTL waveforms. The 56-pin package brings out three of these signals, CTL0–CTL2. CTLx waveform edges can be programmed to make transitions as fast as once per clock (20.8 ns using a 48-MHz clock).

Six Ready IN Signals

The 100-pin and 128-pin packages bring out all six Ready inputs (RDY0–RDY5). The 8051 programs the GPIF unit to test the RDY pins for GPIF branching. The 56-pin package brings out two of these signals, RDY0–1.

Nine GPIF Address OUT Signals

Nine GPIF address lines are available in the 100-pin and 128-pin packages, GPIFADR[8..0]. The GPIF address lines enable indexing through up to a 512-byte block of RAM. If more address lines are needed, then I/O port pins are used.

Long Transfer Mode

In the master mode, the 8051 appropriately sets GPIF transaction count registers (GPIFTCB3, GPIFTCB2, GPIFTCB1, or GPIFTCB0) for unattended transfers of up to 2^{32} transactions. The GPIF automatically throttles data flow to prevent under or overflow until the full number of requested transactions complete. The GPIF decrements the value in these registers to represent the current status of the transaction.

ECC Generation[8]

The EZ-USB can calculate ECCs (Error Correcting Codes) on data that passes across its GPIF or Slave FIFO interfaces. There are two ECC configurations: Two ECCs, each calculated over 256 bytes (SmartMedia Standard); and one ECC calculated over 512 bytes.

The ECC can correct any one-bit error or detect any two-bit error.

ECC Implementation

The two ECC configurations are selected by the ECCM bit:

ECCM = 0

Two 3-byte ECCs, each calculated over a 256-byte block of data. This configuration conforms to the SmartMedia Standard.

Write any value to ECCRESET, then pass data across the GPIF or Slave FIFO interface. The ECC for the first 256 bytes of data is calculated and stored in ECC1. The ECC for the next 256 bytes is stored in ECC2. After the second ECC is calculated, the values in the ECCx registers do not change until ECCRESET is written again, even if more data is subsequently passed across the interface.

ECCM = 1

One 3-byte ECC calculated over a 512-byte block of data.

Write any value to ECCRESET then pass data across the GPIF or Slave FIFO interface. The ECC for the first 512 bytes of data is calculated and stored in ECC1; ECC2 is unused. After the ECC is calculated, the values in ECC1 do not change even if more data is subsequently passed across the interface, till ECCRESET is written again.

USB Uploads and Downloads

The core has the ability to directly edit the data contents of the internal 16-KB RAM and of the internal 512-byte scratch pad RAM via a vendor-specific command. This capability is normally used when soft downloading the user code and is available only to and from the internal RAM, only when the 8051 is held in reset. The available RAM spaces are 16 KB from 0x0000–0x3FFF (code/data) and 512 bytes from 0xE000–0xE1FF (scratch pad data RAM)[9].

Notes
8. To use the ECC logic, the GPIF or Slave FIFO interface must be configured for byte-wide operation.
9. After the data is downloaded from the host, a “loader” can execute from internal RAM to transfer downloaded data to external memory.

Autopointer Access

FX2LP provides two identical autopointers. They are similar to the internal 8051 data pointers but with an additional feature: they can optionally increment after every memory access. This capability is available to and from both internal and external RAM. Autopointers are available in external FX2LP registers under the control of a mode bit (AUTOPTRSET-UP.0). Using the external FX2LP autopointer access (at 0xE67B – 0xE67C) enables the autopointer to access all internal and external RAM to the part.

Also, autopointers can point to any FX2LP register or endpoint buffer space. When the autopointer access to external memory is enabled, locations 0xE67B and 0xE67C in XDATA and code space cannot be used.

I²C Controller

FX2LP has one I²C port that is driven by two internal controllers, the one that automatically operates at boot time to load VID/PID/DID and configuration information, and another that the 8051 uses when running to control external I²C devices. The I²C port operates in master mode only.

I²C Port Pins

The I²C pins SCL and SDA must have external 2.2-kΩ pull-up resistors even if no EEPROM is connected to the FX2LP. External EEPROM device address pins must be configured properly. See Table 8 for configuring the device address pins.

Table 8. Strap Boot EEPROM Address Lines to These Values

Bytes	Example EEPROM	A2	A1	A0
16	24LC00[10]	N/A	N/A	N/A
128	24LC01	0	0	0
256	24LC02	0	0	0
4K	24LC32	0	0	1
8K	24LC64	0	0	1
16K	24LC128	0	0	1

I²C Interface Boot Load Access

At power-on reset, the I²C interface boot loader loads the VID/PID/DID configuration bytes and up to 16 KB of program/data. The available RAM spaces are 16 KB from 0x0000–0x3FFF and 512 bytes from 0xE000–0xE1FF. The 8051 is in reset. I²C interface boot loads only occur after power-on reset.

I²C Interface General-Purpose Access

The 8051 can control peripherals connected to the I²C bus using the I2CTL and I2DAT registers. FX2LP provides I²C master control only; it is never an I²C slave.

Compatible with Previous Generation EZ-USB FX2

The EZ-USB FX2LP is form-, fit-, and with minor exceptions, functionally-compatible with its predecessor, the EZ-USB FX2.

This makes for an easy transition for designers wanting to upgrade their systems from the FX2 to the FX2LP. The pinout and package selection are identical and a vast majority of firmware previously developed for the FX2 functions in the FX2LP.

For designers migrating from the FX2 to the FX2LP, a change in the bill of material and review of the memory allocation (due to increased internal memory) is required. For more information about migrating from EZ-USB FX2 to EZ-USB FX2LP, see the application note titled *Migrating from EZ-USB FX2 to EZ-USB FX2LP* available in the Cypress web site.

Table 9. Part Number Conversion Table

EZ-USB FX2 Part Number	EZ-USB FX2LP Part Number	Package Description
CY7C68013-56PVC	CY7C68013A-56PVXC or CY7C68014A-56PVXC	56-pin SSOP
CY7C68013-56PVCT	CY7C68013A-56PVXCT or CY7C68014A-56PVXCT	56-pin SSOP – Tape and Reel
CY7C68013-56LFC	CY7C68013A-56LFXC or CY7C68014A-56LFXC	56-pin QFN
CY7C68013-100AC	CY7C68013A-100AXC or CY7C68014A-100AXC	100-pin TQFP
CY7C68013-128AC	CY7C68013A-128AXC or CY7C68014A-128AXC	128-pin TQFP

CY7C68013A/14A and CY7C68015A/16A Differences

CY7C68013A is identical to CY7C68014A in form, fit, and functionality. CY7C68015A is identical to CY7C68016A in form, fit, and functionality. CY7C68014A and CY7C68016A have a lower suspend current than CY7C68013A and CY7C68015A respectively and are ideal for power-sensitive battery applications.

CY7C68015A and CY7C68016A are available in 56-pin QFN package only. Two additional GPIO signals are available on the CY7C68015A and CY7C68016A to provide more flexibility when neither IFCLK or CLKOUT are needed in the 56-pin package.

USB developers wanting to convert their FX2 56-pin application to a bus-powered system directly benefit from these additional signals. The two GPIOs give developers the signals they need for the power-control circuitry of their bus-powered application without pushing them to a high-pincount version of FX2LP.

The CY7C68015A is only available in the 56-pin QFN package

Table 10. CY7C68013A/14A and CY7C68015A/16A Pin Differences

CY7C68013A/CY7C68014A	CY7C68015A/CY7C68016A
IFCLK	PE0
CLKOUT	PE1

Note
10. This EEPROM does not have address pins.

Figure 6. Signal

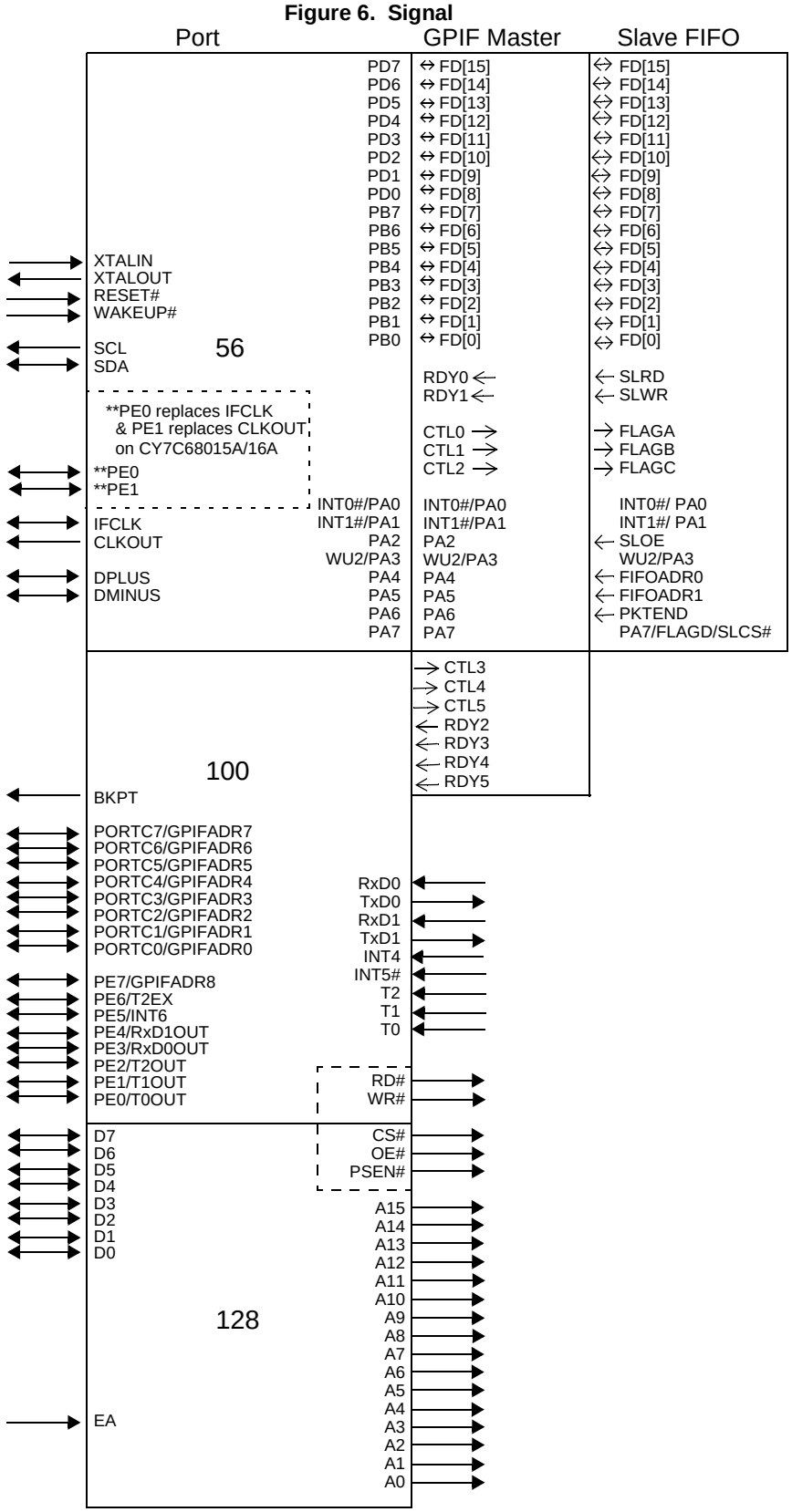
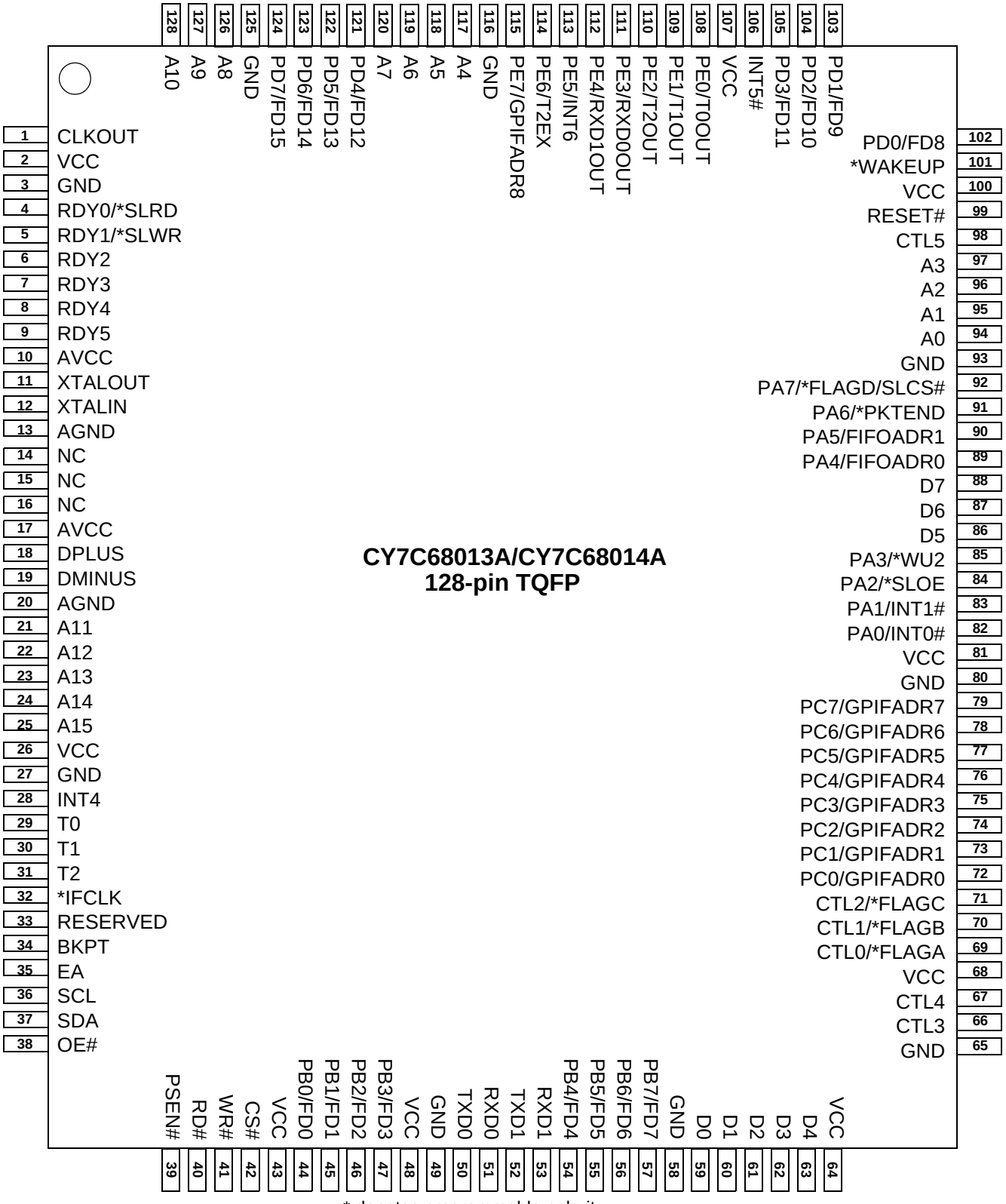


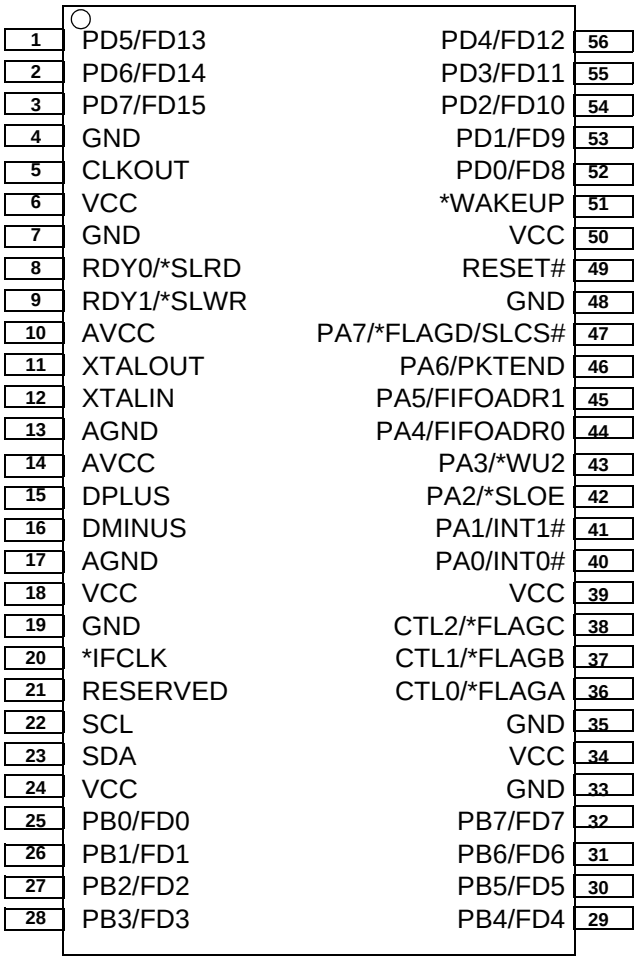
Figure 7. CY7C68013A/CY7C68014A 128-Pin TQFP Pin Assignment



* denotes programmable polarity

Figure 9. CY7C68013A/CY7C68014A 56-Pin SSOP Pin Assignment

CY7C68013A/CY7C68014A
56-pin SSOP



* denotes programmable polarity

Table 11. FX2LP Pin Descriptions[11] (continued)

128 TQFP	100 TQFP	56 SSOP	56 QFN	56 VFBGA	Name	Type	Default	Reset[12]	Description
34	28	–	–		BKPT	Output	L	L	**Breakpoint**. This pin goes active (HIGH) when the 8051 address bus matches the BPADDRH/L registers and breakpoints are enabled in the BREAKPT register (BPEN = 1). If the BPPULSE bit in the BREAKPT register is HIGH, this signal pulses HIGH for eight 12-/24-/48-MHz clocks. If the BPPULSE bit is LOW, the signal remains HIGH until the 8051 clears the BREAK bit (by writing 1 to it) in the BREAKPT register.
99	77	49	42	8B	RESET#	Input	N/A	N/A	**Active LOW Reset**. Resets the entire chip. See section "Reset and Wakeup" on page 9 for more details.
35	–	–	–	–	EA	Input	N/A	N/A	**External Access**. This pin determines where the 8051 fetches code between addresses 0x0000 and 0x3FFF. If EA = 0 the 8051 fetches this code from its internal RAM. IF EA = 1 the 8051 fetches this code from external memory.
12	11	12	5	1C	XTALIN	Input	N/A	N/A	**Crystal Input**. Connect this signal to a 24-MHz parallel-resonant, fundamental mode crystal and load capacitor to GND. It is also correct to drive XTALIN with an external 24-MHz square wave derived from another clock source. When driving from an external source, the driving signal should be a 3.3-V square wave.
11	10	11	4	2C	XTALOUT	Output	N/A	N/A	**Crystal Output**. Connect this signal to a 24-MHz parallel-resonant, fundamental mode crystal and load capacitor to GND. If an external clock is used to drive XTALIN, leave this pin open.
1	100	5	54	2B	CLKOUT on CY7C68013A and CY7C68014A ---------- PE1 on CY7C68015A and CY7C68016A	O/Z ---------- I/O/Z	12 MHz ---------- I	Clock Driven ---------- Z	**CLKOUT:** 12-, 24- or 48-MHz clock, phase-locked to the 24-MHz input clock. The 8051 defaults to 12-MHz operation. The 8051 may three-state this output by setting CPUCS.1 = 1. ---------- ------**PE1** is a bidirectional I/O port pin.
Port A									
82	67	40	33	8G	PA0 or INT0#	I/O/Z	I (PA0)	Z (PA0)	Multiplexed pin whose function is selected by PORTACFG.0 **PA0** is a bidirectional I/O port pin. **INT0#** is the active-LOW 8051 INT0 interrupt input signal, which is either edge-triggered (IT0 = 1) or level-triggered (IT0 = 0).
83	68	41	34	6G	PA1 or INT1#	I/O/Z	I (PA1)	Z (PA1)	Multiplexed pin whose function is selected by: PORTACFG.1 **PA1** is a bidirectional I/O port pin. **INT1#** is the active-LOW 8051 INT1 interrupt input signal, which is either edge-triggered (IT1 = 1) or level-triggered (IT1 = 0).

Table 11. FX2LP Pin Descriptions[11] (continued)

128 TQFP	100 TQFP	56 SSOP	56 QFN	56 VFBGA	Name	Type	Default	Reset[12]	Description
84	69	42	35	8F	PA2 or SLOE	I/O/Z	I (PA2)	Z (PA2)	Multiplexed pin whose function is selected by two bits: IFCONFIG[1:0]. **PA2** is a bidirectional I/O port pin. **SLOE** is an input-only output enable with programmable polarity (FIFOPINPOLAR.4) for the slave FIFOs connected to FD[7..0] or FD[15..0].
85	70	43	36	7F	PA3 or WU2	I/O/Z	I (PA3)	Z (PA3)	Multiplexed pin whose function is selected by: WAKEUP.7 and OEA.3 **PA3** is a bidirectional I/O port pin. **WU2** is an alternate source for **USB Wakeup,** enabled by WU2EN bit (WAKEUP.1) and polarity set by WU2POL (WAKEUP.4). If the 8051 is in suspend and WU2EN = 1, a transition on this pin starts up the oscillator and interrupts the 8051 to enable it to exit the suspend mode. Asserting this pin inhibits the chip from suspending if WU2EN = 1.
89	71	44	37	6F	PA4 or FIFOADR0	I/O/Z	I (PA4)	Z (PA4)	Multiplexed pin whose function is selected by: IFCONFIG[1..0]. **PA4** is a bidirectional I/O port pin. **FIFOADR0** is an input-only address select for the slave FIFOs connected to FD[7..0] or FD[15..0].
90	72	45	38	8C	PA5 or FIFOADR1	I/O/Z	I (PA5)	Z (PA5)	Multiplexed pin whose function is selected by: IFCONFIG[1..0]. **PA5** is a bidirectional I/O port pin. **FIFOADR1** is an input-only address select for the slave FIFOs connected to FD[7..0] or FD[15..0].
91	73	46	39	7C	PA6 or PKTEND	I/O/Z	I (PA6)	Z (PA6)	Multiplexed pin whose function is selected by the IFCONFIG[1:0] bits. **PA6** is a bidirectional I/O port pin. **PKTEND** is an input used to commit the FIFO packet data to the endpoint and whose polarity is programmable via FIFOPINPOLAR.5.
92	74	47	40	6C	PA7 or FLAGD or SLCS#	I/O/Z	I (PA7)	Z (PA7)	Multiplexed pin whose function is selected by the IFCONFIG[1:0] and PORTACFG.7 bits. **PA7** is a bidirectional I/O port pin. **FLAGD** is a programmable slave-FIFO output status flag signal. **SLCS#** gates all other slave FIFO enable/strobes
Port B									
44	34	25	18	3H	PB0 or FD[0]	I/O/Z	I (PB0)	Z (PB0)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB0** is a bidirectional I/O port pin. **FD[0]** is the bidirectional FIFO/GPIF data bus.
45	35	26	19	4F	PB1 or FD[1]	I/O/Z	I (PB1)	Z (PB1)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB1** is a bidirectional I/O port pin. **FD[1]** is the bidirectional FIFO/GPIF data bus.
46	36	27	20	4H	PB2 or FD[2]	I/O/Z	I (PB2)	Z (PB2)	Multiplexed pin whose function is selected by the following bits: IFCONFIG[1..0]. **PB2** is a bidirectional I/O port pin. **FD[2]** is the bidirectional FIFO/GPIF data bus.

Table 11. FX2LP Pin Descriptions[11] (continued)

128 TQFP	100 TQFP	56 SSOP	56 QFN	56 VFBGA	Name	Type	Default	Reset[12]	Description
PORT D									
102	80	52	45	8A	PD0 or FD[8]	I/O/Z	I (PD0)	Z (PD0)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[8]** is the bidirectional FIFO/GPIF data bus.
103	81	53	46	7A	PD1 or FD[9]	I/O/Z	I (PD1)	Z (PD1)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[9]** is the bidirectional FIFO/GPIF data bus.
104	82	54	47	6B	PD2 or FD[10]	I/O/Z	I (PD2)	Z (PD2)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[10]** is the bidirectional FIFO/GPIF data bus.
105	83	55	48	6A	PD3 or FD[11]	I/O/Z	I (PD3)	Z (PD3)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[11]** is the bidirectional FIFO/GPIF data bus.
121	95	56	49	3B	PD4 or FD[12]	I/O/Z	I (PD4)	Z (PD4)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[12]** is the bidirectional FIFO/GPIF data bus.
122	96	1	50	3A	PD5 or FD[13]	I/O/Z	I (PD5)	Z (PD5)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[13]** is the bidirectional FIFO/GPIF data bus.
123	97	2	51	3C	PD6 or FD[14]	I/O/Z	I (PD6)	Z (PD6)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[14]** is the bidirectional FIFO/GPIF data bus.
124	98	3	52	2A	PD7 or FD[15]	I/O/Z	I (PD7)	Z (PD7)	Multiplexed pin whose function is selected by the IFCONFIG[1..0] and EPxFIFOCFG.0 (wordwide) bits. **FD[15]** is the bidirectional FIFO/GPIF data bus.
Port E									
108	86	–	–	–	PE0 or T0OUT	I/O/Z	I (PE0)	Z (PE0)	Multiplexed pin whose function is selected by the PORTECFG.0 bit. **PE0** is a bidirectional I/O port pin. **T0OUT** is an active-HIGH signal from 8051 Timer-counter0. T0OUT outputs a high level for one CLKOUT clock cycle when Timer0 overflows. If Timer0 is operated in Mode 3 (two separate timer/counters), T0OUT is active when the low byte timer/counter overflows.
109	87	–	–	–	PE1 or T1OUT	I/O/Z	I (PE1)	Z (PE1)	Multiplexed pin whose function is selected by the PORTECFG.1 bit. **PE1** is a bidirectional I/O port pin. **T1OUT** is an active HIGH signal from 8051 Timer-counter1. T1OUT outputs a high level for one CLKOUT clock cycle when Timer1 overflows. If Timer1 is operated in Mode 3 (two separate timer/counters), T1OUT is active when the low byte timer/counter overflows.

Table 11. FX2LP Pin Descriptions[11] (continued)

128 TQFP	100 TQFP	56 SSOP	56 QFN	56 VFBGA	Name	Type	Default	Reset[12]	Description
100	78	50	43	5B	VCC	Power	N/A	N/A	**VCC**. Connect to the 3.3-V power source.
107	85	–	–	–	VCC	Power	N/A	N/A	**VCC**. Connect to the 3.3-V power source.
3	2	7	56	4B	GND	Ground	N/A	N/A	**Ground**
27	21	19	12	1H	GND	Ground	N/A	N/A	**Ground**
49	39	–	–	–	GND	Ground	N/A	N/A	**Ground**
58	48	33	26	7D	GND	Ground	N/A	N/A	**Ground**
65	50	35	28	8D	GND	Ground	N/A	N/A	**Ground**
80	65	–	–	–	GND	Ground	N/A	N/A	**Ground**
93	75	48	41	4C	GND	Ground	N/A	N/A	**Ground**
116	94	–	–	–	GND	Ground	N/A	N/A	**Ground**
125	99	4	53	4A	GND	Ground	N/A	N/A	**Ground**
14	13	–	–	–	NC	N/A	N/A	N/A	**No Connect**. This pin must be left open.
15	14	–	–	–	NC	N/A	N/A	N/A	**No Connect**. This pin must be left open.
16	15	–	–	–	NC	N/A	N/A	N/A	**No Connect**. This pin must be left open.

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power supplied (commercial)..... 0 °C to +70 °C

Ambient temperature with power supplied (industrial)..... –40 °C to + 105 °C

Supply voltage to ground potential .....–0.5 V to +4.0 V

DC input voltage to any input pin[17] ..... 5.25 V

DC voltage applied to outputs in high Z state ..... –0.5 V to V_{CC} + 0.5 V

Power dissipation ..... 300 mW

Static discharge voltage..... .....>2000 V

Max output current, per I/O port ..... 10 mA

Max output current, all five I/O ports (128-pin and 100-pin packages)..... 50 mA

Operating Conditions

T_A (ambient temperature under bias) Commercial ..... 0 °C to +70 °C

T_A (ambient temperature under bias) Industrial ..... –40 °C to +105 °C

Supply voltage .....+3.00 V to +3.60 V

Ground voltage ..... 0 V

F_{OSC} (oscillator or crystal frequency) ..... 24 MHz ± 100 ppm, parallel resonant

Thermal Characteristics

The following table displays the thermal characteristics of various packages:

Table 13. Thermal Characteristics

Package	Ambient Temperature (°C)	θ_{Jc} Junction to Case Thermal Resistance (°C/W)	θ_{Ja} Junction to Ambient Thermal Resistance (°C/W)
56 SSOP	70	24.4	47.7
100 TQFP	70	11.9	45.9
128 TQFP	70	15.5	43.2
56 QFN	70	10.6	25.2
56 VFBGA	70	30.9	58.6

The junction temperature θ_j, can be calculated using the following equation: $\theta_j = P*\theta_{Ja} + \theta_a$

Where,

P = Power

θ_{Ja} = Junction to ambient temperature ($\theta_{Jc} + \theta_{Ca}$)

θ_a = Ambient temperature (70 °C)

The case temperature θ_c, can be calculated using the following equation: $\theta_c = P*\theta_{Ca} + \theta_a$

where,

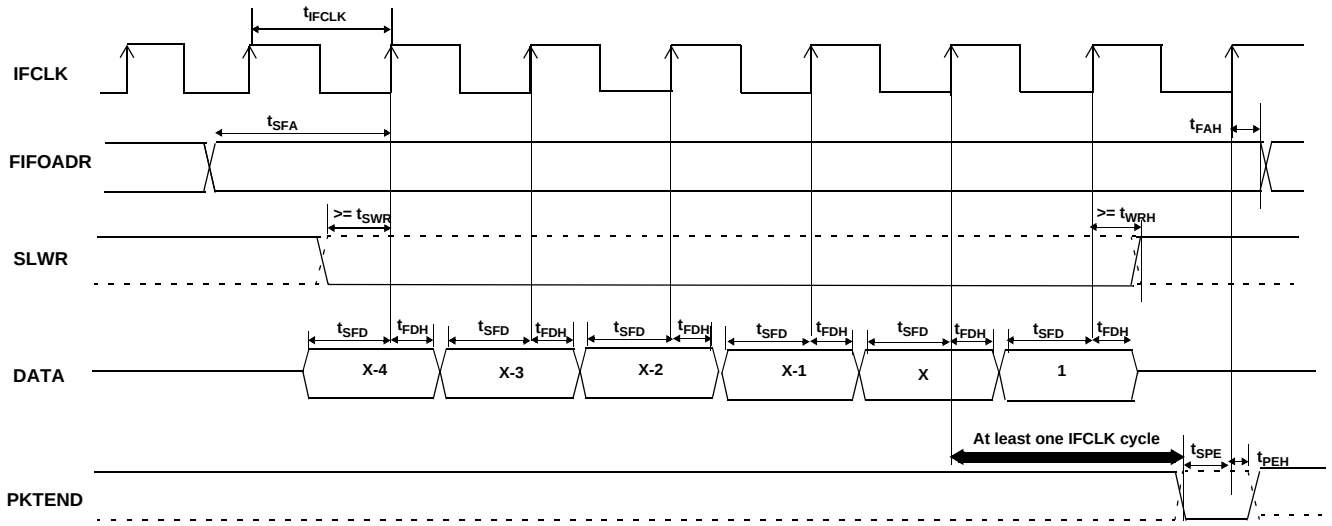
P = Power

θ_{Ca} = Case to ambient temperature

θ_a = Ambient temperature (70 °C)

Note
17. Do not power I/O with the chip power OFF.

Figure 24. Slave FIFO Synchronous Write Sequence and Timing Diagram[24]



Slave FIFO Asynchronous Packet End Strobe

Figure 25. Slave FIFO Asynchronous Packet End Strobe Timing Diagram[24]

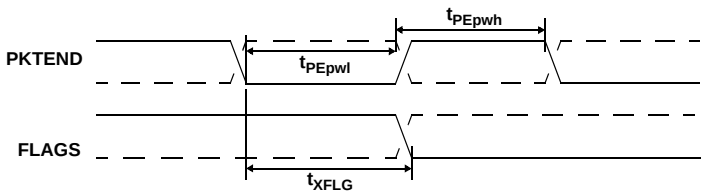


Table 28. Slave FIFO Asynchronous Packet End Strobe Parameters[27]

Parameter	Description	Min	Max	Unit
t_{PEpwl}	PKTEND pulse width LOW	50	–	ns
t_{PWpwh}	PKTEND pulse width HIGH	50	–	ns
t_{XFLG}	PKTEND to FLAGS output propagation delay	–	115	ns

Slave FIFO Output Enable

Figure 26. Slave FIFO Output Enable Timing Diagram[24]

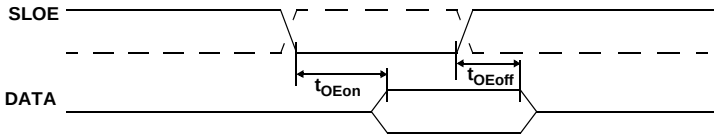


Table 29. Slave FIFO Output Enable Parameters

Parameter	Description	Min	Max	Unit
t_{OEon}	SLOE assert to FIFO DATA output		10.5	ns
t_{OEoff}	SLOE deassert to FIFO DATA hold		10.5	ns

Sequence Diagram of a Single and Burst Asynchronous Write

Figure 35. Slave FIFO Asynchronous Write Sequence and Timing Diagram[24]

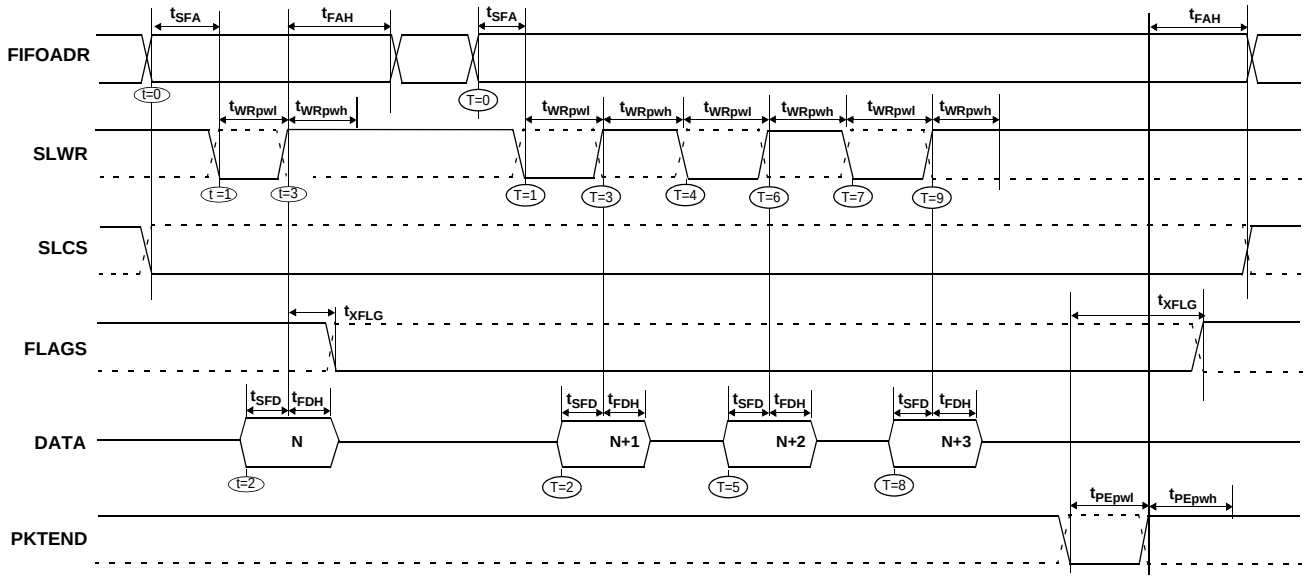


Figure 35 shows the timing relationship of the SLAVE FIFO write in an asynchronous mode. The diagram shows a single write followed by a burst write of 3 bytes and committing the 4byte short packet using PKTEND.

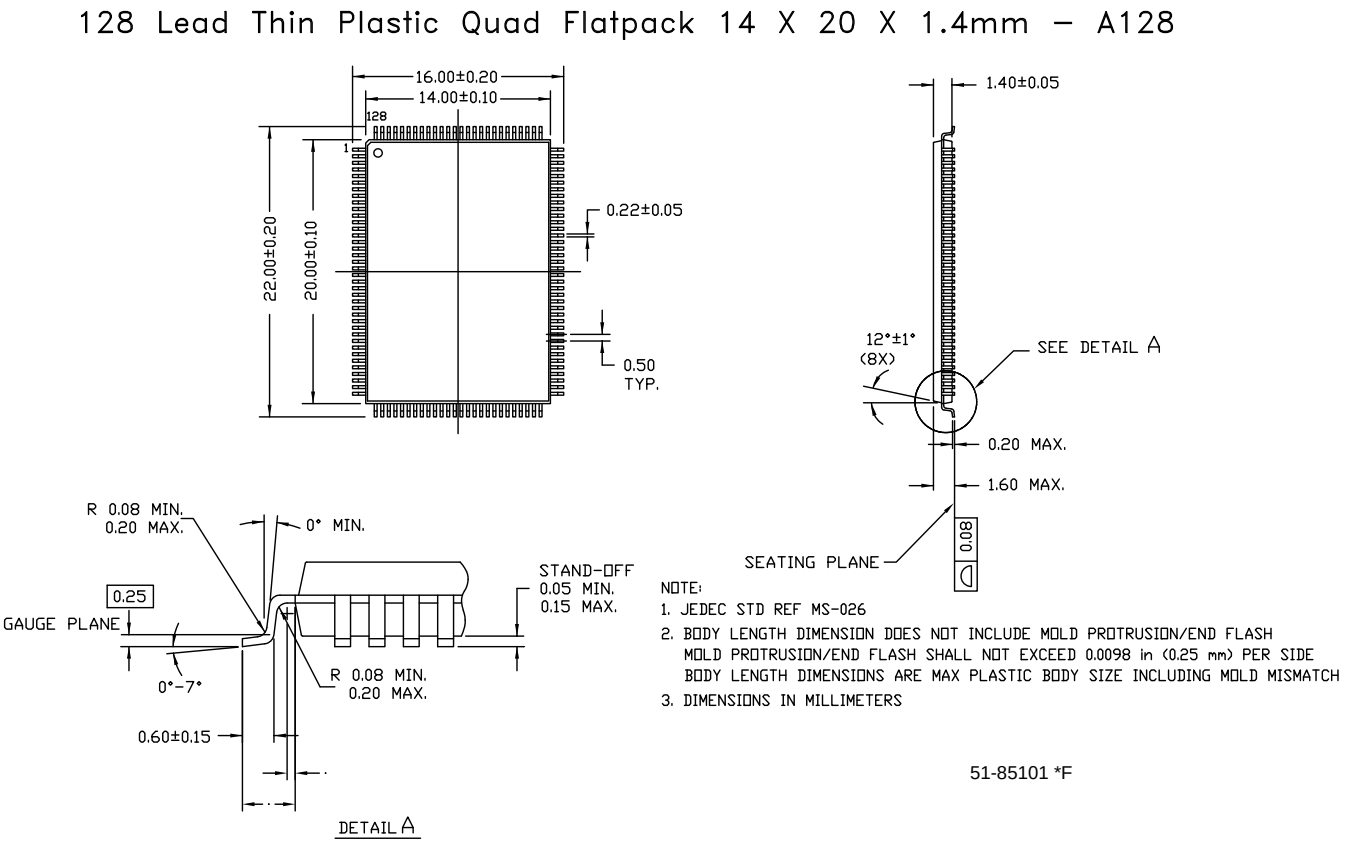
- At t = 0 the FIFO address is applied, ensuring that it meets the setup time of t_{SFA}. If SLCS is used, it must also be asserted (SLCS may be tied LOW in some applications).
- At t = 1 SLWR is asserted. SLWR must meet the minimum active pulse of t_{WRpwl} and minimum de-active pulse width of t_{WRpwh}. If the SLCS is used, it must be asserted with SLWR or before SLWR is asserted.
- At t = 2, data must be present on the bus t_{SFD} before the deasserting edge of SLWR.
- At t = 3, deasserting SLWR causes the data to be written from the data bus to the FIFO and then increments the FIFO pointer. The FIFO flag is also updated after t_{XFLG} from the deasserting edge of SLWR.

The same sequence of events is shown for a burst write and is indicated by the timing marks of T = 0 through 5.

Note In the burst write mode, after SLWR is deasserted, the data is written to the FIFO and then the FIFO pointer is incremented to the next byte in the FIFO. The FIFO pointer is post incremented.

In Figure 35, after the four bytes are written to the FIFO and SLWR is deasserted, the short 4-byte packet can be committed to the host using PKTEND. The external device should be designed to not assert SLWR and the PKTEND signal at the same time. It should be designed to assert the PKTEND after SLWR is deasserted and met the minimum deasserted pulse width. The FIFOADDR lines have to held constant during the PKTEND assertion.

Figure 39. 128-Pin Thin Plastic Quad Flatpack (14 × 20 × 1.4 mm) A128 (51-85101)



Document History Page

Document Title: CY7C68013A, CY7C68014A, CY7C68015A, CY7C68016A, EZ-USB® FX2LP™ USB Microcontroller High-Speed USB Peripheral Controller Document Number: 38-08032				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	124316	VCS	03/17/03	New datasheet
*A	128461	VCS	09/02/03	Added PN CY7C68015A throughout datasheet Modified Figure 1 to add ECC block and fix errors Removed word “compatible” where associated with I^2C Corrected grammar and formatting in various locations Updated Sections 3.2.1, 3.9, 3.11, Table 9, Section 5.0 Added Sections 3.15, 3.18.4, 3.20 Modified Figure 5 for clarity Updated Figure 37 to match current spec revision
*B	130335	KKV	10/09/03	Restored PRELIMINARY to header (had been removed in error from rev. *A)
*C	131673	KKU	02/12/04	Section 8.1 changed “certified” to “compliant” Table 14 added parameter V_{IH_X} and V_{IL_X} Added Sequence diagrams Section 9.16 Updated Ordering information with lead-free parts Updated Registry Summary Section 3.12.4:example changed to column 8 from column 9 Updated Figure 14 memory write timing Diagram Updated section 3.9 (reset) Updated section 3.15 ECC Generation
*D	230713	KKU	See ECN	Changed Lead free Marketing part numbers in Table 33 as per spec change in 28-00054.
*E	242398	TMD	See ECN	Minor Change: datasheet posted to the web,
*F	271169	MON	See ECN	Added USB-IF Test ID number Added USB 2.0 logo Added values for Isusp, Icc, Power Dissipation, Vih_x, Vil_x Changed VCC from ± 10% to ± 5% Changed PKTEND to FLAGS output propagation delay (asynchronous interface) in Table 28 from a max value of 70 ns to 115 ns
*G	316313	MON	See ECN	Removed CY7C68013A-56PVXCT part availability Added parts ideal for battery powered applications: CY7C68014A, CY7C68016A Provided additional timing restrictions and requirement about the use of PKETEND pin to commit a short one byte/word packet subsequent to committing a packet automatically (when in auto mode). Added Min Vcc Ramp Up time (0 to 3.3v)
*H	338901	MON	See ECN	Added information about the AUTOPTR1/AUTOPTR2 address timing with regards to data memory read/write timing diagram. Removed TBD for Min value of Clock to FIFO Data Output Propagation Delay (t_{XFD}) for Slave FIFO Synchronous Read Changed Table 33 to include part CY7C68016A-56LFXC in the part listed for battery powered applications Added register GPCR2 in register summary
*I	371097	MON	See ECN	Added timing for strobing RD#/WR# signals when using PortC strobe feature (Section)
*J	397239	MON	See ECN	Removed XTALINSRC register from register summary. Changed Vcc margins to ±10% Added 56-pin VFBGA Pin Package Diagram Added 56-pin VFBGA definition in pin listing Added RDK part number to the Ordering Information table

Document History Page (continued)

Document Title: CY7C68013A, CY7C68014A, CY7C68015A, CY7C68016A, EZ-USB® FX2LP™ USB Microcontroller High-Speed USB Peripheral Controller Document Number: 38-08032				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*W	3998554	GAYA	07/19/2013	Added Errata footnote (Note 3). Updated Functional Overview: Updated Interrupt System: Updated FIFO/GPIF Interrupt (INT4): Added Note 3 and referred the same note in “Endpoint 2 empty flag” in Table 4. Updated Package Diagrams: spec 51-85062 – Changed revision from *E to *F. spec 001-53450 – Changed revision from *B to *C. Added Errata. Updated in new template.
*X	4617527	GAYA	01/15/2015	Updated Figure 13 Added a note to sections Data Memory Read[21] and Data Memory Write[23] sections Updated template to include the More Information section Updated Figure 37, Figure 38, Figure 39 Updated Table 11 with Reset state information for pins Sunset Review
*Y	5317277	ODC	06/28/2016	Updated CY Logo and Sales Disclaimer.

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