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### Understanding [Embedded - Microprocessors](#)

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

### Applications of [Embedded - Microprocessors](#)

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

#### Details

Product Status	Obsolete
Core Processor	MIPS-II
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	133MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (17x17)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79rc32v334-133bbi">https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79rc32v334-133bbi</a>

- ◆ 2KB of 2-way set associative data cache, capable of write-back and write-through operation.
- ◆ Cache locking per line to speed real-time systems and critical system functions
- ◆ On-chip TLB to enable multi-tasking in modern operating systems
- ◆ EJTAG interface to enable sophisticated low-cost in-circuit emulation.

## Synchronous-DRAM Interface

The RC32334 integrates a SDRAM controller which provides direct control of system SyncDRAM running at speeds to 75MHz.

Key capabilities of the SDRAM controller include:

- ◆ Direct control of 4 banks of SDRAM (up to 2 64-bit wide DIMMs)
- ◆ On-chip page comparators optimize access latency.
- ◆ Speeds to 75MHz
- ◆ Programmable address map.
- ◆ Supports 16, 64, 128, 256, or 512Mb SDRAM devices
- ◆ Automatic refresh generation driven by on-chip timer
- ◆ Support for discrete devices, SODIMM, or DIMM modules.

Thus, systems can take advantage of the full range of commodity memory that is available, enabling system optimization for cost, real-estate, or other attributes.

## Local Memory and I/O Controller

The local memory and I/O controller implements direct control of external memory devices, including the boot ROM as well as other memory areas, and also implements direct control of external peripherals.

The local memory controller is highly flexible, allowing a wide range of devices to be directly controlled by the RC32334 processor. For example, a system can be built using an 8-bit boot ROM, 16-bit FLASH cards (possibly on PCMCIA), a 32-bit SRAM or dual-port memory, and a variety of low-cost peripherals.

Key capabilities include:

- ◆ Direct control of EPROM, FLASH, RAM, and dual-port memories
- ◆ 6 chip-select outputs, supporting up to 64MB per memory space
- ◆ Supports mixture of 8-, 16-, and 32-bit wide memory regions
- ◆ Flexible timing protocols allow direct control of a wide variety of devices
- ◆ Programmable address map for 2 chip selects
- ◆ Automatic wait state generation.

## PCI Bus Bridge

In order to leverage the wide availability of low-cost peripherals for the PC market as well as to simplify the design of add-in functions, the RC32334 integrates a full 32-bit PCI bus bridge. Key attributes of this bridge include:

- ◆ 66 MHz operation
- ◆ PCI revision 2.2 compliant
- ◆ Programmable address mappings between CPU/Local memory and PCI memory and I/O
- ◆ On-chip PCI arbiter
- ◆ Extensive buffering allows PCI to operate concurrently with local memory transfers
- ◆ Selectable byte-ordering swapper
- ◆ 5V tolerant I/O.

## On-Chip DMA Controller

To minimize CPU exception handling and maximize the efficiency of system bandwidth, the RC32334 integrates a very sophisticated 4-channel DMA controller on chip.

The RC32334 DMA controller is capable of:

- ◆ Chaining and scatter/gather support through the use of a flexible, linked list of DMA transaction descriptors
- ◆ Capable of memory<->memory, memory<->I/O, and PCI<->memory DMA
- ◆ Unaligned transfer support
- ◆ Byte, halfword, word, quadword DMA support.

## On-Chip Peripherals

The RC32334 also integrates peripherals that are common to a wide variety of embedded systems.

- ◆ Dual channel 16550 compatible UARTs, with modem control interface on one channel.
- ◆ SPI master mode interface for direct interface to EEPROM, A/D, etc.
- ◆ Interrupt Controller to speed interrupt decode and management
- ◆ Four 32-bit on-chip Timer/Counters
- ◆ Programmable I/O module

## Debug Support

To facilitate rapid time to market, the RC32334 provides extensive support for system debug.

First and foremost, this product integrates an EJTAG in-circuit emulation module, allowing a low-cost emulator to interoperate with programs executing on the controller. By using an augmented JTAG interface, the RC32334 is able to reuse the same low-cost emulators developed around the RC32364 CPU.

Secondly, the RC32334 implements additional reporting signals intended to simplify the task of system debugging when using a logic analyzer. This product allows the logic analyzer to differentiate transactions initiated by DMA from those initiated by the CPU and further allows CPU transactions to be sorted into instruction fetches vs. data fetches.

Finally, the RC32334 implements a full boundary scan capability, allowing board manufacturing diagnostics and debug.

## Packaging

The RC32334 is packaged using a 256-lead PBGA package, with 1.0mm ball spacing.

## Thermal Considerations

The RC32334 consumes less than 2.1 W peak power. The device is guaranteed in an ambient temperature range of 0° to +70° C for commercial temperature devices; -40° to +85° for industrial temperature devices.

## Revision History

**May 16, 2000:** Initial version.

**June 8, 2000:** In CPU Core Specific Signals section of Table 1, changed `cpu_dr_r_n` pin from Input to Output. Updated document from Advance to Preliminary Information.

**June 15, 2000:** In Table 1, switched assertion and de-assertion for `debug_cpu_dma_n` signal. In the AC Timing Characteristics table, added SPI section and adjusted parameters in the Reset section.

**July 12, 2000:** Removed "Preliminary Information" statement. Added information regarding external pull-ups and pull-downs to the Pin Description Table. Made minor revisions in other parts of the data sheet.

**August 3, 2000:** Added Pin Layout diagram showing power and ground pins. Revised Power Curves section to reflect support of only 2x, 3x, and 4x.

**August 30, 2000:** Added Standby mode and values to Power Consumption table. Extended Power Curve figure to 75 MHz.

**September 25, 2000:** Changed MIPS32 ISA to Enhanced MIPS-II. In Local System Interface section of Table 6, changed `Thld2` values for `mem_data[31:0]` from 1.8 to 1.5 ns and changed `Tdoh3` values for `mem_addr[25:2]`, etc. from 1.8 to 1.5 ns.

**December 12, 2000:** Changed Max values for `cpu_masterclock` period in Table 5 and added footnote. In Table 1, added 2nd alternate function for `spi_mosi`, `spi_miso`, `spi_sck`. In Table 10, removed the "1" from Alt column for `cpu_masterclk` and added "2" in Alt column for pins G3, G4, H2. In RC32334 Alternate Signal Functions table: added pin T2; added pin names in Alt #2 column for pins G3, G4, H2; added `PIO[11]` to Alt #2 column for pin R3.

**January 4, 2001:** In Table 6 under Interrupt Handling, moved the values for `Tsu9` from the Max to the Min columns.

**March 13, 2001:** Changed upper ambient temperature for industrial and commercial uses from +70° C to +85° C.

**June 7, 2001:** In the Clock Parameters table, added footnote 3 to `output_clk` category and added NA to Min and Max columns. In Figure 3 (Reset Specification), enhanced signal line for `cpu_masterclk`. In Local System Interface section of AC Timing Characteristics table, changed values in Min column for last category of signals (`Tdoh3`) from 1.5 to 2.5 for all speeds. In SDRAM Controller section of same table, changed values in Min column for last category of signals (9 signals) from 1 to 2.5 for all speeds.

**September 14, 2001:** In the Reset category of Table 6: switched `mem_addr[19:17]` from `Tsu22` and `Thld22` to `Tsu10` and `Thld10`; switched `mem_addr[22:20]` from `Tsu10` and `Thld10` to `Tsu22` and `Thld22`; moved `eitag_pcst[2:0]` from Reset to Debug Interface category under `Tsu20` and `Thld20`.

**November 1, 2001:** Added Input Voltage Undershoot parameter and 2 footnotes to Table 10.

**March 20, 2002:** In Local System Interface section of AC Timing Characteristics table, changed values in Min column for last category of signals (`Tdoh3`) from 2.5 to 1.5 for all speeds. In Table 8, PCI Drive Output Pads, the Conditions for parameters  $V_{OL}$ ,  $V_{OH}$ ,  $V_{IL}$ , and  $V_{IH}$  were changed to read Per PCI 2.2.

**May 2, 2002:** Changed upper ambient temperature for commercial uses back from +85° C to +70° C (changed erroneously from 70 to 85 on March 13, 2001). Added Reset State Status column to Table 1. Revised description of `jtag_trst_n` in Table 1 and changed this pin to a pull-down instead of a pull-up.

**July 3, 2002:** This data sheet now describes revision Y silicon and is no longer applicable to revision Z.

**July 12, 2002:** In Table 6: PCI section, changed `Thld` Min values from 1 to zero; DMA section, changed `Thld9` Min values from 2 to 1; in PIO section, changed `Thld9` Min values from 2 to 1; in Timer section, changed `Thld10` Min values from 2 to 1. Revision Y data sheet changed from Preliminary to Final.

**September 18, 2002:** Added `cpu_coldreset_n` rise time to Table 5, Clock Parameters. Added `mem_addr[16]` and `sdram_addr[16]` to Tables 1 and 12. Changed Logic Diagram to include `sdram_addr[16]`.

**December 18, 2002:** In the Reset section of Table 6, AC Timing Characteristics, setup and hold time categories for `cpu_coldreset_n` have been deleted.

**July 30, 2003:** In Table 8, added 3 new categories (Input Pads, PCI Input Pads, and All Pads) and added footnotes 2 and 3.

**March 24, 2004:** In Table 1, changed description in Satellite Mode for `pci_rst_n`. Specified "cold" reset on pages 11 and 12. Changed the maximum value for  $V_{cc}$  to 4.0 in Table 10, Absolute Maximum Ratings, and changed footnote 1 to that table. Added Power Ramp-up section on page 21.

**August 31, 2004:** Added "Green" orderable parts on page 30.

## Pin Description Table

The following table lists the pins provided on the RC32334. Note that those pin names followed by "\_n" are active-low signals. All external pull-ups and pull-downs require 10 k $\Omega$  resistor.

Name	Type	Reset State Status	Drive Strength Capability	Description																									
<b>Local System Interface</b>																													
mem_data[31:0]	I/O	Z	High	<b>Local System Data Bus</b> Primary data bus for memory. I/O and SDRAM.																									
mem_addr[25:2]	I/O	[25:10] Z [9:2] L	[25:17] Low [16:2] High	<b>Memory Address Bus</b> These signals provide the Memory or DRAM address, during a Memory or DRAM bus transaction. During each word data, the address increments either in linear or sub-block ordering, depending on the transaction type. The table below indicates how the memory write enable signals are used to address discreet memory port width types. <table border="1"> <thead> <tr> <th>Port Width</th><th>Pin Signals mem_we_n[3]</th><th>mem_we_n[2]</th><th>mem_we_n[1]</th><th>mem_we_n[0]</th></tr> </thead> <tbody> <tr> <td>DMA (32-bit)</td><td>mem_we_n[3]</td><td>mem_we_n[2]</td><td>mem_we_n[1]</td><td>mem_we_n[0]</td></tr> <tr> <td>32-bit</td><td>mem_we_n[3]</td><td>mem_we_n[2]</td><td>mem_we_n[1]</td><td>mem_we_n[0]</td></tr> <tr> <td>16-bit</td><td>Byte High Write Enable</td><td>mem_addr[1]</td><td>Not Used (Driven Low)</td><td>Byte Low Write Enable</td></tr> <tr> <td>8-bit</td><td>Not Used (Driven High)</td><td>mem_addr[1]</td><td>mem_addr[0]</td><td>Byte Write Enable</td></tr> </tbody> </table> mem_addr[22] Alternate function: reset_boot_mode[1]. mem_addr[21] Alternate function: reset_boot_mode[0]. mem_addr[20] Alternate function: reset_pci_host_mode. mem_addr[19] Alternate function: modebit [9]. mem_addr[18] Alternate function: modebit [8]. mem_addr[17] Alternate function: modebit [7]. mem_addr[16] Alternate function: sdram_addr[16]. mem_addr[15] Alternate function: sdram_addr[15]. mem_addr[14] Alternate function: sdram_addr[14]. mem_addr[13] Alternate function: sdram_addr[13]. mem_addr[11] Alternate function: sdram_addr[11]. mem_addr[10] Alternate function: sdram_addr[10]. mem_addr[9] Alternate function: sdram_addr[9]. mem_addr[8] Alternate function: sdram_addr[8]. mem_addr[7] Alternate function: sdram_addr[7]. mem_addr[6] Alternate function: sdram_addr[6]. mem_addr[5] Alternate function: sdram_addr[5]. mem_addr[4] Alternate function: sdram_addr[4]. mem_addr[3] Alternate function: sdram_addr[3]. mem_addr[2] Alternate function: sdram_addr[2].	Port Width	Pin Signals mem_we_n[3]	mem_we_n[2]	mem_we_n[1]	mem_we_n[0]	DMA (32-bit)	mem_we_n[3]	mem_we_n[2]	mem_we_n[1]	mem_we_n[0]	32-bit	mem_we_n[3]	mem_we_n[2]	mem_we_n[1]	mem_we_n[0]	16-bit	Byte High Write Enable	mem_addr[1]	Not Used (Driven Low)	Byte Low Write Enable	8-bit	Not Used (Driven High)	mem_addr[1]	mem_addr[0]	Byte Write Enable
Port Width	Pin Signals mem_we_n[3]	mem_we_n[2]	mem_we_n[1]	mem_we_n[0]																									
DMA (32-bit)	mem_we_n[3]	mem_we_n[2]	mem_we_n[1]	mem_we_n[0]																									
32-bit	mem_we_n[3]	mem_we_n[2]	mem_we_n[1]	mem_we_n[0]																									
16-bit	Byte High Write Enable	mem_addr[1]	Not Used (Driven Low)	Byte Low Write Enable																									
8-bit	Not Used (Driven High)	mem_addr[1]	mem_addr[0]	Byte Write Enable																									
mem_cs_n[5:0]	Output	H	Low with internal pull-up	<b>Memory Chip Select Negated</b> Recommend external pull-up. Signals that a Memory Bank is actively selected.																									
mem_oe_n	Output	H	High	<b>Memory Output Enable Negated</b> Recommend external pull-up. Signals that a Memory Bank can output its data lines onto the cpu_ad bus.																									

Table 1 Pin Description (Part 1 of 7)

Name	Type	Reset State Status	Drive Strength Capability	Description
pci_rst_n	Input	L	—	<b>PCI Reset Negated</b> Host mode: Resets all PCI related logic. Satellite mode: Resets all PCI related logic and also warm resets the 32334.
pci_devsel_n	I/O	Z	PCI	<b>PCI Device Select Negated</b> Driven by the target to indicate that the target has decoded the present address as a target address.
pci_req_n[2]	Input	Z	—	<b>PCI Bus Request #2 Negated</b> Requires external pull-up. Host mode: pci_req_n[2] is an input indicating a request from an external device. Satellite mode: used as pci_idsel pin which selects this device during a configuration read or write. Alternate function: pci_idsel (satellite).
pci_req_n[1]	Input	Z	—	<b>PCI Bus Request #1 Negated</b> Requires external pull-up. Host mode: pci_req_n[1] is an input indicating a request from an external device. Alternate function: Unused (satellite).
pci_req_n[0]	I/O	Z	High	<b>PCI Bus Request #0 Negated</b> Requires external pull-up for burst mode. Host mode: pci_req_n[0] is an input indicating a request from an external device. Satellite mode: pci_req_n[0] is an output indicating a request from this device.
pci_gnt_n[2]	Output	Z <sup>1</sup>	High	<b>PCI Bus Grant #2 Negated</b> Recommend external pull-up. Host mode: pci_gnt_n[2] is an output indicating a grant to an external device. Satellite mode: pci_gnt_n[2] is used as the pci_inta_n output pin. Alternate function: pci_inta_n (satellite).
pci_gnt_n[1] / pci_eeeprom_cs	I/O	X for 1 pci clock then H <sup>2</sup>	High	<b>PCI Bus Grant #1 Negated</b> Recommend external pull-up. Host mode: pci_gnt_n[1] is an output indicating a grant to an external device. Satellite mode: Used as pci_eprom_cs output pin for Serial Chip Select for loading PCI Configuration Registers in the RC32334 Reset Initialization Vector PCI boot mode. Defaults to the output direction at reset time. 1st Alternate function: pci_eeeprom_cs (satellite). 2nd Alternate function: PIO[11].
pci_gnt_n[0]	I/O	Z	High	<b>PCI Bus Grant #0 Negated</b> Host mode: pci_gnt_n[0] is an output indicating a grant to an external device. Recommend external pull-up. Satellite mode: pci_gnt_n[0] is an input indicating a grant to this device. Require external pull-up.
pci_inta_n	Output Open- collector	Z	PCI	<b>PCI Interrupt #A Negated</b> Uses pci_gnt_n[2]. See the PCI subsection.
pci_lock_n	Input		—	<b>PCI Lock Negated</b> Driven by the Bus Master to indicate that an exclusive operation is occurring.

<sup>1</sup> Z in host mode; L in satellite non-boot mode; Z in satellite boot mode.  
<sup>2</sup> H in host mode; L in satellite non-boot and boot modes. X = unknown.

**SDRAM Control Interface**

sdram_addr_12	Output	L	High	<b>SDRAM Address Bit 12 and Precharge All</b> SDRAM mode: Provides SDRAM address bit 12 (10 on the SDRAM chip) during row address and "pre-charge all" signal during refresh, read and write command.
sdram_ras_n	Output	H	High	<b>SDRAM RAS Negated</b> SDRAM mode: Provides SDRAM RAS control signal to all SDRAM banks.

Table 1 Pin Description (Part 3 of 7)

Name	Type	Reset State Status	Drive Strength Capability	Description
uart_tx[1:0]	I/O	Z	Low	<b>UART Transmit Data Bus</b> UART mode: Each UART channel sends data on their respective output pin. Note that these pins default to inputs at reset time and must be programmed via the PIO interface before being used as UART outputs. uart_tx[0] Alternate function: PIO[5]. uart_tx[1] Alternate function: PIO[3].
uart_cts_n[0] uart_dsr_n[0] uart_dtr_n[0] uart_rts_n[0]	I/O	Z	Low	<b>UART Transmit Data Bus</b> UART mode: Data bus modem control signal pins for UART channel 0. uart_cts_n[0] Alternate function: PIO[15]. uart_dsr_n[0] Alternate function: PIO[14]. uart_dtr_n[0] Alternate function: PIO[13]. uart_rts_n[0] Alternate function: PIO[12].
spi_mosi	I/O	L	Low	<b>SPI Data Output</b> Serial mode: Output pin from RC32334 as an Input to a Serial Chip for the Serial data input stream. In PCI satellite mode, acts as an Output pin from RC32334 that connects as an Input to a Serial Chip for the Serial data input stream for loading PCI Configuration Registers in the RC32334 Reset Initialization Vector PCI boot mode. 1st Alternate function: PIO[10]. Defaults to the output direction at reset time. 2nd Alternate function: pci_eeprom_mdo.
spi_miso	I/O	Z	Low	<b>SPI Data Input</b> Serial mode: Input pin to RC32334 from the Output of a Serial Chip for the Serial data output stream. In PCI satellite mode, acts as an Input pin from RC32334 that connects as an output to a Serial Chip for the Serial data output stream for loading PCI Configuration Registers in the RC32334 Reset Initialization Vector PCI boot mode. Defaults to input direction at reset time. 1st Alternate function: PIO[7]. 2nd Alternate function: pci_eeprom_mdi.
spi_sck	I/O	L	Low	<b>SPI Clock</b> Serial mode: Output pin for Serial Clock. In PCI satellite mode, acts as an Output pin for Serial Clock for loading PCI Configuration Registers in the RC32334 Reset Initialization Vector PCI boot mode. 1st Alternate function: PIO[9]. Defaults to the output direction at reset time. 2nd Alternate function: pci_eeprom_sk.
spi_ss_n	I/O	H	Low	<b>SPI Chip Select</b> Output pin selecting the serial protocol device as opposed to the PCI satellite mode EEPROM device. Alternate function: PIO[8]. Defaults to the output direction at reset time.

**CPU Core Specific Signals**

cpu_nmi_n	Input		—	<b>CPU Non-Maskable Interrupt</b> Requires external pull-up. This interrupt input is active low to the CPU.
cpu_masterclk	Input		—	<b>CPU Master System Clock</b> Provides the basic system clock.
cpu_int_n[5:4], [2:0]	Input		—	<b>CPU Interrupt</b> Requires external pull-up. These interrupt inputs are active low to the CPU.
cpu_coldreset_n	Input	L	—	<b>CPU Cold Reset</b> This active-low signal is asserted to the RC32334 after $V_{cc}$ becomes valid on the initial power-up. The Reset initialization vectors for the RC32334 are latched by cold reset.

Table 1 Pin Description (Part 5 of 7)

Name	Type	Reset State Status	Drive Strength Capability	Description
cpu_dt_r_n	Output	Z	—	<b>CPU Direction Transmit/Receive</b> This active-low signal controls the DT/R pin of an optional FCT245 transceiver bank. It is asserted during read operations. 1st Alternate function: mem_245_dt_r_n. 2nd Alternate function: sdram_245_dt_r_n.

**JTAG Interface Signals**

jtag_tck	Input		—	<b>JTAG Test Clock</b> Requires external pull-down. An input test clock used to shift into or out of the Boundary-Scan register cells. jtag_tck is independent of the system and the processor clock with nominal 50% duty cycle.
jtag_tdi, ejtag_dint_n	Input		—	<b>JTAG Test Data In</b> Requires an external pull-up on the board. On the rising edge of jtag_tck, serial input data are shifted into either the Instruction or Data register, depending on the TAP controller state. During Real Mode, this input is used as an interrupt line to stop the debug unit from Real Time mode and return the debug unit back to Run Time Mode (standard JTAG). This pin is also used as the ejtag_dint_n signal in the EJTAG mode.
jtag_tdo, ejtag_tpc	Output	Z	High	<b>JTAG Test Data Out</b> The jtag_tdo is serial data shifted out from instruction or data register on the falling edge of jtag_tck. When no data is shifted out, the jtag_tdo is tri-stated. During Real Time Mode, this signal provides a non-sequential program counter at the processor clock or at a division of processor clock. This pin is also used as the ejtag_tpc signal in the EJTAG mode.
jtag_tms	Input		—	<b>JTAG Test Mode Select</b> Requires external pull-up. The logic signal received at the jtag_tms input is decoded by the TAP controller to control test operation. jtag_tms is sampled on the rising edge of the jtag_tck.
jtag_trst_n	Input	L	—	<b>JTAG Test Reset</b> When neither JTAG nor EJTAG are being used, jtag_trst_n must be driven low (pulled down) or the jtag_tms/ejtag_tms signals must be pulled up and jtag_clk actively clocked.
ejtag_dclk	Output	Z	—	<b>EJTAG Test Clock</b> Processor Clock. During Real Time Mode, this signal is used to capture address and data from the ejtag_tpc signal at the processor clock speed or any division of the internal pipeline.
ejtag_pcst[2:0]	I/O	Z	Low	<b>EJTAG PC Trace Status Information</b> 111 (STL) Pipe line Stall 110 (JMP) Branch/Jump forms with PC output 101 (BRT) Branch/Jump forms with no PC output 100 (EXP) Exception generated with an exception vector code output 011 (SEQ) Sequential performance 010 (TST) Trace is outputted at pipeline stall time 001 (TSQ) Trace trigger output at performance time 000 (DBM) Run Debug Mode Alternate function: modebit[2:0].
ejtag_debugboot	Input		— Requires external pull-down	<b>EJTAG DebugBoot</b> The ejtag_debugboot input is used during reset and forces the CPU core to take a debug exception at the end of the reset sequence instead of a reset exception. This enables the CPU to boot from the ICE probe without having the external memory working. This input signal is level sensitive and is not latched internally. This signal will also set the JtagBrk bit in the JTAG_Control_Register[12].
ejtag_tms	Input		— Requires external pull-up	<b>EJTAG Test Mode Select</b> An external pull-up on the board is required. The ejtag_tms is sampled on the rising edge of jtag_tck.

Table 1 Pin Description (Part 6 of 7)

Name	Type	Reset State Status	Drive Strength Capability	Description
<b>Debug Signals</b>				
debug_cpu_dma_n	I/O	Z	Low	<b>Debug CPU versus DMA Negated</b> De-assertion high during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction was generated from the CPU. Assertion low during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction was generated from DMA. Alternate function: modebit[6].
debug_cpu_ack_n	I/O	Z	Low	<b>Debug CPU Acknowledge Negated</b> Indicates either a data acknowledge to the CPU or DMA. Alternate function: modebit[4].
debug_cpu_ads_n	I/O	Z	Low	<b>Debug CPU Address/Data Strobe Negated</b> Assertion indicates that either a CPU or a DMA transaction is beginning and that the mem_data[31:4] bus has the current block address. Alternate function: modebit[5].
debug_cpu_i_d_n	I/O	Z	Low	<b>Debug CPU Instruction versus Data Negated</b> Assertion during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction is a CPU or DMA data transaction. De-assertion during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction is a CPU instruction transaction. Alternate function: modebit[3].

Table 1 Pin Description (Part 7 of 7)

## Mode Bit Settings to Configure Controller on Reset

The following table lists the mode bit settings to configure the controller on cold reset.

Pin	Mode Bit	Description	Value	Mode Setting
ejtag_pcst[2:0]	2:0 MSB (2)	Clock Multiplier <b>MasterClock</b> is multiplied internally to generate PClock	0	Multiply by 2
			1	Multiply by 3
			2	Multiply by 4
			3	Reserved
			4	Reserved
			5	Reserved
			6	Reserved
			7	Reserved
debug_cpu_i_d_n	3	EndBit	0	Little-endian ordering
			1	Big-endian ordering
debug_cpu_ack_n	4	Reserved	0	
debug_cpu_ads_n	5	Reserved	0	
debug_cpu_dma_n	6	TmrIntEn Enables/Disables the timer interrupt on Int*[5]	0	Enables timer interrupt
			1	Disables timer interrupt
mem_addr[17]	7	Reserved for future use	1	

Table 2 Boot-Mode Configuration Settings (Part 1 of 2)



Pin	Mode Bit	Description	Value	Mode Setting
mem_addr[19:18]	9:8 MSB (9)	Boot-Prom Width specifies the memory port width of the memory space which contains the boot prom.	00	8 bits
			01	16 bits
			10	32 bits
			11	Reserved

Table 2 Boot-Mode Configuration Settings (Part 2 of 2)

### reset\_boot\_mode Settings

By using the non-boot mode cold reset initialization mode the user can change the internal register addresses from base 1800\_0000 to base 1900\_0000, as required. The RC32334 cold reset-boot mode initialization setting values and mode descriptions are listed below.

Pin	Reset Boot Mode	Description	Value	Mode Settings
mem_addr[22:21]	1:0 MSB (1)	Tri-state memory bus and EEPROM bus during cold reset_n assertion	11	Tri-state_bus_mode
		Reserved	10	
		<b>PCI-boot mode</b> (pci_host_mode must be in satellite mode) RC32334 will reset either from a cold reset or from a PCI reset. Boot code is provided via PCI.	01	PCI_boot_mode
		<b>Standard-boot mode</b> Boot from the RC32334's memory controller (typical system).	00	standard_boot_mode

Table 3 RC32334 reset\_boot\_mode Initialization Settings

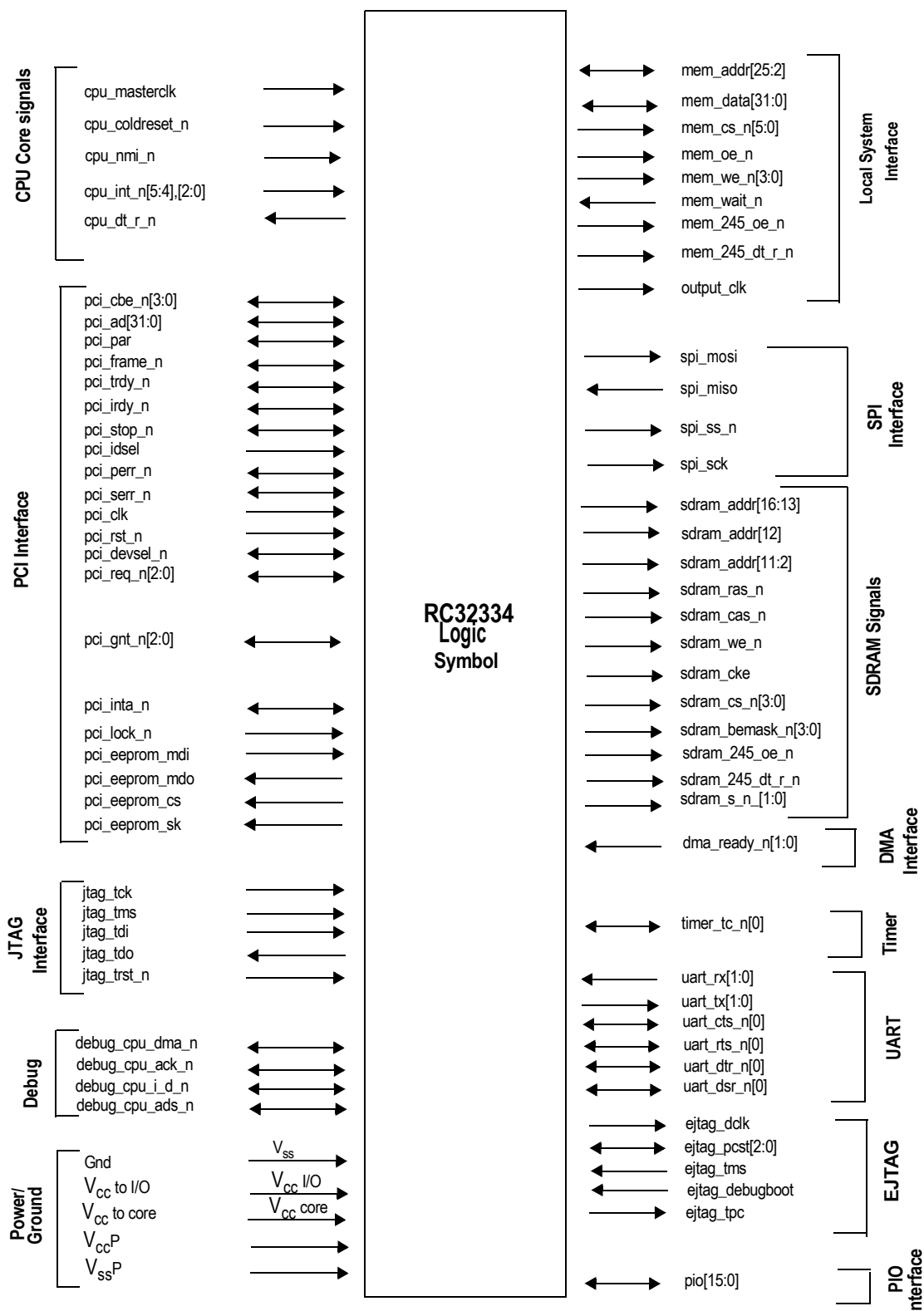
### pci\_host\_mode Settings

During cold reset initialization, the RC32334's PCI interface can be set to the Satellite or Host mode settings. When set to the Host mode, the CPU must configure the RC32334's PCI configuration registers, including the read-only registers. If the RC32334's PCI is in the PCI-boot mode Satellite mode, read-only configuration registers are loaded by the serial EEPROM.

Pin	Reset Boot Mode	Description	Value	Mode Settings
mem_addr[20]	PCI host mode	PCI is in satellite mode	1	PCI_satellite
		PCI is in host mode (typical system)	0	PCI_host

Table 4 RC32334 pci\_host\_mode Initialization Settings

# Logic Diagram — RC32334



## Clock Parameters — RC32334

(Ta = 0°C to +70°C Commercial, Ta = -40°C to +85°C Industrial, V<sub>cc</sub> I/O = +3.3V±5%, V<sub>cc</sub> Core = +3.3V±5%)

Parameter	Symbol	Test Conditions	RC32334 100MHz		RC32334 133MHz		RC32334 150MHz		Units
			Min	Max	Min	Max	Min	Max	
cpu_masterclock HIGH	t <sub>MCHIGH</sub>	Transition ≤ 2ns	8	—	6.75	—	6	—	ns
cpu_masterclock LOW	t <sub>MCLOW</sub>	Transition ≤ 2ns	8	—	6.75	—	6	—	ns
cpu_masterclock period <sup>1</sup>	t <sub>MCP</sub>	—	20	66.6	15	66.6	13.33	66.6	ns
cpu_masterclock Rise & Fall Time <sup>2</sup>	t <sub>MCRise</sub> , t <sub>MCFall</sub>	—	—	3	—	3	—	3	ns
cpu_masterclock Jitter	t <sub>JITTER</sub>	—	—	± 250	—	± 250	—	± 200	ps
pci_clk Rise & Fall Time	t <sub>PCRise</sub> , t <sub>PCFall</sub>	PCI 2.2	—	1.6	—	1.6	—	1.6	ns
pci_clk Period <sup>1</sup>	t <sub>PCP</sub>	—	15	—	15	—	15	—	ns
jtag_tck Rise & Fall Time	t <sub>JCRise</sub> , t <sub>JCFall</sub>	—	—	5	—	5	—	5	ns
eitag_dck period	t <sub>DCK</sub> , t <sub>t1</sub>	—	10	—	10	—	10	—	ns
jtag_tck clock period	t <sub>TCK</sub> , t <sub>3</sub>	—	100	—	100	—	100	—	ns
eitag_dck High, Low Time	t <sub>DCK High</sub> , t <sub>9</sub> t <sub>DCK Low</sub> , t <sub>10</sub>	—	4	—	4	—	4	—	ns
eitag_dck Rise, Fall Time	t <sub>DCK Rise</sub> , t <sub>9</sub> t <sub>DCK Fall</sub> , t <sub>10</sub>	—	—	1	—	1	—	1	ns
output_clk <sup>3</sup>	Tdo21	—	N/A	N/A	N/A	N/A	N/A	N/A	—
cpu_coldreset_n Asserted during power-up	—	power-on sequence	120	—	120	—	120	—	ms
cpu_coldreset_n Rise Time	t <sub>CRRise</sub>	—	—	5	—	5	—	5	ns

Table 5 Clock Parameters - RC32334

<sup>1</sup> cpu\_masterclock frequency should never be below pci\_clk frequency if PCI interface is used.

<sup>2</sup> Rise and fall times are measured between 10% and 90%

<sup>3</sup> Output\_clk should not be used in a system. Only the cpu\_masterclock or its derivative must be used to drive all the subsystems with designs based on the RC32334 device. Refer to the RC3233x Device Errata for more information.

## Reset Specification

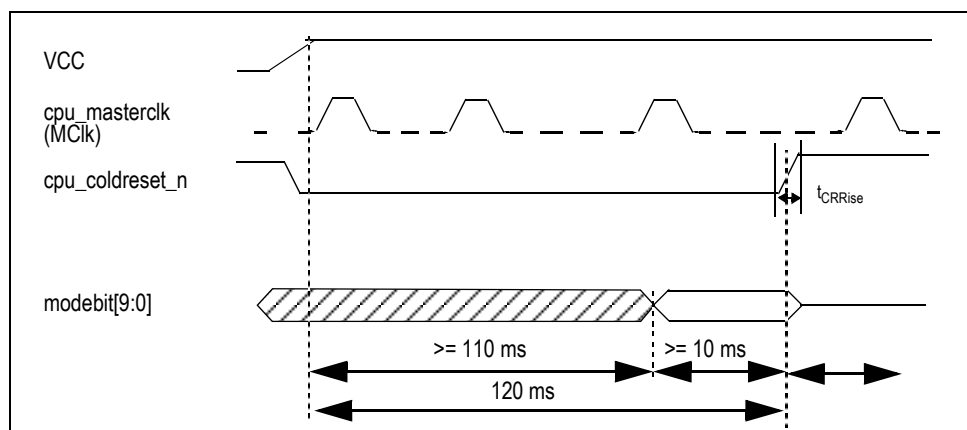


Figure 3 Mode Configuration Interface Cold Reset Sequence

Signal	Symbol	Reference Edge	RC32334 <sup>1</sup> 100MHz		RC32334 <sup>1</sup> 133MHz		RC32334 <sup>1</sup> 150MHz		Unit	User Manual Timing Diagram Reference	
			Min	Max	Min	Max	Min	Max			
UARTs											
uart_rx[1:0], uart_tx[1:0], uart_cts_n[0], uart_dsr_n[0], uart_dtr_n[0], uart_rts_n[0]	Tsu7	cpu_masterclk rising	15	—	12	—	10	—	ns	Chapter 17, Figure 17.16	
uart_rx[1:0], uart_tx[1:0], uart_cts_n[0], uart_dsr_n[0], uart_dtr_n[0], uart_rts_n[0]	Thld9	cpu_masterclk rising	15	—	12	—	10	—	ns		
uart_rx[1:0], uart_tx[1:0], uart_cts_n[0], uart_dsr_n[0], uart_dtr_n[0], uart_rts_n[0]	Tdo16	cpu_masterclk rising	—	15	—	12	—	10	ns		
uart_rx[1:0], uart_tx[1:0], uart_cts_n[0], uart_dsr_n[0], uart_dtr_n[0], uart_rts_n[0]	Tdoh8	cpu_masterclk rising	1	—	1	—	1	—	ns		
SPI Interface											
spi_clk, spi_mosi, spi_miso	Tsu7	cpu_masterclk rising	15	—	12	—	10	—	ns	Chapter 18, Figures 18.8 and 18.9	
spi_clk, spi_mosi, spi_miso	Thld9	cpu_masterclk rising	15	—	12	—	10	—	ns		
spi_clk, spi_mosi, spi_miso	Tdo16	cpu_masterclk rising	—	15	—	12	—	10	ns		
spi_clk, spi_mosi, spi_miso	Tdoh8	cpu_masterclk rising	1	—	1	—	1	—	ns		
Reset											
mem_addr[19:17]	Tsu10	cpu_coldreset_n rising	10	—	10	—	10	—	ms	Chapter 19 Figures 19.8 and 19.9	
mem_addr[19:17]	Thld10	cpu_coldreset_n rising	1	—	1	—	1	—	ns		
mem_addr[22:20],	Tsu22	cpu_masterclk rising	9	—	7	—	6	—	ns		
mem_addr[22:20]	Thld22	cpu_masterclk rising	1	—	1	—	1	—	ns		
Debug Interface											
debug_cpu_dma_n, debug_cpu_ack_n, debug_cpu_ads_n, debug_cpu_i_d_n, ejtag_pcst[2:0]	Tsu20	cpu_coldreset_n rising	10	—	10	—	10	—	ms	Chapter 19, Figure 19.9 and Chapter 9, Figure 9.2	
debug_cpu_dma_n, debug_cpu_ack_n, debug_cpu_ads_n, debug_cpu_i_d_n, ejtag_pcst[2:0]	Thld20	cpu_coldreset_n rising	1	—	1	—	1	—	ns		
debug_cpu_dma_n, debug_cpu_ack_n, debug_cpu_ads_n, debug_cpu_i_d_n	Tdo20	cpu_masterclk rising	—	15	—	12	—	10	ns		
debug_cpu_dma_n, debug_cpu_ack_n, debug_cpu_ads_n, debug_cpu_i_d_n	Tdoh20	cpu_masterclk rising	1	—	1	—	1	—	ns		
JTAG Interface											
jtag_tms, jtag_tdi, jtag_trst_n	t <sub>5</sub>	jtag_tck rising	10	—	10	—	10	—	ns	See Figure 4 below.	
jtag_tms, jtag_tdi, jtag_trst_n	t <sub>6</sub>	jtag_tck rising	10	—	10	—	10	—	ns		
jtag_tdo	t <sub>4</sub>	jtag_tck falling	—	10	—	10	—	10	ns		

Table 6 AC Timing Characteristics - RC32334 (Part 3 of 4)

Signal	Symbol	Reference Edge	RC32334 <sup>1</sup> 100MHz		RC32334 <sup>1</sup> 133MHz		RC32334 <sup>1</sup> 150MHz		Unit	User Manual Timing Diagram Reference
			Min	Max	Min	Max	Min	Max		

**EJTAG Interface**

ejtag_tms, ejtag_debugboot	t <sub>5</sub>	jtag_tclk rising	4	—	4	—	4	—	ns	See Figure 4 below.
ejtag_tms, ejtag_debugboot	t <sub>6</sub>	jtag_clk rising	2	—	2	—	2	—	ns	
jtag_tdo Output Delay Time	t <sub>TDOD</sub> , t <sub>4</sub>	jtag_tck falling	—	6	—	6	—	6	ns	
jtag_tdi Input Setup Time	t <sub>DIS</sub> , t <sub>5</sub>	jtag_tck rising	4	—	4	—	4	—	ns	
jtag_tdi Input Hold Time	t <sub>DIH</sub> , t <sub>6</sub>	jtag_tck rising	2	—	2	—	2	—	ns	
jtag_trst_n Low Time	t <sub>TRSTLow</sub> , t <sub>12</sub>	—	100	—	100	—	100	—	ns	
jtag_trst_n Removal Time	t <sub>TRSTR</sub> , t <sub>13</sub>	jtag_tck rising	3	—	3	—	3	—	ns	
ejtag_tpc Output Delay Time	t <sub>TPCDO</sub> , t <sub>8</sub>	ejtag_dclk rising	-1	3	-1	3	-1	3	ns	
ejtag_pcst Output Delay Time	t <sub>PCSTDO</sub> , t <sub>7</sub>	ejtag_dclk rising	-1	3	-1	3	-1	3	ns	

**Table 6 AC Timing Characteristics - RC32334 (Part 4 of 4)**

<sup>1</sup>. At all pipeline frequencies.

<sup>2</sup>. Guaranteed by design.

<sup>3</sup>. pci\_rst\_n is tested per PCI 2.2 as an asynchronous signal.

**Standard EJTAG Timing — RC32334**

Figure 4 represents the timing diagram for the EJTAG interface signals.

The standard JTAG connector is a 10-pin connector providing 5 signals and 5 ground pins. For Standard EJTAG, a 24-pin connector has been chosen providing 12 signals and 12 ground pins. This guarantees elimination of noise problems by incorporating signal-ground type arrangement. Refer to the RC32334 User Reference Manual for connector pinout and mechanical specifications.

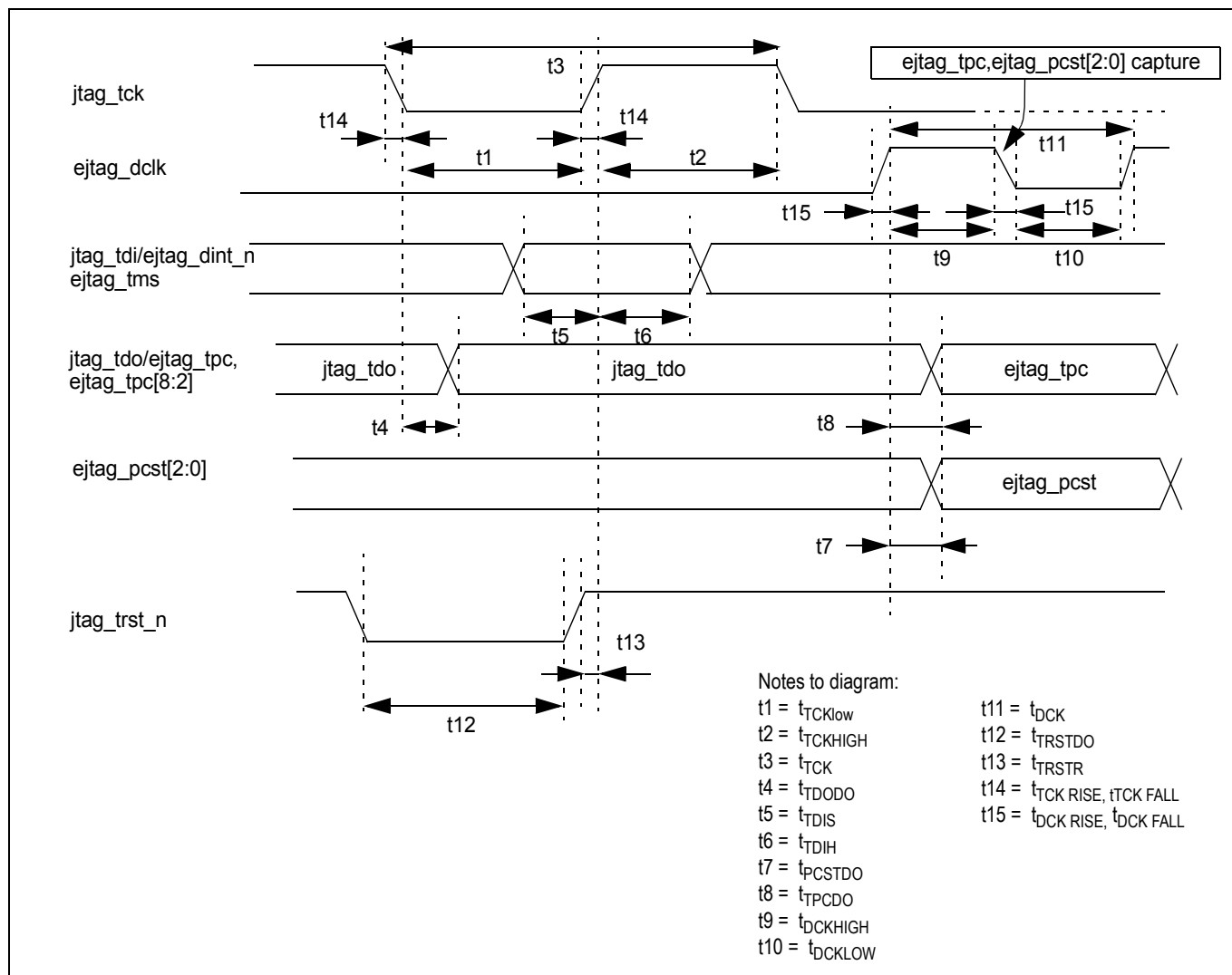
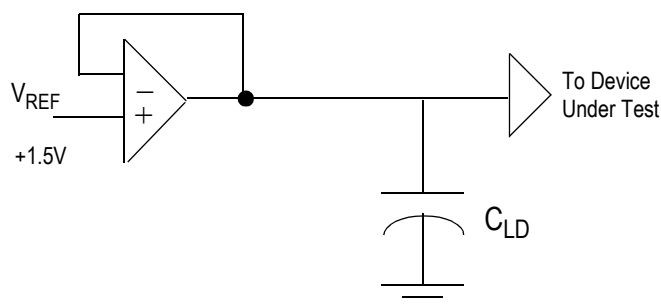


Figure 4 Standard EJTAG Timing

## Output Loading for AC Testing



Signal	C <sub>ld</sub>
All High Drive Signals	50 pF
All Low Drive Signals	25 pF

Figure 5 Output Loading for AC Testing

Note: PCI pins have been correlated to PCI 2.2.

## Recommended Operation Temperature and Supply Voltage

Grade	Temperature	Gnd	V <sub>cc</sub> IO	V <sub>cc</sub> Core	V <sub>cc</sub> P
Commercial	0°C to +70°C (Ambient)	0V	3.3V±5%	3.3V±5%	3.3V±5%
Industrial	-40°C to +85°C (Ambient)	0V	3.3V±5%	3.3V±5%	3.3V±5%

Table 7 Temperature and Voltage

## DC Electrical Characteristics — RC32334

Commercial Temperature Range—RC32334

(T<sub>a</sub> = 0°C to +70°C Commercial, T<sub>a</sub> = -40°C to +85°C Industrial, V<sub>cc</sub> I/O = +3.3V±5%, V<sub>cc</sub> Core = +3.3V±5%)

	Parameter	RC32334 <sup>1</sup>		Pin Numbers	Conditions
		Minimum	Maximum		
Input Pads	V <sub>IL</sub>	—	0.8V	B14, E13, F4, K1, L2, M1, M3, M4, M14, N1-N3, P14, R2, R16	—
	V <sub>IH</sub>	2.0V	—		—
LOW Drive Output Pads	V <sub>OL</sub>	—	0.4V	A1, A12, A15, A16, B1, B2, B12, B15, C1-C3, C12, C13, C14, D12, D13, E1-E4, F1, F2, G1-G4, H1, H2, J1, J2, K2-K4, L1, L3, L4, P3, P14, R2, R15, R16, T16	I <sub>OUT</sub>   = 6mA
	V <sub>OH</sub>	V <sub>cc</sub> - 0.4V	—		I <sub>OUT</sub>   = 8mA
	V <sub>IL</sub>	—	0.8V		—
	V <sub>IH</sub>	2.0V	—		—
HIGH Drive Output Pads	V <sub>OL</sub>	—	0.4V	A2-A4, A6-A11, A13, A14, B3, B4, B6-B11, B13, B16, C4, C6-C8, C10, C11, C15, C16, D1-D4, D6, D7, D10, D11, D14-D16, E14, E15, F3, F13-F16, G13-G16, H15, H16, J13, J14, K5, K13, K14, K16, L13-L16, M2, M13, M16, P2, P4, R1, R3, R4	I <sub>OUT</sub>   = 7mA
	V <sub>OH</sub>	V <sub>cc</sub> - 0.4V	—		I <sub>OUT</sub>   = 16mA
	V <sub>IL</sub>	—	0.8V		—
	V <sub>IH</sub>	2.0V	—		—
PCI Drive Input Pads	V <sub>IL</sub>	—	—	P1, R1, R10, T2, T3	Per PCI 2.2
	V <sub>IH</sub>	—	—		

Table 8 DC Electrical Characteristics - RC32334 (Part 1 of 2)

	Parameter	RC32334 <sup>1</sup>		Pin Numbers	Conditions
		Minimum	Maximum		
PCI Drive Output Pads	$V_{OL}$	—	—	M15, N4-N7, N10-N16, P5-P13, P15, P16, R5-R9, R11-R14, T4-T15	Per PCI 2.2
	$V_{OH}$	—	—		
	$V_{IL}$	—	—		
	$V_{IH}$	—	—		
All Pads	$C_{IN}$	—	10pF	All input pads except T3 and R3	—
	$C_{IN}^2$	5pF	12pF	T3	Per PCI 2.2
	$C_{IN}^3$	—	8pF	R3	Per PCI 2.2
	$C_{OUT}$	—	10pF	All output pads	—
	$I/O_{LEAK}$	—	10 $\mu$ A	All non-internal pull-up pins	Input/Output Leakage
	$I/O_{LEAK}$	—	50 $\mu$ A	All internal pull-up pins	Input/Output Leakage

Table 8 DC Electrical Characteristics - RC32334 (Part 2 of 2)

<sup>1</sup> At all pipeline frequencies.<sup>2</sup> Applies only to pad T3.<sup>3</sup> Applies only to pad R3.

### Capacitive Load Deration — RC32334

Refer to the IDT document [79RC32334 IBIS Model](#) located on the company's web site.

### Power Consumption — RC32334

**Note:** This table is based on a 2:1 pipeline-to-bus clock ratio.

Parameter		100MHz RC32334		133MHz RC32334		150MHz RC32334		Unit	Conditions
		Typical	Max.	Typical	Max.	Typical	Max.		
$I_{CC}$	Normal mode	360	480	480	630	550	700	mA	$C_L$ = (See Figure 5, Output Loading for AC Testing) $T_a = 25^\circ\text{C}$ $V_{CC}$ core = 3.46V (for max. values) $V_{CC}$ I/O = 3.46V (for max. values) $V_{CC}$ core = 3.3V (for typical values) $V_{CC}$ I/O = 3.3V (for typical values)
	Standby mode <sup>1</sup>	250	370	330	480	390	540	mA	
Power Dissipation	Normal mode	1.2	1.7	1.5	2.2	1.7	2.4	W	
	Standby mode <sup>1</sup>	.87	1.3	1.1	1.7	1.3	1.9	W	

Table 9 Power Consumption

<sup>1</sup> RISCore 32300 CPU core enters Standby mode by executing WAIT instructions. On-chip logic outside the CPU core continues to function.

### Power Ramp-up

There is no special requirement for how fast  $V_{CC}$  I/O ramps up to 3.3V. However, all timing references are based on a stable  $V_{CC}$  I/O.



## Power Curves

The following two graphs contain the simulated power curves that show power consumption at various bus frequencies.

**Note:** Only pipeline frequencies that are integer multiples (2x, 3x, 4x) of bus frequencies are supported.

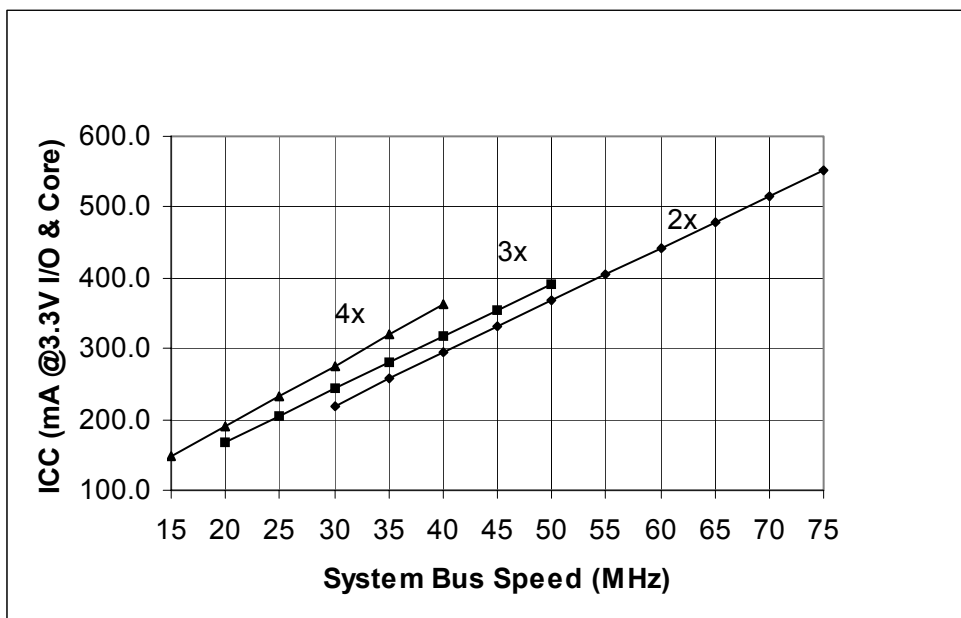


Figure 6 Typical Power Usage - RC32334

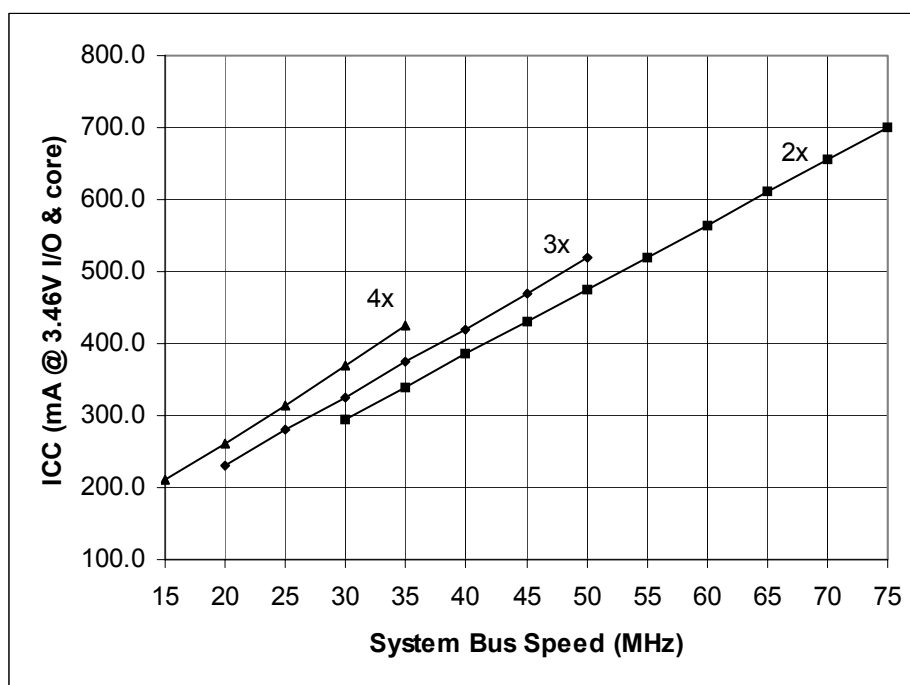


Figure 7 Maximum Power Usage - RC32334

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
B9	sdram_addr_12		F9	V <sub>ss</sub>		K9	V <sub>ss</sub>		P9	pci_cbe_n[2]	
B10	sdram_bemask_n[3]		F10	V <sub>ss</sub>		K10	V <sub>ss</sub>		P10	pci_devsel_n	
B11	mem_addr[16]	1	F11	V <sub>ss</sub>		K11	V <sub>ss</sub>		P11	pci_serr_n	
B12	mem_addr[20]	1	F12	V <sub>cc</sub> IO		K12	V <sub>cc</sub> IO		P12	pci_ad[14]	
B13	mem_data[11]		F13	mem_data[1]		K13	cpu_dt_r_n	2	P13	pci_ad[11]	
B14	cpu_coldreset_n		F14	mem_data[30]		K14	mem_data[6]		P14	cpu_int_n[5]	
B15	mem_addr[25]		F15	mem_data[31]		K15	mem_data[24]		P15	pci_ad[6]	
B16	mem_data[12]		F16	mem_data[0]		K16	mem_data[25]		P16	pci_ad[5]	
C1	uart_rx[0]	1	G1	dma_ready_n[0]	2	L1	ejtag_pcst[0]		R1	pci_req_n[2]	1
C2	uart_tx[0]	1	G2	mem_245_oe_n		L2	jtag_trst_n		R2	cpu_int_n[2]	
C3	uart_dtr_n[0]	1	G3	spi_mosi	2	L3	ejtag_pcst[1]	1	R3	pci_gnt_n[1]	2
C4	sdram_cs_n[0]		G4	spi_miso	2	L4	ejtag_pcst[2]	1	R4	pci_gnt_n[0]	
C5	sdram_s_n[0]		G5	V <sub>cc</sub> IO		L5	V <sub>cc</sub> IO		R5	pci_ad[29]	
C6	mem_addr[4]	1	G6	V <sub>ss</sub>		L6	V <sub>ss</sub>		R6	pci_ad[25]	
C7	mem_addr[9]	1	G7	V <sub>ss</sub>		L7	V <sub>ss</sub>		R7	pci_ad[22]	
C8	output_clk		G8	V <sub>ss</sub>		L8	V <sub>ss</sub>		R8	pci_ad[18]	
C9	mem_addr[12]		G9	V <sub>ss</sub>		L9	V <sub>ss</sub>		R9	pci_irdy_n	
C10	sdram_cs_n[3]		G10	V <sub>ss</sub>		L10	V <sub>ss</sub>		R10	pci_lock_n	
C11	mem_addr[14]	1	G11	V <sub>ss</sub>		L11	V <sub>ss</sub>		R11	pci_cbe_n[1]	
C12	mem_addr[18]	1	G12	V <sub>cc</sub> IO		L12	V <sub>cc</sub> IO		R12	pci_ad[12]	
C13	mem_addr[22]	1	G13	mem_data[3]		L13	mem_data[7]		R13	pci_ad[10]	
C14	mem_addr[24]		G14	mem_data[28]		L14	mem_data[8]		R14	pci_cbe_n[0]	
C15	mem_data[19]		G15	mem_data[29]		L15	mem_data[22]		R15	uart_tx[1]	1
C16	mem_data[13]		G16	mem_data[2]		L16	mem_data[23]		R16	cpu_int_n[4]	
D1	mem_we_n[1]		H1	spi_ss_n	1	M1	jtag_tms		T1	V <sub>ss</sub>	
D2	mem_we_n[3]		H2	spi_sck	2	M2	jtag_tdo		T2	pci_req_n[1]	1
D3	mem_we_n[2]		H3	V <sub>cc</sub> IO		M3	ejtag_tms		T3	pci_clk	
D4	mem_we_n[0]		H4	V <sub>cc</sub> core		M4	jtag_tck		T4	pci_ad[31]	
D5	sdram_s_n[1]		H5	V <sub>cc</sub> IO		M5	V <sub>cc</sub> IO		T5	pci_ad[28]	
D6	mem_addr[5]	1	H6	V <sub>ss</sub>		M6	V <sub>cc</sub> IO		T6	pci_ad[24]	
D7	mem_addr[8]	1	H7	V <sub>ss</sub>		M7	V <sub>cc</sub> IO		T7	pci_ad[21]	
D8	V <sub>ss</sub>		H8	V <sub>ss</sub>		M8	V <sub>cc</sub> IO		T8	pci_ad[17]	
D9	V <sub>cc</sub> core		H9	V <sub>ss</sub>		M9	V <sub>cc</sub> IO		T9	pci_frame_n	
D10	sdram_cs_n[2]		H10	V <sub>ss</sub>		M10	V <sub>cc</sub> IO		T10	pci_stop_n	
D11	mem_addr[13]	1	H11	V <sub>ss</sub>		M11	V <sub>cc</sub> IO		T11	pci_par	
D12	mem_addr[17]	1	H12	V <sub>cc</sub> IO		M12	V <sub>cc</sub> IO		T12	pci_ad[13]	
D13	mem_addr[21]	1	H13	V <sub>ss</sub> P		M13	mem_data[9]		T13	pci_ad[9]	

Table 11 RC32334 256-pin PBGA Package Pin-Out (Part 2 of 3)

**RC32334 Alternate Signal Functions**

Pin	Alt #1	Alt #2	Pin	Alt #1	Alt #2	Pin	Alt #1	Alt #2
A1	PIO[15]		C3	PIO[13]	C3	H2	PIO[9]	pci_eeeprom_sk
A6	sdram_addr[3]		C6	sdram_addr[4]		J1	modebit[6]	
A7	sdram_addr[7]		C7	sdram_addr[9]		J2	modebit[4]	
A8	sdram_addr[11]		C11	sdram_addr[14]		K3	modebit[3]	
A11	sdram_addr[15]		C12	modebit[8]		K4	modebit[5]	
A12	modebit[9]		C13	reset_boot_mode[1]		K13	mem_245_dt_r_n	sdram_245_dt_r_n
A16	PIO[2]	timer_gate_n[0]	D6	sdram_addr[5]		L1	modebit[0]	
B1	PIO[12]		D7	sdram_addr[8]		L3	modebit[1]	
B2	PIO[14]		D11	sdram_addr[13]		L4	modebit[2]	
B6	sdram_addr[2]		D12	modebit[7]		P2	pci_inta_n (satellite)	
B7	sdram_addr[6]		D13	reset_boot_mode[0]		P3	PIO[0]	dma_done_n[1]
B8	sdram_addr[10]		F4	sdram_wait_n		R1	pci_idsel (satellite)	
B11	sdram_addr[16]		G1	PIO[1]	dma_done_n[0]	R3	pci_eeeprom_cs (satellite)	PIO[11]
B12	reset_pci_host_mode		G3	PIO[10]	pci_eeeprom_mdo	R15	PIO[3]	
C1	PIO[6]		G4	PIO[7]	pci_eeeprom_mdi	T2	Unused (satellite)	
C2	PIO[5]		H1	PIO[8]		T16	PIO[4]	



