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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS-II
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	150MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	256-BBGA
Supplier Device Package	256-PBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79rc32v334-150bb

- **4 DMA Channels**
  - *4 general purpose DMA, each with endianess swappers and byte lane data alignment*
  - *Supports scatter/gather, chaining via linked lists of records*
  - *Supports memory-to-memory, memory-to-I/O, memory-to-PCI, PCI-to-PCI, and I/O-to-I/O transfers*
  - *Supports unaligned transfers*
  - *Supports burst transfers*
  - *Programmable DMA bus transactions burst size (up to 16 bytes)*
- **PCI Bus Interface**
  - *32-bit PCI, up to 66 MHz*
  - *Revision 2.2 compatible*
  - *Target or master*
  - *Host or satellite*
  - *Three slot PCI arbiter*
  - *Serial EEPROM support, for loading configuration registers*
- **Off-the-shelf development tools**
- **JTAG Interface (IEEE Std. 1149.1 compatible)**
- **256-ball BGA (1.0mm spacing)**
- **3.3V operation with 5V tolerant I/O**
- **EJTAG in-circuit emulator interface**

Device Overview

The IDT RC32334 device is an integrated processor based on the RC32300 CPU core. This product incorporates a high-performance, low-cost 32-bit CPU core with functionality common to a large number of embedded applications. The RC32334 integrates these functions to enable the use of low-cost PC commodity market memory and I/O devices, allowing the aggressive price/performance characteristics of the CPU to be realized quickly into low-cost systems.

CPU Execution Core

The RC32334 integrates the RISCore32300, the same CPU core found in the award-winning RC32364 microprocessor.

The RISCore32300 implements the Enhanced MIPS-II ISA. Thus, it is upwardly compatible with applications written for a wide variety of MIPS architecture processors, and it is kernel compatible with the modern operating systems that support IDT's 64-bit RISController product family.

The RISCore32300 was explicitly defined and designed for integrated processor products such as the RC32334. Key attributes of the execution core found within this product include:

- High-speed, 5-stage scalar pipeline executes to 150MHz. This high performance enables the RC32334 to perform a variety of performance intensive tasks, such as routing, DSP algorithms, etc.
- 32-bit architecture with enhancements of key capabilities. Thus, the RC32334 can execute existing 32-bit programs, while enabling designers to take advantage of recent advances in CPU architecture.
- Count leading-zeroes/ones. These instructions are common to a wide variety of tasks, including modem emulation, voice over IP compression and decompression, etc.
- Cache PREFetch instruction support, including a specialized form intended to help memory coherency. System programmers can allocate and stage the use of memory bandwidth to achieve maximum performance.
- 8kB of 2-way set associative instruction cache

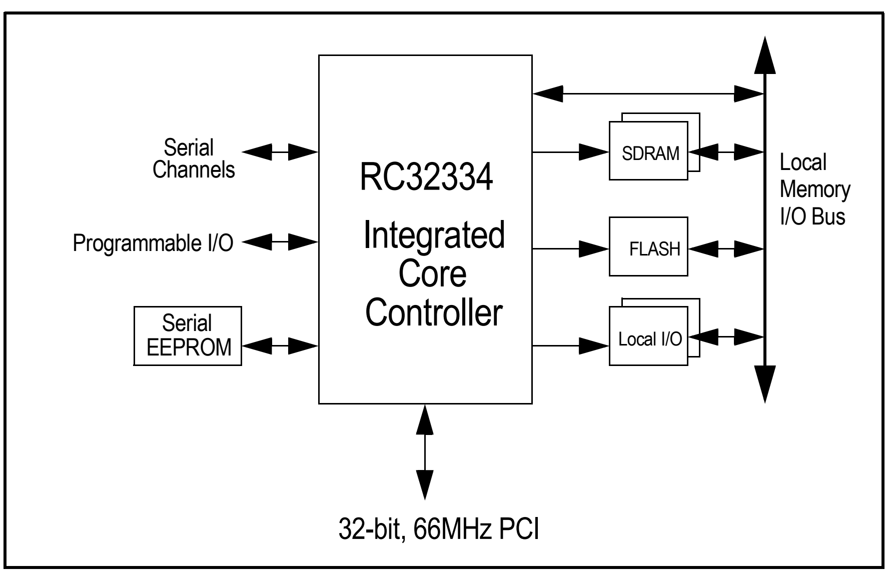


Figure 2 RC32334 Based System Diagram

Pin Description Table

The following table lists the pins provided on the RC32334. Note that those pin names followed by ”_n” are active-low signals. All external pull-ups and pull-downs require 10 kΩ resistor.

<table>
<tr><th>Name</th><th>Type</th><th>Reset State Status</th><th>Drive Strength Capability</th><th>Description</th></tr>
<tr><td colspan="5">Local System Interface</td></tr>
<tr><td>mem_data[31:0]</td><td>I/O</td><td>Z</td><td>High</td><td>Local System Data Bus
Primary data bus for memory. I/O and SDRAM.</td></tr>
<tr><td>mem_addr[25:2]</td><td>I/O</td><td>[25:10] Z
[9:2] L</td><td>[25:17] Low
[16:2] High</td><td>Memory Address Bus
These signals provide the Memory or DRAM address, during a Memory or DRAM bus transaction. During each word data, the address increments either in linear or sub-block ordering, depending on the transaction type. The table below indicates how the memory write enable signals are used to address discreet memory port width types.
<table>
<tr><th>Port Width</th><th>Pin Signals mem_we_n[3]</th><th>mem_we_n[2]</th><th>mem_we_n[1]</th><th>mem_we_n[0]</th></tr>
<tr><td>DMA (32-bit)</td><td>mem_we_n[3]</td><td>mem_we_n[2]</td><td>mem_we_n[1]</td><td>mem_we_n[0]</td></tr>
<tr><td>32-bit</td><td>mem_we_n[3]</td><td>mem_we_n[2]</td><td>mem_we_n[1]</td><td>mem_we_n[0]</td></tr>
<tr><td>16-bit</td><td>Byte High Write Enable</td><td>mem_addr[1]</td><td>Not Used (Driven Low)</td><td>Byte Low Write Enable</td></tr>
<tr><td>8-bit</td><td>Not Used (Driven High)</td><td>mem_addr[1]</td><td>mem_addr[0]</td><td>Byte Write Enable</td></tr>
</table>
mem_addr[22] Alternate function: reset_boot_mode[1].
mem_addr[21] Alternate function: reset_boot_mode[0].
mem_addr[20] Alternate function: reset_pci_host_mode.
mem_addr[19] Alternate function: modebit [9].
mem_addr[18] Alternate function: modebit [8].
mem_addr[17] Alternate function: modebit [7].
mem_addr[16] Alternate function: sdram_addr[16].
mem_addr[15] Alternate function: sdram_addr[15].
mem_addr[14] Alternate function: sdram_addr[14].
mem_addr[13] Alternate function: sdram_addr[13].
mem_addr[11] Alternate function: sdram_addr[11].
mem_addr[10] Alternate function: sdram_addr[10].
mem_addr[9] Alternate function: sdram_addr[9].
mem_addr[8] Alternate function: sdram_addr[8].
mem_addr[7] Alternate function: sdram_addr[7].
mem_addr[6] Alternate function: sdram_addr[6].
mem_addr[5] Alternate function: sdram_addr[5].
mem_addr[4] Alternate function: sdram_addr[4].
mem_addr[3] Alternate function: sdram_addr[3].
mem_addr[2] Alternate function: sdram_addr[2].</td></tr>
<tr><td>mem_cs_n[5:0]</td><td>Output</td><td>H</td><td>Low with internal pull-up</td><td>Memory Chip Select Negated
Recommend external pull-up.
Signals that a Memory Bank is actively selected.</td></tr>
<tr><td>mem_oe_n</td><td>Output</td><td>H</td><td>High</td><td>Memory Output Enable Negated
Recommend external pull-up.
Signals that a Memory Bank can output its data lines onto the cpu_ad bus.</td></tr>
</table>

Table 1 Pin Description (Part 1 of 7)

Name	Type	Reset State Status	Drive Strength Capability	Description
mem_we_n[3:0]	Output	H	High	**Memory Write Enable Negated Bus** Signals which bytes are to be written during a memory transaction. Bits act as Byte Enable and mem_addr[1:0] signals for 8-bit or 16-bit wide addressing.
mem_wait_n	Input		—	**Memory Wait Negated** Requires external pull-up. SRAM/IOI/IOM modes: Allows external wait-states to be injected during last cycle before data is sampled. DPM (dual-port) mode: Allows dual-port busy signal to restart memory transaction. Alternate function: sdram_wait_n.
mem_245_oe_n	Output	H	Low	**Memory FCT245 Output Enable Negated** Controls output enable to optional FCT245 transceiver bank by asserting during both reads and writes to a memory or I/O bank.
mem_245_dt_r_n	Output	Z	High	**Memory FCT245 Direction Xmit/Rcv Negated** Recommend external pull-up. Alternate function: cpu_dt_r_n. See CPU Core Specific Signals below.
output_clk	Output	cpu_mas terclk	High	**Output Clock** Optional clock output.
PCI Interface				
pci_ad[31:0]	I/O	Z	PCI	**PCI Multiplexed Address/Data Bus** Address driven by Bus Master during initial frame_n assertion, and then the Data is driven by the Bus Master during writes; or the Data is driven by the Bus Slave during reads.
pci_cbe_n[3:0]	I/O	Z	PCI	**PCI Multiplexed Command/Byte Enable Bus** Command (not negated) Bus driven by the Bus Master during the initial frame_n assertion. Byte Enable Negated Bus driven by the Bus Master during the data phase(s).
pci_par	I/O	Z	PCI	**PCI Parity** Even parity of the pci_ad[31:0] bus. Driven by Bus Master during Address and Write Data phases. Driven by the Bus Slave during the Read Data phase.
pci_frame_n	I/O	Z	PCI	**PCI Frame Negated** Driven by the Bus Master. Assertion indicates the beginning of a bus transaction. De-assertion indicates the last datum.
pci_trdy_n	I/O	Z	PCI	**PCI Target Ready Negated** Driven by the Bus Slave to indicate the current datum can complete.
pci_irdy_n	I/O	Z	PCI	**PCI Initiator Ready Negated** Driven by the Bus Master to indicate that the current datum can complete.
pci_stop_n	I/O	Z	PCI	**PCI Stop Negated** Driven by the Bus Slave to terminate the current bus transaction.
pci_idsel_n	Input		—	**PCI Initialization Device Select** Uses pci_req_n[2] pin. See the PCI subsection.
pci_perr_n	I/O	Z	PCI	**PCI Parity Error Negated** Driven by the receiving Bus Agent 2 clocks after the data is received, if a parity error occurs.
pci_serr_n	I/O Open-collector	Z	PCI	**System Error** External pull-up resistor is required. Driven by any agent to indicate an address parity error, data parity during a Special Cycle command, or any other system error.
pci_clk	Input		—	**PCI Clock** Clock for PCI Bus transactions. Uses the rising edge for all timing references.

Table 1 Pin Description (Part 2 of 7)

Name	Type	Reset State Status	Drive Strength Capability	Description
pci_rst_n	Input	L	—	**PCI Reset Negated** Host mode: Resets all PCI related logic. Satellite mode: Resets all PCI related logic and also warm resets the 32334.
pci_devsel_n	I/O	Z	PCI	**PCI Device Select Negated** Driven by the target to indicate that the target has decoded the present address as a target address.
pci_req_n[2]	Input	Z	—	**PCI Bus Request #2 Negated** Requires external pull-up. Host mode: pci_req_n[2] is an input indicating a request from an external device. Satellite mode: used as pci_idsel pin which selects this device during a configuration read or write. Alternate function: pci_idsel (satellite).
pci_req_n[1]	Input	Z	—	**PCI Bus Request #1 Negated** Requires external pull-up. Host mode: pci_req_n[1] is an input indicating a request from an external device. Alternate function: Unused (satellite).
pci_req_n[0]	I/O	Z	High	**PCI Bus Request #0 Negated** Requires external pull-up for burst mode. Host mode: pci_req_n[0] is an input indicating a request from an external device. Satellite mode: pci_req_n[0] is an output indicating a request from this device.
pci_gnt_n[2]	Output	Z[1]	High	**PCI Bus Grant #2 Negated** Recommend external pull-up. Host mode: pci_gnt_n[2] is an output indicating a grant to an external device. Satellite mode: pci_gnt_n[2] is used as the pci_inta_n output pin. Alternate function: pci_inta_n (satellite).
pci_gnt_n[1] / pci_eeprom_cs	I/O	X for 1 pci clock then H[2]	High	**PCI Bus Grant #1 Negated** Recommend external pull-up. Host mode: pci_gnt_n[1] is an output indicating a grant to an external device. Satellite mode: Used as pci_eprom_cs output pin for Serial Chip Select for loading PCI Configuration Registers in the RC32334 Reset Initialization Vector PCI boot mode. Defaults to the output direction at reset time. 1st Alternate function: pci_eeprom_cs (satellite). 2nd Alternate function: PIO[11].
pci_gnt_n[0]	I/O	Z	High	**PCI Bus Grant #0 Negated** Host mode: pci_gnt_n[0] is an output indicating a grant to an external device. Recommend external pull-up. Satellite mode: pci_gnt_n[0] is an input indicating a grant to this device. Require external pull-up.
pci_inta_n	Output Open-collector	Z	PCI	**PCI Interrupt #A Negated** Uses pci_gnt_n[2]. See the PCI subsection.
pci_lock_n	Input		—	**PCI Lock Negated** Driven by the Bus Master to indicate that an exclusive operation is occurring.

[1] Z in host mode; L in satellite non-boot mode; Z in satellite boot mode.
[2] H in host mode; L in satellite non-boot and boot modes. X = unknown.

SDRAM Control Interface

Name	Type	Reset State Status	Drive Strength Capability	Description
sdram_addr_12	Output	L	High	**SDRAM Address Bit 12 and Precharge All** SDRAM mode: Provides SDRAM address bit 12 (10 on the SDRAM chip) during row address and "pre-charge all" signal during refresh, read and write command.
sdram_ras_n	Output	H	High	**SDRAM RAS Negated** SDRAM mode: Provides SDRAM RAS control signal to all SDRAM banks.

Table 1 Pin Description (Part 3 of 7)

Name	Type	Reset State Status	Drive Strength Capability	Description
uart_tx[1:0]	I/O	Z	Low	**UART Transmit Data Bus** UART mode: Each UART channel sends data on their respective output pin. Note that these pins default to inputs at reset time and must be programmed via the PIO interface before being used as UART outputs. uart_tx[0] Alternate function: PIO[5]. uart_tx[1] Alternate function: PIO[3].
uart_cts_n[0] uart_dsr_n[0] uart_dtr_n[0] uart_rts_n[0]	I/O	Z	Low	**UART Transmit Data Bus** UART mode: Data bus modem control signal pins for UART channel 0. uart_cts_n[0] Alternate function: PIO[15]. uart_dsr_n[0] Alternate function: PIO[14]. uart_dtr_n[0] Alternate function: PIO[13]. uart_rts_n[0] Alternate function: PIO[12].
spi_mosi	I/O	L	Low	**SPI Data Output** Serial mode: Output pin from RC32334 as an Input to a Serial Chip for the Serial data input stream. In PCI satellite mode, acts as an Output pin from RC32334 that connects as an Input to a Serial Chip for the Serial data input stream for loading PCI Configuration Registers in the RC32334 Reset Initialization Vector PCI boot mode. 1st Alternate function: PIO[10]. Defaults to the output direction at reset time. 2nd Alternate function: pci_eeprom_mdo.
spi_miso	I/O	Z	Low	**SPI Data Input** Serial mode: Input pin to RC32334 from the Output of a Serial Chip for the Serial data output stream. In PCI satellite mode, acts as an Input pin from RC32334 that connects as an output to a Serial Chip for the Serial data output stream for loading PCI Configuration Registers in the RC32334 Reset Initialization Vector PCI boot mode. Defaults to input direction at reset time. 1st Alternate function: PIO[7]. 2nd Alternate function: pci_eeprom_mdi.
spi_sck	I/O	L	Low	**SPI Clock** Serial mode: Output pin for Serial Clock. In PCI satellite mode, acts as an Output pin for Serial Clock for loading PCI Configuration Registers in the RC323334 Reset Initialization Vector PCI boot mode. 1st Alternate function: PIO[9]. Defaults to the output direction at reset time. 2nd Alternate function: pci_eeprom_sk.
spi_ss_n	I/O	H	Low	**SPI Chip Select** Output pin selecting the serial protocol device as opposed to the PCI satellite mode EEPROM device. Alternate function: PIO[8]. Defaults to the output direction at reset time.
CPU Core Specific Signals				
cpu_nmi_n	Input		—	**CPU Non-Maskable Interrupt** Requires external pull-up. This interrupt input is active low to the CPU.
cpu_masterclk	Input		—	**CPU Master System Clock** Provides the basic system clock.
cpu_int_n[5:4], [2:0]	Input		—	**CPU Interrupt** Requires external pull-up. These interrupt inputs are active low to the CPU.
cpu_coldreset_n	Input	L	—	**CPU Cold Reset** This active-low signal is asserted to the RC32334 after V_{CC} becomes valid on the initial power-up. The Reset initialization vectors for the RC32334 are latched by cold reset.

Table 1 Pin Description (Part 5 of 7)

Name	Type	Reset State Status	Drive Strength Capability	Description
cpu_dt_r_n	Output	Z	—	**CPU Direction Transmit/Receive** This active-low signal controls the DT/R pin of an optional FCT245 transceiver bank. It is asserted during read operations. 1st Alternate function: mem_245_dt_r_n. 2nd Alternate function: sdram_245_dt_r_n.
JTAG Interface Signals				
jtag_tck	Input		—	**JTAG Test Clock** Requires external pull-down. An input test clock used to shift into or out of the Boundary-Scan register cells. jtag_tck is independent of the system and the processor clock with nominal 50% duty cycle.
jtag_tdi, ejtag_dint_n	Input		—	**JTAG Test Data In** Requires an external pull-up on the board. On the rising edge of jtag_tck, serial input data are shifted into either the Instruction or Data register, depending on the TAP controller state. During Real Mode, this input is used as an interrupt line to stop the debug unit from Real Time mode and return the debug unit back to Run Time Mode (standard JTAG). This pin is also used as the ejtag_dint_n signal in the EJTAG mode.
jtag_tdo, ejtag_tpc	Output	Z	High	**JTAG Test Data Out** The jtag_tdo is serial data shifted out from instruction or data register on the falling edge of jtag_tck. When no data is shifted out, the jtag_tdo is tri-stated. During Real Time Mode, this signal provides a non-sequential program counter at the processor clock or at a division of processor clock. This pin is also used as the ejtag_tpc signal in the EJTAG mode.
jtag_tms	Input		—	**JTAG Test Mode Select** Requires external pull-up. The logic signal received at the jtag_tms input is decoded by the TAP controller to control test operation. jtag_tms is sampled on the rising edge of the jtag_tck.
jtag_trst_n	Input	L	—	**JTAG Test Reset** When neither JTAG nor EJTAG are being used, jtag_trst_n must be driven low (pulled down) or the jtag_tms/ejtag_tms signals must be pulled up and jtag_clk actively clocked.
ejtag_dclk	Output	Z	—	**EJTAG Test Clock** Processor Clock. During Real Time Mode, this signal is used to capture address and data from the ejtag_tpc signal at the processor clock speed or any division of the internal pipeline.
ejtag_pcst[2:0]	I/O	Z	Low	**EJTAG PC Trace Status Information** 111 (STL) Pipe line Stall 110 (JMP) Branch/Jump forms with PC output 101 (BRT) Branch/Jump forms with no PC output 100 (EXP) Exception generated with an exception vector code output 011 (SEQ) Sequential performance 010 (TST) Trace is outputted at pipeline stall time 001 (TSQ) Trace trigger output at performance time 000 (DBM) Run Debug Mode Alternate function: modebit[2:0].
ejtag_debugboot	Input		— Requires external pull-down	**EJTAG DebugBoot** The ejtag_debugboot input is used during reset and forces the CPU core to take a debug exception at the end of the reset sequence instead of a reset exception. This enables the CPU to boot from the ICE probe without having the external memory working. This input signal is level sensitive and is not latched internally. This signal will also set the JtagBrk bit in the JTAG_Control_Register[12].
ejtag_tms	Input		— Requires external pull-up	**EJTAG Test Mode Select** An external pull-up on the board is required. The ejtag_tms is sampled on the rising edge of jtag_tck.

Table 1 Pin Description (Part 6 of 7)

Name	Type	Reset State Status	Drive Strength Capability	Description
Debug Signals				
debug_cpu_dma_n	I/O	Z	Low	**Debug CPU versus DMA Negated** De-assertion high during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction was generated from the CPU. Assertion low during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction was generated from DMA. Alternate function: modebit[6].
debug_cpu_ack_n	I/O	Z	Low	**Debug CPU Acknowledge Negated** Indicates either a data acknowledge to the CPU or DMA. Alternate function: modebit[4].
debug_cpu_ads_n	I/O	Z	Low	**Debug CPU Address/Data Strobe Negated** Assertion indicates that either a CPU or a DMA transaction is beginning and that the mem_data[31:4] bus has the current block address. Alternate function: modebit[5].
debug_cpu_i_d_n	I/O	Z	Low	**Debug CPU Instruction versus Data Negated** Assertion during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction is a CPU or DMA data transaction. De-assertion during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction is a CPU instruction transaction. Alternate function: modebit[3].

Table 1 Pin Description (Part 7 of 7)

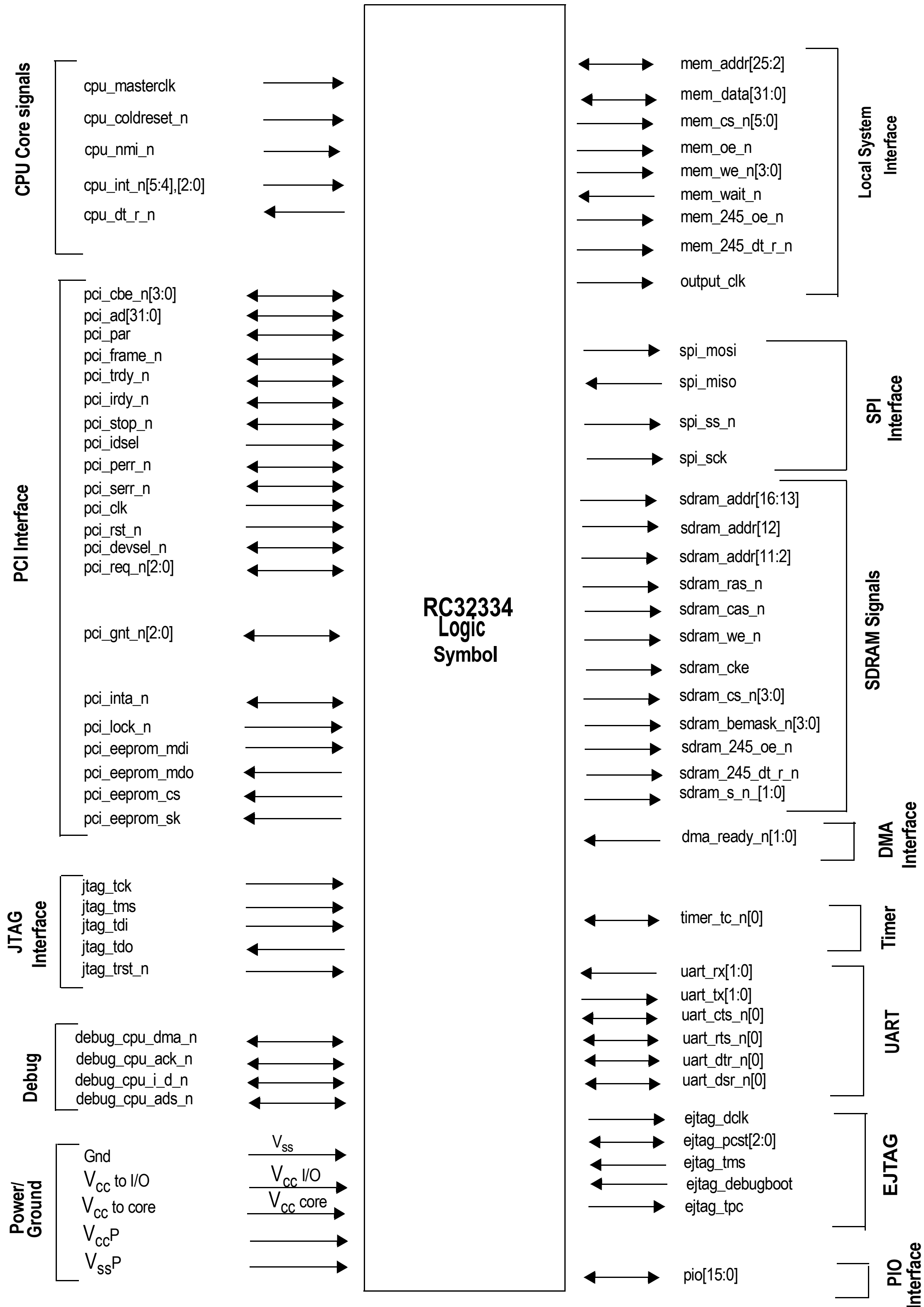
Mode Bit Settings to Configure Controller on Reset

The following table lists the mode bit settings to configure the controller on cold reset.

Pin	Mode Bit	Description	Value	Mode Setting
ejtag_pcst[2:0]	2:0 MSB (2)	Clock Multiplier **MasterClock** is multiplied internally to generate PClock	0	Multiply by 2
			1	Multiply by 3
			2	Multiply by 4
			3	Reserved
			4	Reserved
			5	Reserved
			6	Reserved
			7	Reserved
debug_cpu_i_d_n	3	EndBit	0	Little-endian ordering
			1	Big-endian ordering
debug_cpu_ack_n	4	Reserved	0	
debug_cpu_ads_n	5	Reserved	0	
debug_cpu_dma_n	6	TmrIntEn Enables/Disables the timer interrupt on Int*[5]	0	Enables timer interrupt
			1	Disables timer interrupt
mem_addr[17]	7	Reserved for future use	1	

Table 2 Boot-Mode Configuration Settings (Part 1 of 2)

Logic Diagram — RC32334



Power Ramp-up

There is no special requirement for how fast Vcc and VccP ramp up to 3.3V. However, all timing references are based on Vcc and VccP stabilized at 3.3V -5%.

AC Timing Characteristics — RC32334

(Ta = 0°C to +70°C Commercial, Ta = -40°C to +85°C Industrial, V_{cc} I/O = +3.3V±5%,V_{cc} Core = +3.3V±5%)

Signal	Symbol	Reference Edge	RC32334[1] 100MHz		RC32334[1] 133MHz		RC32334[1] 150MHz		Unit	User Manual Timing Diagram Reference
			Min	Max	Min	Max	Min	Max		
Local System Interface										
mem_data[31:0] (data phase)	Tsu2	cpu_masterclk rising	6	—	5	—	4.8	—	ns	
mem_data[31:0] (data phase)	Thld2	cpu_masterclk rising	1.5	—	1.5	—	1.5	—	ns	
cpu_dt_r_n	Tdo3	cpu_masterclk rising	—	15	—	12	—	10	ns	Chapter 9, Figures 9.2 and 9.3
mem_data[31:0]	Tdo4	cpu_masterclk rising	—	12	—	10	—	9.3	ns	
mem_data[31:0] output hold time	Tdoh1	cpu_masterclk rising	1	—	1	—	1	—	ns	
mem_data[31:0] (tristate disable time)	Tdz	cpu_masterclk rising	—	12[2]	—	10[2]	—	9.3[2]	ns	
mem_data[31:0] (tristate to data time)	Tzd	cpu_masterclk rising	—	12[2]	—	10[2]	—	9.3[2]	ns	
mem_wait_n	Tsu6	cpu_masterclk rising	9	—	7	—	6	—	ns	
mem_wait_n	Thld8	cpu_masterclk rising	1	—	1	—	1	—	ns	Chapter 10, Figures 10.6 through 10.8
mem_addr[25:2]	Tdo5	cpu_masterclk rising	—	12	—	9	—	8	ns	
mem_cs_n[5:0]	Tdo6	cpu_masterclk rising	—	12	—	9	—	8	ns	
mem_oe_n, mem_245_oe_n	Tdo7	cpu_masterclk rising	—	12	—	9	—	8	ns	
mem_we_n[3:0]	Tdo7a	cpu_masterclk rising	—	15	—	12	—	10	ns	
mem_245_dt_r_n	Tdo8	cpu_masterclk rising	—	15	—	12	—	10	ns	
mem_addr[25:2] mem_cs_n[5:0] mem_oe_n, mem_we_n[3:0], mem_245_dt_r_n, mem_245_oe_n	Tdoh3	cpu_masterclk rising	1.5	—	1.5	—	1.5	—	ns	
PCI										
pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n, pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n, pci_serr_n, pci_devsel_n, pci_lock_n[3]	Tsu	pci_clk rising	3	—	3	—	3	—	ns	
pci_idsel, pci_req_n[2], pci_req_n[1], pci_req_n[0], pci_gnt_n[0], pci_inta_n	Tsu	pci_clk rising	5	—	5	—	5	—	ns	
pci_gnt_n[0]	Tsu	pci_clk rising	5	—	5	—	5	—	ns	
pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n, pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n, pci_serr_n, pci_rst_n, pci_devsel_n, pci_lock_n[3]	Thld	pci_clk rising	0	—	0	—	0	—	ns	Per PCI 2.2
pci_idsel, pci_req_n[2], pci_req_n[1], pci_req_n[0], pci_gnt_n[0], pci_inta_n	Thld	pci_clk rising	0	—	0	—	0	—	ns	
pci_eeprom_mdi	Tsu	pci_clk rising, pci_eeprom_sk falling	15	—	12	—	10	—	ns	

Table 6 AC Timing Characteristics - RC32334 (Part 1 of 4)

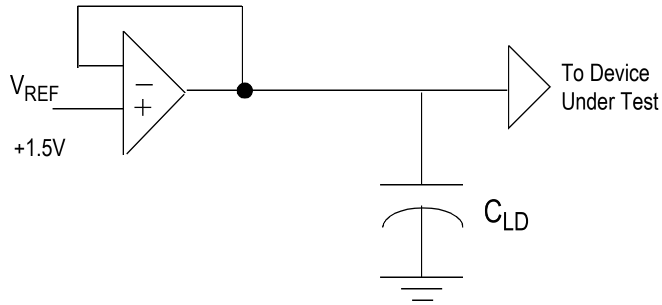
Signal	Symbol	Reference Edge	RC32334[1] 100MHz		RC32334[1] 133MHz		RC32334[1] 150MHz		Unit	User Manual Timing Diagram Reference
			Min	Max	Min	Max	Min	Max		
pci_eeprom_mdi	Thld	pci_clk rising, pci_eeprom_sk falling	15	—	12	—	10	—	ns	
pci_eeprom_mdo, pci_eeprom_cs	Tdo	pci_clk rising, pci_eeprom_sk falling	—	15	—	12	—	10	ns	
pci_eeprom_sk	Tdo	pci_clk rising	—	15	—	12	—	10	ns	
pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n, pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n, pci_serr_n, pci_devsel_n	Tdo	pci_clk rising	2	6	2	6	2	6	ns	Per PCI 2.2
pci_req_n[0], pci_gnt_[2], pci_gnt_n[1], pci_gnt_n[0], pci_inta_n	Tdo	pci_clk rising	2	6	2	6	2	6	ns	
SDRAM Controller										
sdram_245_dt_r_n	Tdo8	cpu_masterclk rising	—	15	—	12	—	10	ns	Chapter 11, Figures 11.4 and 11.5
sdram_ras_n, sdram_cas_n, sdram_we_n, sdram_cs_n[3:0], sdram_s_n[1:0], sdram_bemask_n[3:0], sdram_cke	Tdo9	cpu_masterclk rising	—	12	—	9	—	8	ns	
sdram_addr_12	Tdo10	cpu_masterclk rising	—	12	—	9	—	8	ns	
sdram_245_oe_n	Tdo11	cpu_masterclk rising	—	12	—	9	—	8	ns	
sdram_245_dt_r_n	Tdoh4	cpu_masterclk rising	1	—	1	—	1	—	ns	
sdram_ras_n, sdram_cas_n, sdram_we_n, sdram_cs_n[3:0], sdram_s_n[1:0], sdram_bemask_n[3:0] sdram_cke, sdram_addr_12, sdram_245_oe_n	Tdoh4	cpu_masterclk rising	2.5	—	2.5	—	2.5	—	ns	
DMA										
dma_ready_n[1:0], dma_done_n[1:0]	Tsu7	cpu_masterclk rising	9	—	7	—	6	—	ns	Chapter 13, Figure 13.4
dma_ready_n[1:0], dma_done_n[1:0]	Thld9	cpu_masterclk rising	1	—	1	—	1	—	ns	
Interrupt Handling										
cpu_int_n[5:4], cpu_int_n[2:0], cpu_nmi_n	Tsu9	cpu_masterclk rising	9	—	9	—	6	—	ns	Chapter 14, Figure 14.12
cpu_int_n[5:4], cpu_int_n[2:0], cpu_nmi_n	Thld13	cpu_masterclk rising	1	—	1	—	1	—	ns	
PIO										
PIO[15:0]	Tsu7	cpu_masterclk rising	9	—	7	—	6	—	ns	Chapter 15, Figures 15.9 and 15.10
PIO[15:0]	Thld9	cpu_masterclk rising	1	—	1	—	1	—	ns	
PIO[15:10], PIO[8:0]	Tdo16	cpu_masterclk rising	—	15	—	12	—	10	ns	
PIO[9]	Tdo19	cpu_masterclk rising	—	15	—	12	—	10	ns	
PIO[15:10], PIO[8:0]	Tdoh7	cpu_masterclk rising	1	—	1	—	1	—	ns	
PIO[9]	Tdoh7	cpu_masterclk rising	1	—	1	—	1	—	ns	
Timer										
timer_tc_n[0], timer_gate_n[0]	Tsu8	cpu_masterclk rising	9	—	7	—	6	—	ns	Chapter 16, Figures 16.6 and 16.7
timer_tc_n[0], timer_gate_n[0]	Thld10	cpu_masterclk rising	1	—	1	—	1	—	ns	
timer_tc_n[0], timer_gate_n[0]	Tdo15	cpu_masterclk rising	—	15	—	12	—	10	ns	
timer_tc_n[0], timer_gate_n[0]	Tdoh6	cpu_masterclk rising	1	—	1	—	1	—	ns	

Table 6 AC Timing Characteristics - RC32334 (Part 2 of 4)

Signal	Symbol	Reference Edge	RC32334[1] 100MHz		RC32334[1] 133MHz		RC32334[1] 150MHz		Unit	User Manual Timing Diagram Reference
			Min	Max	Min	Max	Min	Max		
UARTs										
uart_rx[1:0], uart_tx[1:0], uart_cts_n[0], uart_dsr_n[0], uart_dtr_n[0], uart_rts_n[0]	Tsu7	cpu_masterclk rising	15	—	12	—	10	—	ns	Chapter 17, Figure 17.16
uart_rx[1:0], uart_tx[1:0], uart_cts_n[0], uart_dsr_n[0], uart_dtr_n[0], uart_rts_n[0]	Thld9	cpu_masterclk rising	15	—	12	—	10	—	ns	
uart_rx[1:0], uart_tx[1:0], uart_cts_n[0], uart_dsr_n[0], uart_dtr_n[0], uart_rts_n[0]	Tdo16	cpu_masterclk rising	—	15	—	12	—	10	ns	
uart_rx[1:0], uart_tx[1:0], uart_cts_n[0], uart_dsr_n[0], uart_dtr_n[0], uart_rts_n[0]	Tdoh8	cpu_masterclk rising	1	—	1	—	1	—	ns	
SPI Interface										
spi_clk, spi_mosi, spi_miso	Tsu7	cpu_masterclk rising	15	—	12	—	10	—	ns	Chapter 18, Figures 18.8 and 18.9
spi_clk, spi_mosi, spi_miso	Thld9	cpu_masterclk rising	15	—	12	—	10	—	ns	
spi_clk, spi_mosi, spi_miso	Tdo16	cpu_masterclk rising	—	15	—	12	—	10	ns	
spi_clk, spi_mosi, spi_miso	Tdoh8	cpu_masterclk rising	1	—	1	—	1	—	ns	
Reset										
mem_addr[19:17]	Tsu10	cpu_coldreset_n rising	10	—	10	—	10	—	ms	Chapter 19 Figures 19.8 and 19.9
mem_addr[19:17]	Thld10	cpu_coldreset_n rising	1	—	1	—	1	—	ns	
mem_addr[22:20],	Tsu22	cpu_masterclk rising	9	—	7	—	6	—	ns	
mem_addr[22:20]	Thld22	cpu_masterclk rising	1	—	1	—	1	—	ns	
Debug Interface										
debug_cpu_dma_n, debug_cpu_ack_n, debug_cpu_ads_n, debug_cpu_i_d_n, ejtag_pcst[2:0]	Tsu20	cpu_coldreset_n rising	10	—	10	—	10	—	ms	Chapter 19, Figure 19.9 and Chapter 9, Figure 9.2
debug_cpu_dma_n, debug_cpu_ack_n, debug_cpu_ads_n, debug_cpu_i_d_n, ejtag_pcst[2:0]	Thld20	cpu_coldreset_n rising	1	—	1	—	1	—	ns	
debug_cpu_dma_n, debug_cpu_ack_n, debug_cpu_ads_n, debug_cpu_i_d_n	Tdo20	cpu_masterclk rising	—	15	—	12	—	10	ns	
debug_cpu_dma_n, debug_cpu_ack_n, debug_cpu_ads_n, debug_cpu_i_d_n	Tdoh20	cpu_masterclk rising	1	—	1	—	1	—	ns	
JTAG Interface										
jtag_tms, jtag_tdi, jtag_trst_n	t_5	jtag_tck rising	10	—	10	—	10	—	ns	See Figure 4 below.
jtag_tms, jtag_tdi, jtag_trst_n	t_6	jtag_tck rising	10	—	10	—	10	—	ns	
jtag_tdo	t_4	jtag_tck falling	—	10	—	10	—	10	ns	

Table 6 AC Timing Characteristics - RC32334 (Part 3 of 4)

Output Loading for AC Testing



Signal	Cld
All High Drive Signals	50 pF
All Low Drive Signals	25 pF

Figure 5 Output Loading for AC Testing

Note: PCI pins have been correlated to PCI 2.2.

Recommended Operation Temperature and Supply Voltage

Grade	Temperature	Gnd	V_{cc}IO	V_{cc}Core	V_{cc}P
Commercial	0°C to +70°C (Ambient)	0V	3.3V±5%	3.3V±5%	3.3V±5%
Industrial	-40°C to +85°C (Ambient)	0V	3.3V±5%	3.3V±5%	3.3V±5%

Table 7 Temperature and Voltage

DC Electrical Characteristics — RC32334

Commercial Temperature Range—RC32334

(Ta = 0°C to +70°C Commercial, Ta = -40°C to +85°C Industrial, V_{cc} I/O = +3.3V±5%, V_{cc} Core = +3.3V±5%)

	Parameter	RC32334[1]		Pin Numbers	Conditions
		Minimum	Maximum		
Input Pads	V_{IL}	—	0.8V	B14, E13, F4, K1, L2, M1, M3, M4, M14, N1-N3, P14, R2, R16	—
	V_{IH}	2.0V	—		—
LOW Drive Output Pads	V_{OL}	—	0.4V	A1, A12, A15, A16, B1, B2, B12, B15, C1-C3, C12, C13, C14, D12, D13, E1- E4, F1, F2, G1-G4, H1, H2, J1, J2, K2-K4, L1, L3, L4, P3, P14, R2, R15, R16, T16	$\lvert I_{OUT}\rvert$ = 6mA
	V_{OH}	V_{cc} - 0.4V	—		$\lvert I_{OUT}\rvert$ = 8mA
	V_{IL}	—	0.8V		—
	V_{IH}	2.0V	—		—
HIGH Drive Output Pads	V_{OL}	—	0.4V	A2-A4, A6-A11, A13, A14, B3, B4, B6-B11, B13, B16, C4, C6-C8, C10, C11, C15, C16, D1-D4, D6, D7, D10, D11, D14-D16, E14, E15, F3, F13-F16, G13-G16, H15, H16, J13, J14, K5, K13, K14, K16, L13-L16, M2, M13, M16, P2, P4, R1, R3, R4	$\lvert I_{OUT}\rvert$ = 7mA
	V_{OH}	V_{cc} - 0.4V	—		$\lvert I_{OUT}\rvert$ = 16mA
	V_{IL}	—	0.8V		—
	V_{IH}	2.0V	—		—
PCI Drive Input Pads	V_{IL}	—	—	P1, R1, R10, T2, T3	Per PCI 2.2
	V_{IH}	—	—		

Table 8 DC Electrical Characteristics - RC32334 (Part 1 of 2)

	Parameter	RC32334[1] Minimum	RC32334[1] Maximum	Pin Numbers	Conditions
PCI Drive Output Pads	V_{OL}	—	—	M15, N4-N7, N10-N16, P5-P13, P15, P16, R5-R9, R11-R14, T4-T15	Per PCI 2.2
	V_{OH}	—	—		
	V_{IL}	—	—		
	V_{IH}	—	—		
All Pads	C_{IN}	—	10pF	All input pads except T3 and R3	—
	C_{IN}[2]	5pF	12pF	T3	Per PCI 2.2
	C_{IN}[3]	—	8pF	R3	Per PCI 2.2
	C_{OUT}	—	10pF	All output pads	—
	I/O_{LEAK}	—	10µA	All non-internal pull-up pins	Input/Output Leakage
	I/O_{LEAK}	—	50µA	All internal pull-up pins	Input/Output Leakage

Table 8 DC Electrical Characteristics - RC32334 (Part 2 of 2)

1. At all pipeline frequencies.
2. Applies only to pad T3.
3. Applies only to pad R3.

Capacitive Load Deration — RC32334

Refer to the IDT document 79RC32334 IBIS Model located on the company's web site.

Power Consumption — RC32334

Note: This table is based on a 2:1 pipeline-to-bus clock ratio.

Parameter		100MHz RC32334 Typical	100MHz RC32334 Max.	133MHz RC32334 Typical	133MHz RC32334 Max.	150MHz RC32334 Typical	150MHz RC32334 Max.	Unit	Conditions
I_{CC}	Normal mode	360	480	480	630	550	700	mA	C_L = (See Figure 5, Output Loading for AC Testing) T_a = 25°C V_{cc} core = 3.46V (for max. values) V_{cc} I/O = 3.46V (for max. values) V_{cc} core = 3.3V (for typical values) V_{cc} I/O = 3.3V (for typical values)
	Standby mode[1]	250	370	330	480	390	540	mA	
Power Dissipation	Normal mode	1.2	1.7	1.5	2.2	1.7	2.4	W	
	Standby mode[1]	.87	1.3	1.1	1.7	1.3	1.9	W	

Table 9 Power Consumption

1. RISCore 32300 CPU core enters Standby mode by executing WAIT instructions. On-chip logic outside the CPU core continues to function.

Power Ramp-up

There is no special requirement for how fast V_{cc} I/O ramps up to 3.3V. However, all timing references are based on a stable V_{cc} I/O.

Power Curves

The following two graphs contain the simulated power curves that show power consumption at various bus frequencies.

Note: Only pipeline frequencies that are integer multiples (2x, 3x, 4x) of bus frequencies are supported.

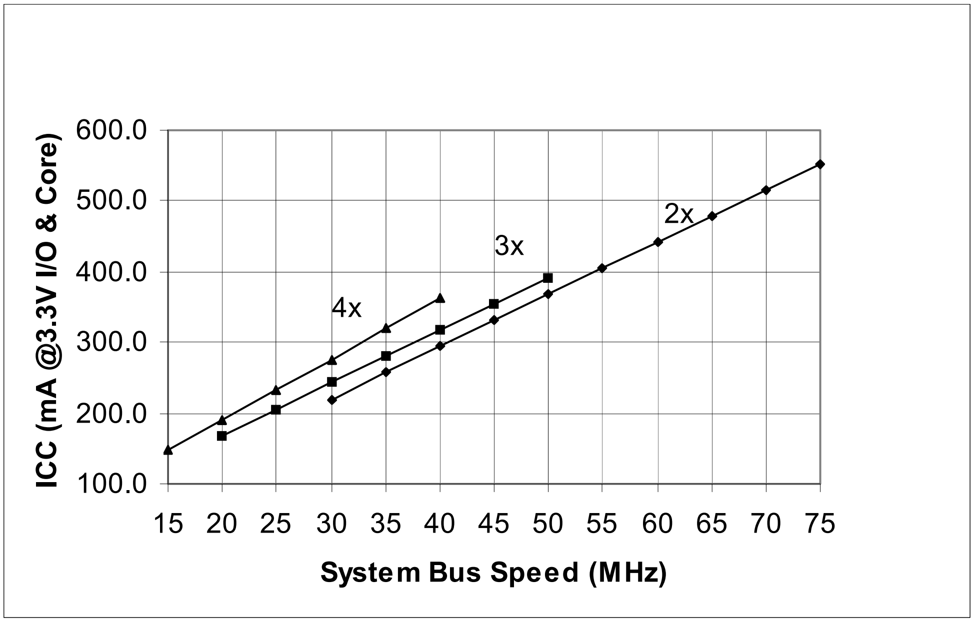


Figure 6 Typical Power Usage - RC32334

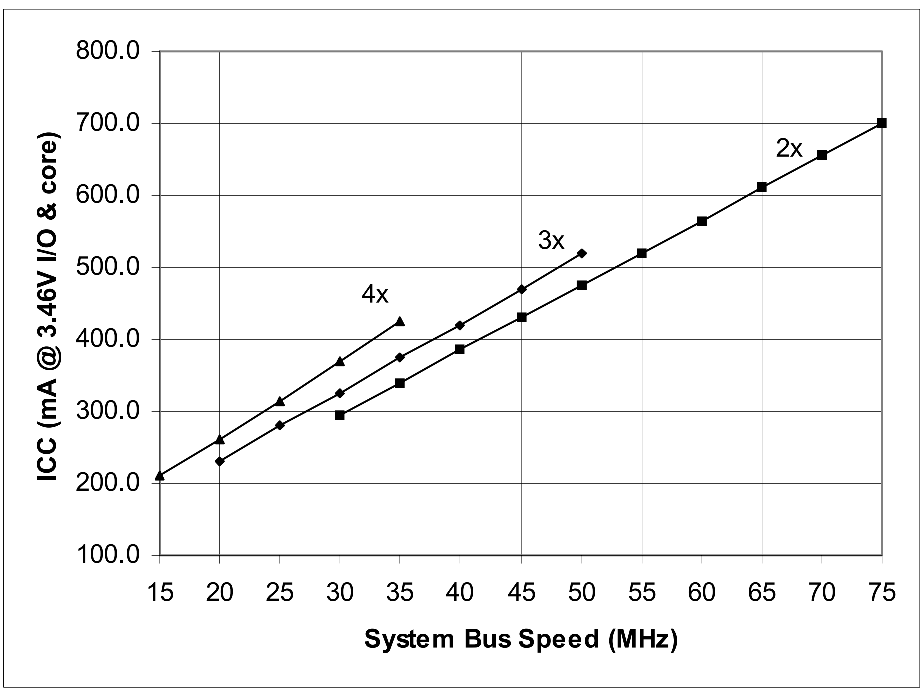


Figure 7 Maximum Power Usage - RC32334

Absolute Maximum Ratings

Symbol	Parameter	Min[1]	Max[1]	Unit
V_{CC}	Supply Voltage	-0.3	4.0	V
Vi	Input Voltage	-0.3	5.5	V
Vimin	Input Voltage - undershoot[2]	-0.6	—	V
Tstg	Storage Temperature	-40	125	degrees C

Table 10 Absolute Maximum Ratings

1. Functional and tested operating conditions are given in Table 7. Absolute maximum ratings are stress ratings only, and functional operation is not guaranteed beyond recommended operating voltages and temperatures. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. All PCI pads are fully compatible with PCI Specification version 2.2.

Package Pin-out — 256-PBGA Pinout for RC32334

The following table lists the pin numbers and signal names for the RC32334. Signal names ending with an "_n" are active when low.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	uart_cts_n[0]	1	E1	mem_cs_n[4]		J1	debug_cpu_dma_n	1	N1	cpu_int_n[1]	
A2	sdram_245_oe_n		E2	mem_cs_n[5]		J2	debug_cpu_ack_n	1	N2	cpu_int_n[0]	
A3	sdram_cas_n		E3	mem_cs_n[3]		J3	V_{cc} IO		N3	jtag_tdi	
A4	sdram_bemask_n[1]		E4	mem_cs_n[2]		J4	V_{ss}		N4	pci_ad[30]	
A5	sdram_ras_n		E5	V_{cc} IO		J5	V_{cc} IO		N5	pci_ad[26]	
A6	mem_addr[3]	1	E6	V_{cc} IO		J6	V_{ss}		N6	pci_ad[23]	
A7	mem_addr[7]	1	E7	V_{cc} IO		J7	V_{ss}		N7	pci_ad[19]	
A8	mem_addr[11]	1	E8	V_{cc} IO		J8	V_{ss}		N8	V_{cc} core	
A9	sdram_cke		E9	V_{cc} IO		J9	V_{ss}		N9	V_{ss}	
A10	sdram_bemask_n[2]		E10	V_{cc} IO		J10	V_{ss}		N10	pci_trdy_n	
A11	mem_addr[15]	1	E11	V_{cc} IO		J11	V_{ss}		N11	pci_perr_n	
A12	mem_addr[19]	1	E12	V_{cc} IO		J12	V_{cc} IO		N12	pci_ad[15]	
A13	mem_data[10]		E13	cpu_masterclk		J13	mem_data[26]		N13	pci_ad[1]	
A14	mem_data[20]		E14	mem_data[15]		J14	mem_data[5]		N14	pci_ad[3]	
A15	mem_addr[23]		E15	mem_data[16]		J15	V_{cc} core		N15	pci_ad[4]	
A16	timer_tc_n[0]	2	E16	V_{cc} core		J16	V_{ss}		N16	pci_ad[2]	
B1	uart_rts_n[0]	1	F1	mem_cs_n[0]		K1	ejtag_debugboot		P1	pci_rst_n	
B2	uart_dsr_n[0]	1	F2	mem_cs_n[1]		K2	ejtag_dclk		P2	pci_gnt_n[2]	1
B3	sdram_we_n		F3	mem_oe_n		K3	debug_cpu_i_d_n	1	P3	dma_ready_n[1]	2
B4	sdram_bemask_n[0]		F4	mem_wait_n	1	K4	debug_cpu_ads_n	1	P4	pci_req_n[0]	
B5	sdram_cs_n[1]		F5	V_{cc} IO		K5	V_{cc} IO		P5	pci_ad[27]	
B6	mem_addr[2]	1	F6	V_{ss}		K6	V_{ss}		P6	pci_cbe_n[3]	
B7	mem_addr[6]	1	F7	V_{ss}		K7	V_{ss}		P7	pci_ad[20]	
B8	mem_addr[10]	1	F8	V_{ss}		K8	V_{ss}		P8	pci_ad[16]	

Table 11 RC32334 256-pin PBGA Package Pin-Out (Part 1 of 3)

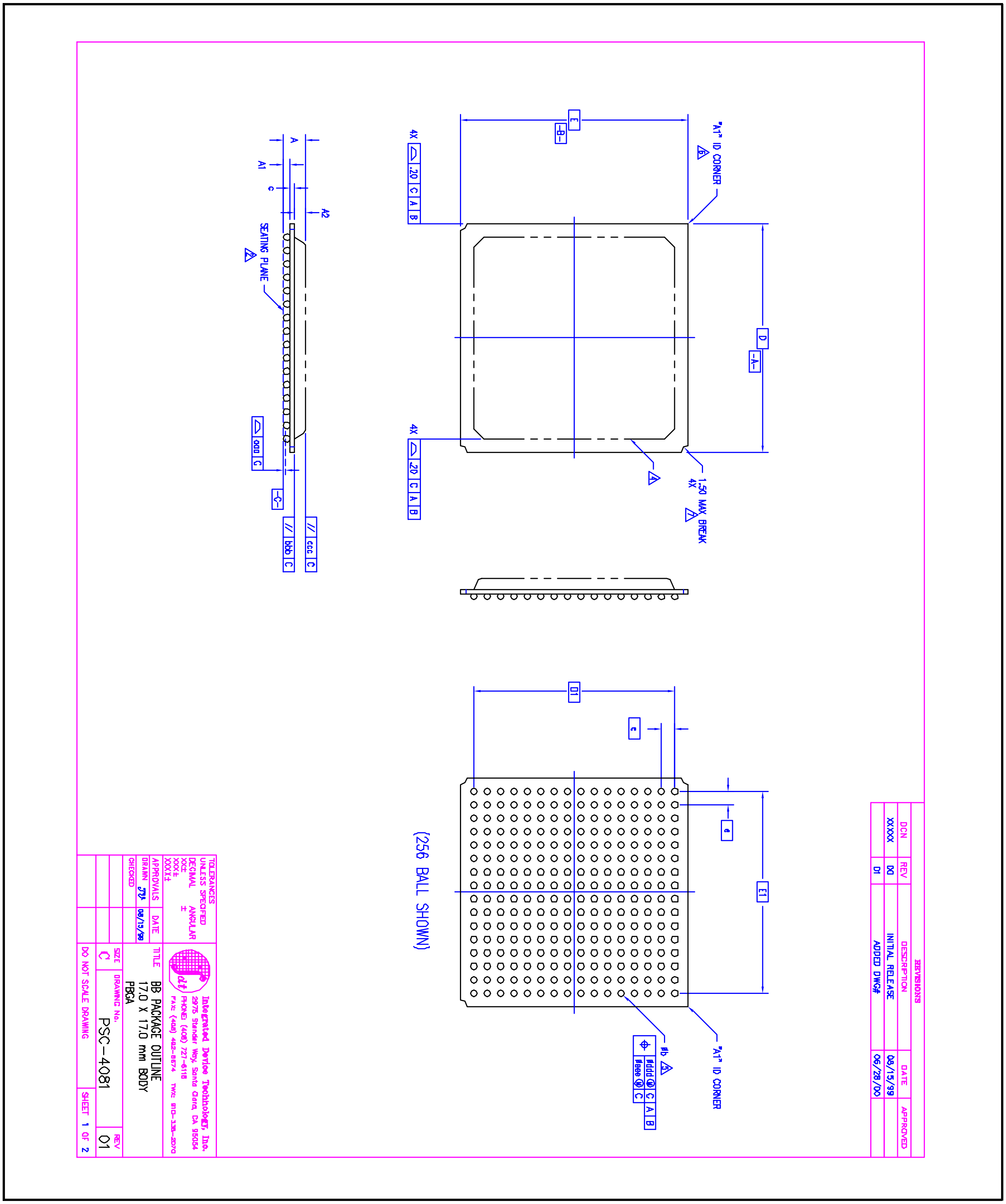
Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
D14	mem_data[17]		H14	$V_{cc}P$		M14	cpu_nmi_n		T14	pci_ad[8]	
D15	mem_data[14]		H15	mem_data[27]		M15	pci_ad[0]		T15	pci_ad[7]	
D16	mem_data[18]		H16	mem_data[4]		M16	mem_data[21]		T16	uart_rx[1]	1

Table 11 RC32334 256-pin PBGA Package Pin-Out (Part 3 of 3)

RC32334 Alternate Signal Functions

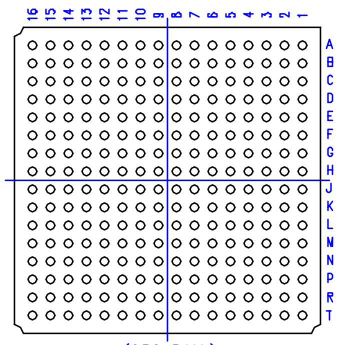
Pin	Alt #1	Alt #2	Pin	Alt #1	Alt #2	Pin	Alt #1	Alt #2
A1	PIO[15]		C3	PIO[13]	C3	H2	PIO[9]	pci_eeprom_sk
A6	sdram_addr[3]		C6	sdram_addr[4]		J1	modebit[6]	
A7	sdram_addr[7]		C7	sdram_addr[9]		J2	modebit[4]	
A8	sdram_addr[11]		C11	sdram_addr[14]		K3	modebit[3]	
A11	sdram_addr[15]		C12	modebit[8]		K4	modebit[5]	
A12	modebit[9]		C13	reset_boot_mode[1]		K13	mem_245_dt_r_n	sdram_245_dt_r_n
A16	PIO[2]	timer_gate_n[0]	D6	sdram_addr[5]		L1	modebit[0]	
B1	PIO[12]		D7	sdram_addr[8]		L3	modebit[1]	
B2	PIO[14]		D11	sdram_addr[13]		L4	modebit[2]	
B6	sdram_addr[2]		D12	modebit[7]		P2	pci_inta_n (satellite)	
B7	sdram_addr[6]		D13	reset_boot_mode[0]		P3	PIO[0]	dma_done_n[1]
B8	sdram_addr[10]		F4	sdram_wait_n		R1	pci_idsel (satellite)	
B11	sdram_addr[16]		G1	PIO[1]	dma_done_n[0]	R3	pci_eeprom_cs (satellite)	PIO[11]
B12	reset_pci_host_mode		G3	PIO[10]	pci_eeprom_mdo	R15	PIO[3]	
C1	PIO[6]		G4	PIO[7]	pci_eeprom_mdi	T2	Unused (satellite)	
C2	PIO[5]		H1	PIO[8]		T16	PIO[4]	

RC32334 Package Drawing — 256-pin PBGA



RC32334 Package Drawing — Page Two

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
XXXXX	00	INITIAL RELEASE	08/15/99	
	01	ADDED DWG#	06/28/00	



(256 BALL)

SYMBOL	DWG# BB256-1 JEDEC VARIATION AAF-1 MIN	NOM	MAX	NOTE
A	–	2.15	3.50	
A1	.30	.40	.50	
A2	–	–	2.50	
D		17.00 BSC		
D1		15.00 BSC		
E		17.00 BSC		
E1		15.00 BSC		
MD		16		3
ME		16		3
N		256		3
e		1.00 BSC		
b	.40	.50	.60	5
c	.10	–	2.50	
aaa	–	–	.20	
bbb	–	–	.25	
ccc	–	–	.35	
ddd	–	–	.30	
eee	–	–	.10	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994

2 SEATING PLANE AND PRIMARY DATUM $\boxed{-C-}$ ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS

3 "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION
"ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION
"N" IS THE NUMBER OF SOLDER BALLS

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5 DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM $\boxed{-C-}$

6 "A1" ID CORNER MUST BE IDENTIFIED. IDENTIFICATION MAY BE BY MEANS OF CHAMFER, METALLIZED OR INK MARK, INDENTATION OR OTHER FEATURE OF THE PACKAGE BODY. MARK MUST BE VISIBLE FROM TOP SURFACE

7 ACTUAL SHAPE OF THIS FEATURE IS OPTIONAL

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9 THIS DRAWING CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-151, VARIATION AAF-1.
EXCEPTIONS:
A1 MIN = .40
b MIN = .50

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DECIMAL ANGULAR
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XXX±
XXXX±

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Product Type	Operating Voltage	Device Type	CPU Frequency	Package	Temp range/ Process

Blank = Commercial Temperature (0° C to +70° C Ambient)
I = Industrial Temperature (-40° C to +85° C Ambient)

BB = 256-pin PBGA
BBG = 256-pin PBGA (Green package)

100 MHz
133MHz
150MHz

334

V = 3.3V ±5%

79RC32 = 32-bit family product

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