Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details

Product Status	Obsolete
Core Processor	MIPS-II
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	150MHz
Co-Processors/DSP	-
RAM Controllers	SDRAM
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	256-BGA
Supplier Device Package	256-PBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/idt79rc32v334-150bbgi

- ♦ **4 DMA Channels**
  - – *4 general purpose DMA, each with endianess swappers and byte lane data alignment*
  - – *Supports scatter/gather, chaining via linked lists of records*
  - – *Supports memory-to-memory, memory-to-I/O, memory-to-PCI, PCI-to-PCI, and I/O-to-I/O transfers*
  - – *Supports unaligned transfers*
  - – *Supports burst transfers*
  - – *Programmable DMA bus transactions burst size (up to 16 bytes)*
- ♦ **PCI Bus Interface**
  - – *32-bit PCI, up to 66 MHz*
  - – *Revision 2.2 compatible*
  - – *Target or master*
  - – *Host or satellite*
  - – *Three slot PCI arbiter*
  - – *Serial EEPROM support, for loading configuration registers*
- ♦ **Off-the-shelf development tools**
- ♦ **JTAG Interface (IEEE Std. 1149.1 compatible)**
- ♦ **256-ball BGA (1.0mm spacing)**
- ♦ **3.3V operation with 5V tolerant I/O**
- ♦ **EJTAG in-circuit emulator interface**

Device Overview

The IDT RC32334 device is an integrated processor based on the RC32300 CPU core. This product incorporates a high-performance, low-cost 32-bit CPU core with functionality common to a large number of embedded applications. The RC32334 integrates these functions to enable the use of low-cost PC commodity market memory and I/O devices, allowing the aggressive price/performance characteristics of the CPU to be realized quickly into low-cost systems.

CPU Execution Core

The RC32334 integrates the RISCore32300, the same CPU core found in the award-winning RC32364 microprocessor.

The RISCore32300 implements the Enhanced MIPS-II ISA. Thus, it is upwardly compatible with applications written for a wide variety of MIPS architecture processors, and it is kernel compatible with the modern operating systems that support IDT's 64-bit RISController product family.

The RISCore32300 was explicitly defined and designed for integrated processor products such as the RC32334. Key attributes of the execution core found within this product include:

- ♦ High-speed, 5-stage scalar pipeline executes to 150MHz. This high performance enables the RC32334 to perform a variety of performance intensive tasks, such as routing, DSP algorithms, etc.
- ♦ 32-bit architecture with enhancements of key capabilities. Thus, the RC32334 can execute existing 32-bit programs, while enabling designers to take advantage of recent advances in CPU architecture.
- ♦ Count leading-zeroes/ones. These instructions are common to a wide variety of tasks, including modem emulation, voice over IP compression and decompression, etc.
- ♦ Cache PREFetch instruction support, including a specialized form intended to help memory coherency. System programmers can allocate and stage the use of memory bandwidth to achieve maximum performance.
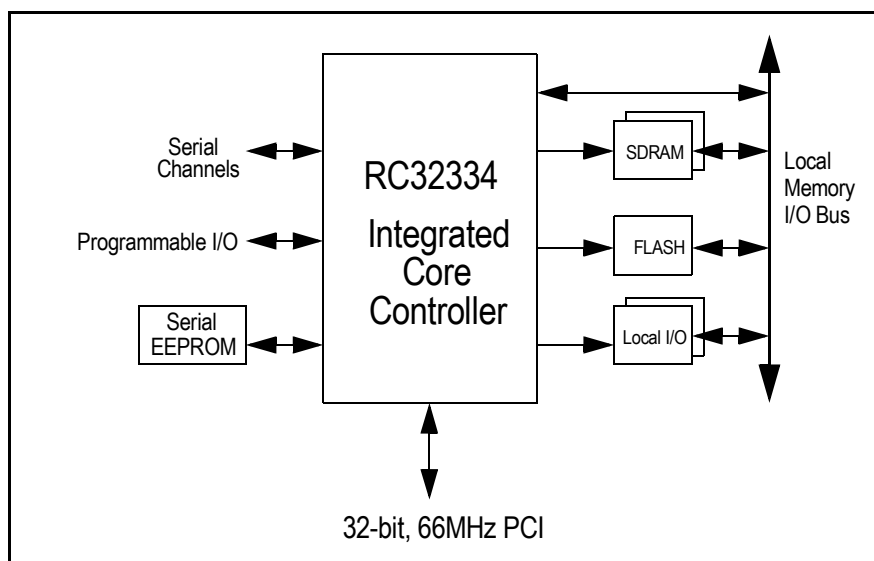- ♦ 8kB of 2-way set associative instruction cache

Figure 2 RC32334 Based System Diagram

- 2KB of 2-way set associative data cache, capable of write-back and write-through operation.
- Cache locking per line to speed real-time systems and critical system functions
- On-chip TLB to enable multi-tasking in modern operating systems
- EJTAG interface to enable sophisticated low-cost in-circuit emulation.

Synchronous-DRAM Interface

The RC32334 integrates a SDRAM controller which provides direct control of system SyncDRAM running at speeds to 75MHz.

Key capabilities of the SDRAM controller include:
- Direct control of 4 banks of SDRAM (up to 2 64-bit wide DIMMs)
- On-chip page comparators optimize access latency.
- Speeds to 75MHz
- Programmable address map.
- Supports 16, 64, 128, 256, or 512Mb SDRAM devices
- Automatic refresh generation driven by on-chip timer
- Support for discrete devices, SODIMM, or DIMM modules.

Thus, systems can take advantage of the full range of commodity memory that is available, enabling system optimization for cost, real-estate, or other attributes.

Local Memory and I/O Controller

The local memory and I/O controller implements direct control of external memory devices, including the boot ROM as well as other memory areas, and also implements direct control of external peripherals.

The local memory controller is highly flexible, allowing a wide range of devices to be directly controlled by the RC32334 processor. For example, a system can be built using an 8-bit boot ROM, 16-bit FLASH cards (possibly on PCMCIA), a 32-bit SRAM or dual-port memory, and a variety of low-cost peripherals.

Key capabilities include:
- Direct control of EPROM, FLASH, RAM, and dual-port memories
- 6 chip-select outputs, supporting up to 64MB per memory space
- Supports mixture of 8-, 16-, and 32-bit wide memory regions
- Flexible timing protocols allow direct control of a wide variety of devices
- Programmable address map for 2 chip selects
- Automatic wait state generation.

PCI Bus Bridge

In order to leverage the wide availability of low-cost peripherals for the PC market as well as to simplify the design of add-in functions, the RC32334 integrates a full 32-bit PCI bus bridge. Key attributes of this bridge include:

- 66 MHz operation
- PCI revision 2.2 compliant
- Programmable address mappings between CPU/Local memory and PCI memory and I/O
- On-chip PCI arbiter
- Extensive buffering allows PCI to operate concurrently with local memory transfers
- Selectable byte-ordering swapper
- 5V tolerant I/O.

On-Chip DMA Controller

To minimize CPU exception handling and maximize the efficiency of system bandwidth, the RC32334 integrates a very sophisticated 4-channel DMA controller on chip.

The RC32334 DMA controller is capable of:
- Chaining and scatter/gather support through the use of a flexible, linked list of DMA transaction descriptors
- Capable of memory<->memory, memory<->I/O, and PCI<->memory DMA
- Unaligned transfer support
- Byte, halfword, word, quadword DMA support.

On-Chip Peripherals

The RC32334 also integrates peripherals that are common to a wide variety of embedded systems.
- Dual channel 16550 compatible UARTs, with modem control interface on one channel.
- SPI master mode interface for direct interface to EEPROM, A/D, etc.
- Interrupt Controller to speed interrupt decode and management
- Four 32-bit on-chip Timer/Counters
- Programmable I/O module

Debug Support

To facilitate rapid time to market, the RC32334 provides extensive support for system debug.

First and foremost, this product integrates an EJTAG in-circuit emulation module, allowing a low-cost emulator to interoperate with programs executing on the controller. By using an augmented JTAG interface, the RC32334 is able to reuse the same low-cost emulators developed around the RC32364 CPU.

Secondly, the RC32334 implements additional reporting signals intended to simplify the task of system debugging when using a logic analyzer. This product allows the logic analyzer to differentiate transactions initiated by DMA from those initiated by the CPU and further allows CPU transactions to be sorted into instruction fetches vs. data fetches.

Finally, the RC32334 implements a full boundary scan capability, allowing board manufacturing diagnostics and debug.

Pin Description Table

The following table lists the pins provided on the RC32334. Note that those pin names followed by "_n" are active-low signals. All external pull-ups and pull-downs require 10 kΩ resistor.

Name	Type	Reset State Status	Drive Strength Capability	Description
Local System Interface				
mem_data[31:0]	I/O	Z	High	**Local System Data Bus** Primary data bus for memory. I/O and SDRAM.
mem_addr[25:2]	I/O	[25:10] Z [9:2] L	[25:17] Low [16:2] High	**Memory Address Bus** These signals provide the Memory or DRAM address, during a Memory or DRAM bus transaction. During each word data, the address increments either in linear or sub-block ordering, depending on the transaction type. The table below indicates how the memory write enable signals are used to address discreet memory port width types. (table below) mem_addr[22] Alternate function: reset_boot_mode[1]. mem_addr[21] Alternate function: reset_boot_mode[0]. mem_addr[20] Alternate function: reset_pci_host_mode. mem_addr[19] Alternate function: modebit [9]. mem_addr[18] Alternate function: modebit [8]. mem_addr[17] Alternate function: modebit [7]. mem_addr[16] Alternate function: sdram_addr[16]. mem_addr[15] Alternate function: sdram_addr[15]. mem_addr[14] Alternate function: sdram_addr[14]. mem_addr[13] Alternate function: sdram_addr[13]. mem_addr[11] Alternate function: sdram_addr[11]. mem_addr[10] Alternate function: sdram_addr[10]. mem_addr[9] Alternate function: sdram_addr[9]. mem_addr[8] Alternate function: sdram_addr[8]. mem_addr[7] Alternate function: sdram_addr[7]. mem_addr[6] Alternate function: sdram_addr[6]. mem_addr[5] Alternate function: sdram_addr[5]. mem_addr[4] Alternate function: sdram_addr[4]. mem_addr[3] Alternate function: sdram_addr[3]. mem_addr[2] Alternate function: sdram_addr[2].
mem_cs_n[5:0]	Output	H	Low with internal pull-up	**Memory Chip Select Negated** Recommend external pull-up. Signals that a Memory Bank is actively selected.
mem_oe_n	Output	H	High	**Memory Output Enable Negated** Recommend external pull-up. Signals that a Memory Bank can output its data lines onto the cpu_ad bus.

Table within mem_addr description:

Port Width	Pin Signals mem_we_n[3]	mem_we_n[2]	mem_we_n[1]	mem_we_n[0]
DMA (32-bit)	mem_we_n[3]	mem_we_n[2]	mem_we_n[1]	mem_we_n[0]
32-bit	mem_we_n[3]	mem_we_n[2]	mem_we_n[1]	mem_we_n[0]
16-bit	Byte High Write Enable	mem_addr[1]	Not Used (Driven Low)	Byte Low Write Enable
8-bit	Not Used (Driven High)	mem_addr[1]	mem_addr[0]	Byte Write Enable

Table 1 Pin Description (Part 1 of 7)

Name	Type	Reset State Status	Drive Strength Capability	Description
mem_we_n[3:0]	Output	H	High	**Memory Write Enable Negated Bus** Signals which bytes are to be written during a memory transaction. Bits act as Byte Enable and mem_addr[1:0] signals for 8-bit or 16-bit wide addressing.
mem_wait_n	Input		—	**Memory Wait Negated** Requires external pull-up. SRAM/IOI/IOM modes: Allows external wait-states to be injected during last cycle before data is sampled. DPM (dual-port) mode: Allows dual-port busy signal to restart memory transaction. Alternate function: sdram_wait_n.
mem_245_oe_n	Output	H	Low	**Memory FCT245 Output Enable Negated** Controls output enable to optional FCT245 transceiver bank by asserting during both reads and writes to a memory or I/O bank.
mem_245_dt_r_n	Output	Z	High	**Memory FCT245 Direction Xmit/Rcv Negated** Recommend external pull-up. Alternate function: cpu_dt_r_n. See CPU Core Specific Signals below.
output_clk	Output	cpu_masterclk	High	**Output Clock** Optional clock output.

PCI Interface

Name	Type	Reset State Status	Drive Strength Capability	Description
pci_ad[31:0]	I/O	Z	PCI	**PCI Multiplexed Address/Data Bus** Address driven by Bus Master during initial frame_n assertion, and then the Data is driven by the Bus Master during writes; or the Data is driven by the Bus Slave during reads.
pci_cbe_n[3:0]	I/O	Z	PCI	**PCI Multiplexed Command/Byte Enable Bus** Command (not negated) Bus driven by the Bus Master during the initial frame_n assertion. Byte Enable Negated Bus driven by the Bus Master during the data phase(s).
pci_par	I/O	Z	PCI	**PCI Parity** Even parity of the pci_ad[31:0] bus. Driven by Bus Master during Address and Write Data phases. Driven by the Bus Slave during the Read Data phase.
pci_frame_n	I/O	Z	PCI	**PCI Frame Negated** Driven by the Bus Master. Assertion indicates the beginning of a bus transaction. De-assertion indicates the last datum.
pci_trdy_n	I/O	Z	PCI	**PCI Target Ready Negated** Driven by the Bus Slave to indicate the current datum can complete.
pci_irdy_n	I/O	Z	PCI	**PCI Initiator Ready Negated** Driven by the Bus Master to indicate that the current datum can complete.
pci_stop_n	I/O	Z	PCI	**PCI Stop Negated** Driven by the Bus Slave to terminate the current bus transaction.
pci_idsel_n	Input		—	**PCI Initialization Device Select** Uses pci_req_n[2] pin. See the PCI subsection.
pci_perr_n	I/O	Z	PCI	**PCI Parity Error Negated** Driven by the receiving Bus Agent 2 clocks after the data is received, if a parity error occurs.
pci_serr_n	I/O Open-collector	Z	PCI	**System Error** External pull-up resistor is required. Driven by any agent to indicate an address parity error, data parity during a Special Cycle command, or any other system error.
pci_clk	Input		—	**PCI Clock** Clock for PCI Bus transactions. Uses the rising edge for all timing references.

Table 1 Pin Description (Part 2 of 7)

Name	Type	Reset State Status	Drive Strength Capability	Description
cpu_dt_r_n	Output	Z	—	**CPU Direction Transmit/Receive** This active-low signal controls the DT/R pin of an optional FCT245 transceiver bank. It is asserted during read operations. 1st Alternate function: mem_245_dt_r_n. 2nd Alternate function: sdram_245_dt_r_n.

JTAG Interface Signals

Name	Type	Reset State Status	Drive Strength Capability	Description
jtag_tck	Input		—	**JTAG Test Clock** Requires external pull-down. An input test clock used to shift into or out of the Boundary-Scan register cells. jtag_tck is independent of the system and the processor clock with nominal 50% duty cycle.
jtag_tdi, ejtag_dint_n	Input		—	**JTAG Test Data In** Requires an external pull-up on the board. On the rising edge of jtag_tck, serial input data are shifted into either the Instruction or Data register, depending on the TAP controller state. During Real Mode, this input is used as an interrupt line to stop the debug unit from Real Time mode and return the debug unit back to Run Time Mode (standard JTAG). This pin is also used as the ejtag_dint_n signal in the EJTAG mode.
jtag_tdo, ejtag_tpc	Output	Z	High	**JTAG Test Data Out** The jtag_tdo is serial data shifted out from instruction or data register on the falling edge of jtag_tck. When no data is shifted out, the jtag_tdo is tri-stated. During Real Time Mode, this signal provides a non-sequential program counter at the processor clock or at a division of processor clock. This pin is also used as the ejtag_tpc signal in the EJTAG mode.
jtag_tms	Input		—	**JTAG Test Mode Select** Requires external pull-up. The logic signal received at the jtag_tms input is decoded by the TAP controller to control test operation. jtag_tms is sampled on the rising edge of the jtag_tck.
jtag_trst_n	Input	L	—	**JTAG Test Reset** When neither JTAG nor EJTAG are being used, jtag_trst_n must be driven low (pulled down) or the jtag_tms/ejtag_tms signals must be pulled up and jtag_clk actively clocked.
ejtag_dclk	Output	Z	—	**EJTAG Test Clock** Processor Clock. During Real Time Mode, this signal is used to capture address and data from the ejtag_tpc signal at the processor clock speed or any division of the internal pipeline.
ejtag_pcst[2:0]	I/O	Z	Low	**EJTAG PC Trace Status Information** 111 (STL) Pipe line Stall 110 (JMP) Branch/Jump forms with PC output 101 (BRT) Branch/Jump forms with no PC output 100 (EXP) Exception generated with an exception vector code output 011 (SEQ) Sequential performance 010 (TST) Trace is outputted at pipeline stall time 001 (TSQ) Trace trigger output at performance time 000 (DBM) Run Debug Mode Alternate function: modebit[2:0].
ejtag_debugboot	Input		— Requires external pull-down	**EJTAG DebugBoot** The ejtag_debugboot input is used during reset and forces the CPU core to take a debug exception at the end of the reset sequence instead of a reset exception. This enables the CPU to boot from the ICE probe without having the external memory working. This input signal is level sensitive and is not latched internally. This signal will also set the JtagBrk bit in the JTAG_Control_Register[12].
ejtag_tms	Input		— Requires external pull-up	**EJTAG Test Mode Select** An external pull-up on the board is required. The ejtag_tms is sampled on the rising edge of jtag_tck.

Table 1 Pin Description (Part 6 of 7)

Name	Type	Reset State Status	Drive Strength Capability	Description
Debug Signals				
debug_cpu_dma_n	I/O	Z	Low	**Debug CPU versus DMA Negated** De-assertion high during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction was generated from the CPU. Assertion low during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction was generated from DMA. Alternate function: modebit[6].
debug_cpu_ack_n	I/O	Z	Low	**Debug CPU Acknowledge Negated** Indicates either a data acknowledge to the CPU or DMA. Alternate function: modebit[4].
debug_cpu_ads_n	I/O	Z	Low	**Debug CPU Address/Data Strobe Negated** Assertion indicates that either a CPU or a DMA transaction is beginning and that the mem_data[31:4] bus has the current block address. Alternate function: modebit[5].
debug_cpu_i_d_n	I/O	Z	Low	**Debug CPU Instruction versus Data Negated** Assertion during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction is a CPU or DMA data transaction. De-assertion during debug_cpu_ads_n assertion or debug_cpu_ack_n assertion indicates transaction is a CPU instruction transaction. Alternate function: modebit[3].

Table 1 Pin Description (Part 7 of 7)

Mode Bit Settings to Configure Controller on Reset

The following table lists the mode bit settings to configure the controller on cold reset.

Pin	Mode Bit	Description	Value	Mode Setting
ejtag_pcst[2:0]	2:0 MSB (2)	Clock Multiplier **MasterClock** is multiplied internally to generate PClock	0	Multiply by 2
			1	Multiply by 3
			2	Multiply by 4
			3	Reserved
			4	Reserved
			5	Reserved
			6	Reserved
			7	Reserved
debug_cpu_i_d_n	3	EndBit	0	Little-endian ordering
			1	Big-endian ordering
debug_cpu_ack_n	4	Reserved	0	
debug_cpu_ads_n	5	Reserved	0	
debug_cpu_dma_n	6	TmrIntEn Enables/Disables the timer interrupt on Int*[5]	0	Enables timer interrupt
			1	Disables timer interrupt
mem_addr[17]	7	Reserved for future use	1	

Table 2 Boot-Mode Configuration Settings (Part 1 of 2)

Pin	Mode Bit	Description	Value	Mode Setting
mem_addr[19:18]	9:8 MSB (9)	Boot-Prom Width specifies the memory port width of the memory space which contains the boot prom.	00	8 bits
			01	16 bits
			10	32 bits
			11	Reserved

Table 2 Boot-Mode Configuration Settings (Part 2 of 2)

reset_boot_mode Settings

By using the non-boot mode cold reset initialization mode the user can change the internal register addresses from base 1800_0000 to base 1900_0000, as required. The RC32334 cold reset-boot mode initialization setting values and mode descriptions are listed below.

Pin	Reset Boot Mode	Description	Value	Mode Settings
mem_addr[22:21]	1:0 MSB (1)	Tri-state memory bus and EEPROM bus during cold reset_n assertion	11	Tri-state_bus_mode
		Reserved	10	
		PCI-boot mode (pci_host_mode must be in satellite mode) RC32334 will reset either from a cold reset or from a PCI reset. Boot code is provided via PCI.	01	PCI_boot_mode
		Standard-boot mode Boot from the RC32334's memory controller (typical system).	00	standard_boot_mode

Table 3 RC32334 reset_boot_mode Initialization Settings

pci_host_mode Settings

During cold reset initialization, the RC32334's PCI interface can be set to the Satellite or Host mode settings. When set to the Host mode, the CPU must configure the RC32334's PCI configuration registers, including the read-only registers. If the RC32334's PCI is in the PCI-boot mode Satellite mode, read-only configuration registers are loaded by the serial EEPROM.

Pin	Reset Boot Mode	Description	Value	Mode Settings
mem_addr[20]	PCI host mode	PCI is in satellite mode	1	PCI_satellite
		PCI is in host mode (typical system)	0	PCI_host

Table 4 RC32334 pci_host_mode Initialization Settings

Logic Diagram — RC32334

CPU Core signals
- cpu_masterclk
- cpu_coldreset_n
- cpu_nmi_n
- cpu_int_n[5:4],[2:0]
- cpu_dt_r_n

PCI Interface
- pci_cbe_n[3:0]
- pci_ad[31:0]
- pci_par
- pci_frame_n
- pci_trdy_n
- pci_irdy_n
- pci_stop_n
- pci_idsel
- pci_perr_n
- pci_serr_n
- pci_clk
- pci_rst_n
- pci_devsel_n
- pci_req_n[2:0]
- pci_gnt_n[2:0]
- pci_inta_n
- pci_lock_n
- pci_eeprom_mdi
- pci_eeprom_mdo
- pci_eeprom_cs
- pci_eeprom_sk

JTAG Interface
- jtag_tck
- jtag_tms
- jtag_tdi
- jtag_tdo
- jtag_trst_n

Debug
- debug_cpu_dma_n
- debug_cpu_ack_n
- debug_cpu_i_d_n
- debug_cpu_ads_n

Power/Ground
- Gnd
- V_{CC} to I/O
- V_{CC} to core
- $V_{CC}P$
- $V_{SS}P$

V_{SS}
V_{CC} I/O
V_{CC} core

RC32334 Logic Symbol

Local System Interface
- mem_addr[25:2]
- mem_data[31:0]
- mem_cs_n[5:0]
- mem_oe_n
- mem_we_n[3:0]
- mem_wait_n
- mem_245_oe_n
- mem_245_dt_r_n
- output_clk

SPI Interface
- spi_mosi
- spi_miso
- spi_ss_n
- spi_sck

SDRAM Signals
- sdram_addr[16:13]
- sdram_addr[12]
- sdram_addr[11:2]
- sdram_ras_n
- sdram_cas_n
- sdram_we_n
- sdram_cke
- sdram_cs_n[3:0]
- sdram_bemask_n[3:0]
- sdram_245_oe_n
- sdram_245_dt_r_n
- sdram_s_n_[1:0]

DMA Interface
- dma_ready_n[1:0]

Timer
- timer_tc_n[0]

UART
- uart_rx[1:0]
- uart_tx[1:0]
- uart_cts_n[0]
- uart_rts_n[0]
- uart_dtr_n[0]
- uart_dsr_n[0]

EJTAG
- ejtag_dclk
- ejtag_pcst[2:0]
- ejtag_tms
- ejtag_debugboot
- ejtag_tpc

PIO Interface
- pio[15:0]

Clock Parameters — RC32334

(Ta = 0°C to +70°C Commercial, Ta = -40°C to +85°C Industrial, V_{cc} I/O = +3.3V±5%, V_{cc} Core = +3.3V±5%)

Parameter	Symbol	Test Conditions	RC32334 100MHz		RC32334 133MHz		RC32334 150MHz		Units
			Min	Max	Min	Max	Min	Max	
cpu_masterclock HIGH	t_{MCHIGH}	Transition ≤ 2ns	8	—	6.75	—	6	—	ns
cpu_masterclock LOW	t_{MCLOW}	Transition ≤ 2ns	8	—	6.75	—	6	—	ns
cpu_masterclock period[1]	t_{MCP}	—	20	66.6	15	66.6	13.33	66.6	ns
cpu_masterclock Rise & Fall Time[2]	t_{MCRise}, t_{MCFall}	—	—	3	—	3	—	3	ns
cpu_masterclock Jitter	t_{JITTER}	—	—	± 250	—	± 250	—	± 200	ps
pci_clk Rise & Fall Time	t_{PCRise}, t_{PCFall}	PCI 2.2	—	1.6	—	1.6	—	1.6	ns
pci_clk Period[1]	t_{PCP}		15	—	15	—	15	—	ns
jtag_tck Rise & Fall Time	t_{JCRise}, t_{JCFall}	—	—	5	—	5	—	5	ns
ejtag_dck period	t_{DCK}, t_{11}		10	—	10	—	10	—	ns
jtag_tck clock period	t_{TCK}, t_3		100	—	100	—	100	—	ns
ejtag_dclk High, Low Time	$t_{DCK High}$, t_9 $t_{DCK Low}$, t_{10}		4	—	4	—	4	—	ns
ejtag_dclk Rise, Fall Time	$t_{DCK Rise}$, t_9 $t_{DCK Fall}$, t_{10}		—	1	—	1	—	1	ns
output_clk[3]	Tdo21		N/A	N/A	N/A	N/A	N/A	N/A	—
cpu_coldreset_n Asserted during power-up		power-on sequence	120	—	120	—	120	—	ms
cpu_coldreset_n Rise Time	t_{CRRise}		—	5	—	5	—	5	ns

Table 5 Clock Parameters - RC32334

[1.] cpu_masterclock frequency should never be below pci_clk frequency if PCI interface is used.

[2.] Rise and fall times are measured between 10% and 90%

[3.] **Output_clk should not be used in a system. Only the cpu_masterclock or its derivative must be used to drive all the subsystems with designs based on the RC32334 device. Refer to the RC3233x Device Errata for more information.**

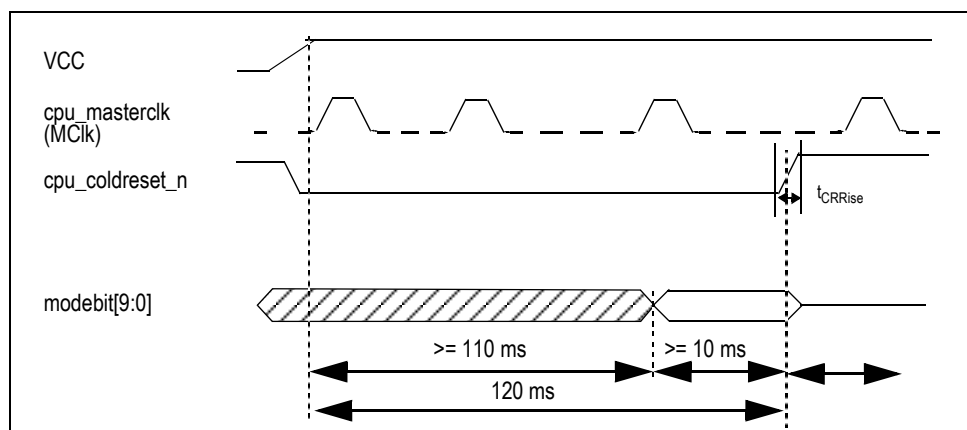## Reset Specification

Figure 3 Mode Configuration Interface Cold Reset Sequence

Power Ramp-up

There is no special requirement for how fast Vcc and VccP ramp up to 3.3V. However, all timing references are based on Vcc and VccP stabilized at 3.3V -5%.

AC Timing Characteristics — RC32334

(Ta = 0°C to +70°C Commercial, Ta = -40°C to +85°C Industrial, V_{cc} I/O = +3.3V±5%, V_{cc} Core = +3.3V±5%)

Signal	Symbol	Reference Edge	RC32334[1] 100MHz		RC32334[1] 133MHz		RC32334[1] 150MHz		Unit	User Manual Timing Diagram Reference
			Min	Max	Min	Max	Min	Max		
Local System Interface										
mem_data[31:0] (data phase)	Tsu2	cpu_masterclk rising	6	—	5	—	4.8	—	ns	
mem_data[31:0] (data phase)	Thld2	cpu_masterclk rising	1.5	—	1.5	—	1.5	—	ns	
cpu_dt_r_n	Tdo3	cpu_masterclk rising	—	15	—	12	—	10	ns	Chapter 9, Figures 9.2 and 9.3
mem_data[31:0]	Tdo4	cpu_masterclk rising	—	12	—	10	—	9.3	ns	
mem_data[31:0] output hold time	Tdoh1	cpu_masterclk rising	1	—	1	—	1	—	ns	
mem_data[31:0] (tristate disable time)	Tdz	cpu_masterclk rising	—	12[2]	—	10[2]	—	9.3[2]	ns	
mem_data[31:0] (tristate to data time)	Tzd	cpu_masterclk rising	—	12[2]	—	10[2]	—	9.3[2]	ns	
mem_wait_n	Tsu6	cpu_masterclk rising	9	—	7	—	6	—	ns	
mem_wait_n	Thld8	cpu_masterclk rising	1	—	1	—	1	—	ns	Chapter 10, Figures 10.6 through 10.8
mem_addr[25:2]	Tdo5	cpu_masterclk rising	—	12	—	9	—	8	ns	
mem_cs_n[5:0]	Tdo6	cpu_masterclk rising	—	12	—	9	—	8	ns	
mem_oe_n, mem_245_oe_n	Tdo7	cpu_masterclk rising	—	12	—	9	—	8	ns	
mem_we_n[3:0]	Tdo7a	cpu_masterclk rising	—	15	—	12	—	10	ns	
mem_245_dt_r_n	Tdo8	cpu_masterclk rising	—	15	—	12	—	10	ns	
mem_addr[25:2] mem_cs_n[5:0] mem_oe_n, mem_we_n[3:0], mem_245_dt_r_n, mem_245_oe_n	Tdoh3	cpu_masterclk rising	1.5	—	1.5	—	1.5	—	ns	
PCI										
pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n, pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n, pci_serr_n, pci_devsel_n, pci_lock_n[3]	Tsu	pci_clk rising	3	—	3	—	3	—	ns	
pci_idsel, pci_req_n[2], pci_req_n[1], pci_req_n[0], pci_gnt_n[0], pci_inta_n	Tsu	pci_clk rising	5	—	5	—	5	—	ns	
pci_gnt_n[0]	Tsu	pci_clk rising	5	—	5	—	5	—	ns	
pci_ad[31:0], pci_cbe_n[3:0], pci_par, pci_frame_n, pci_trdy_n, pci_irdy_n, pci_stop_n, pci_perr_n, pci_serr_n, pci_rst_n, pci_devsel_n, pci_lock_n[3]	Thld	pci_clk rising	0	—	0	—	0	—	ns	Per PCI 2.2
pci_idsel, pci_req_n[2], pci_req_n[1], pci_req_n[0], pci_gnt_n[0], pci_inta_n	Thld	pci_clk rising	0	—	0	—	0	—	ns	
pci_eeprom_mdi	Tsu	pci_clk rising, pci_eeprom_sk falling	15	—	12	—	10	—	ns	

Table 6 AC Timing Characteristics - RC32334 (Part 1 of 4)

Signal	Symbol	Reference Edge	RC32334[1] 100MHz		RC32334[1] 133MHz		RC32334[1] 150MHz		Unit	User Manual Timing Diagram Reference
			Min	Max	Min	Max	Min	Max		
EJTAG Interface										
ejtag_tms, ejtag_debugboot	t_5	jtag_tclk rising	4	—	4	—	4	—	ns	See Figure 4 below.
ejtag_tms, ejtag_debugboot	t_6	jtag_clk rising	2	—	2	—	2	—	ns	
jtag_tdo Output Delay Time	t_{TDODO}, t_4	jtag_tck falling	—	6	—	6	—	6	ns	
jtag_tdi Input Setup Time	t_{TDIS}, t_5	jtag_tck rising	4	—	4	—	4	—	ns	
jtag_tdi Input Hold Time	t_{TDIH}, t_6	jtag_tck rising	2	—	2	—	2	—	ns	
jtag_trst_n Low Time	$t_{TRSTLow}$, t_{12}	—	100	—	100	—	100	—	ns	
jtag_trst_n Removal Time	t_{TRSTR}, t_{13}	jtag_tck rising	3	—	3	—	3	—	ns	
ejtag_tpc Output Delay Time	t_{TPCDO}, t_8	ejtag_dclk rising	-1	3	-1	3	-1	3	ns	
ejtag_pcst Output Delay Time	t_{PCSTDO}, t_7	ejtag_dclk rising	-1	3	-1	3	-1	3	ns	

Table 6 AC Timing Characteristics - RC32334 (Part 4 of 4)

[1]. At all pipeline frequencies.

[2]. Guaranteed by design.

[3]. pci_rst_n is tested per PCI 2.2 as an asynchronous signal.

Standard EJTAG Timing — RC32334

Figure 4 represents the timing diagram for the EJTAG interface signals.

The standard JTAG connector is a 10-pin connector providing 5 signals and 5 ground pins. For Standard EJTAG, a 24-pin connector has been chosen providing 12 signals and 12 ground pins. This guarantees elimination of noise problems by incorporating signal-ground type arrangement. Refer to the RC32334 User Reference Manual for connector pinout and mechanical specifications.
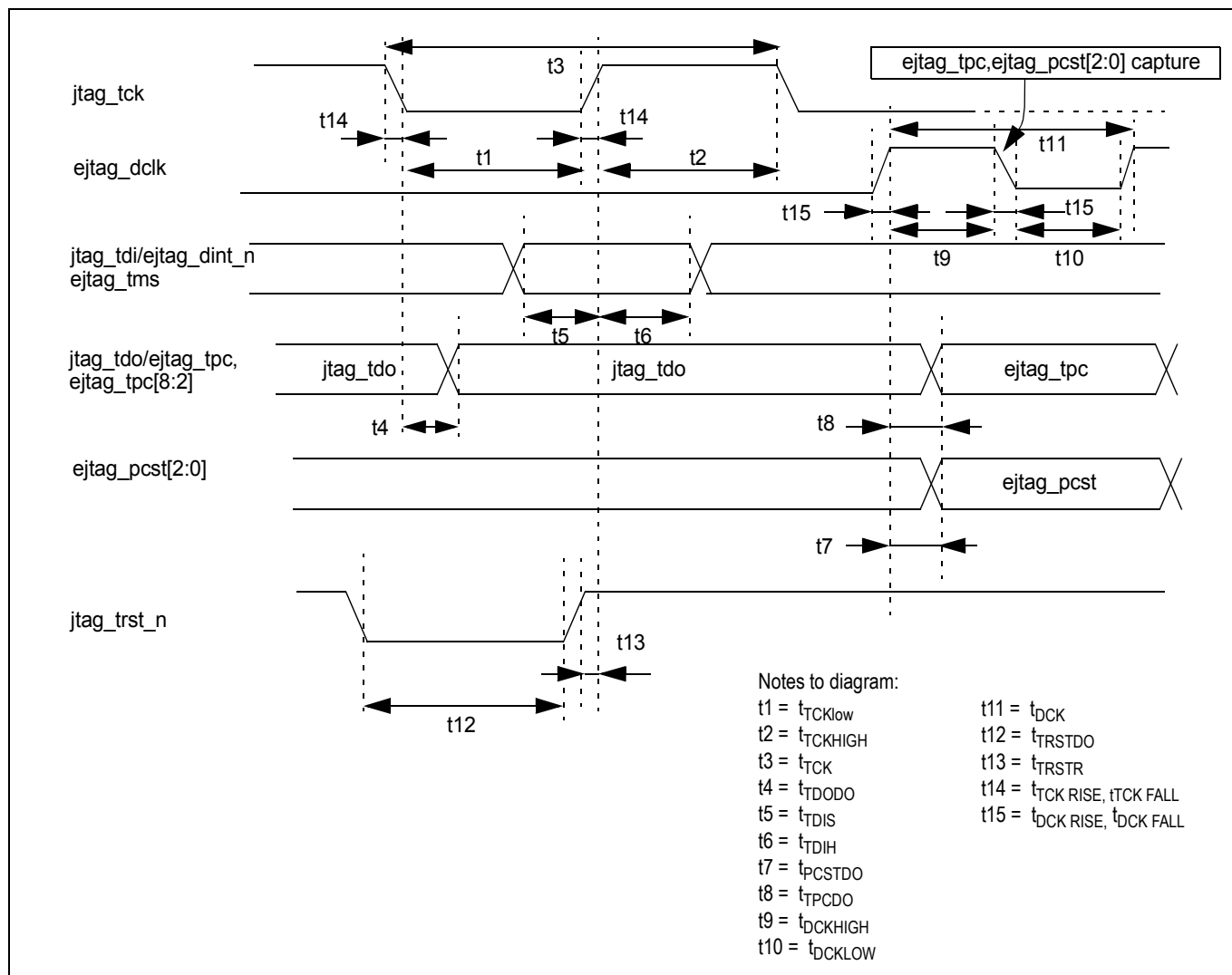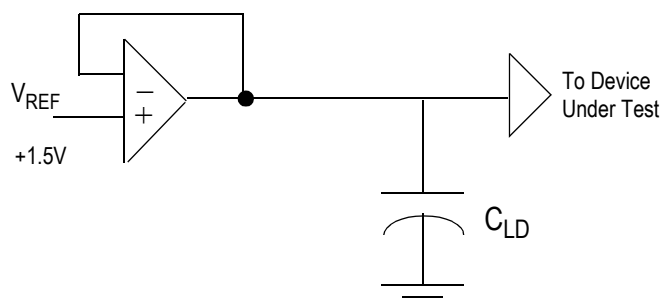
Notes to diagram:

$t1 = t_{TCKlow}$

$t2 = t_{TCKHIGH}$

$t3 = t_{TCK}$

$t4 = t_{TDODO}$

$t5 = t_{TDIS}$

$t6 = t_{TDIH}$

$t7 = t_{PCSTDO}$

$t8 = t_{TPCDO}$

$t9 = t_{DCKHIGH}$

$t10 = t_{DCKLOW}$

$t11 = t_{DCK}$

$t12 = t_{TRSTDO}$

$t13 = t_{TRSTR}$

$t14 = t_{TCK\ RISE,\ tTCK\ FALL}$

$t15 = t_{DCK\ RISE,}\ t_{DCK\ FALL}$

Figure 4 Standard EJTAG Timing

Output Loading for AC Testing

Signal	Cld
All High Drive Signals	50 pF
All Low Drive Signals	25 pF

Figure 5 Output Loading for AC Testing

Note: PCI pins have been correlated to PCI 2.2.

Recommended Operation Temperature and Supply Voltage

Grade	Temperature	Gnd	$V_{cc}IO$	$V_{cc}Core$	$V_{cc}P$
Commercial	0°C to +70°C (Ambient)	0V	3.3V±5%	3.3V±5%	3.3V±5%
Industrial	-40°C to +85°C (Ambient)	0V	3.3V±5%	3.3V±5%	3.3V±5%

Table 7 Temperature and Voltage

DC Electrical Characteristics — RC32334

Commercial Temperature Range—RC32334

(Ta = 0°C to +70°C Commercial, Ta = -40°C to +85°C Industrial, V_{cc} I/O = +3.3V±5%, V_{cc} Core = +3.3V±5%)

	Parameter	RC32334[1] Minimum	RC32334[1] Maximum	Pin Numbers	Conditions
Input Pads	V_{IL}	—	0.8V	B14, E13, F4, K1, L2, M1, M3, M4, M14, N1-N3, P14, R2, R16	—
	V_{IH}	2.0V	—		—
LOW Drive Output Pads	V_{OL}	—	0.4V	A1, A12, A15, A16, B1, B2, B12, B15, C1-C3, C12, C13, C14, D12, D13, E1- E4, F1, F2, G1-G4, H1, H2, J1, J2, K2-K4, L1, L3, L4, P3, P14, R2, R15, R16, T16	$|I_{OUT}|$ = 6mA
	V_{OH}	V_{cc} - 0.4V	—		$|I_{OUT}|$ = 8mA
	V_{IL}	—	0.8V		—
	V_{IH}	2.0V	—		—
HIGH Drive Output Pads	V_{OL}	—	0.4V	A2-A4, A6-A11, A13, A14, B3, B4, B6-B11, B13, B16, C4, C6-C8, C10, C11, C15, C16, D1-D4, D6, D7, D10, D11, D14-D16, E14, E15, F3, F13-F16, G13-G16, H15, H16, J13, J14, K5, K13, K14, K16, L13-L16, M2, M13, M16, P2, P4, R1, R3, R4	$|I_{OUT}|$ = 7mA
	V_{OH}	V_{cc} - 0.4V	—		$|I_{OUT}|$ = 16mA
	V_{IL}	—	0.8V		—
	V_{IH}	2.0V	—		—
PCI Drive Input Pads	V_{IL}	—	—	P1, R1, R10, T2, T3	Per PCI 2.2
	V_{IH}	—	—		

Table 8 DC Electrical Characteristics - RC32334 (Part 1 of 2)

Power Curves

The following two graphs contain the simulated power curves that show power consumption at various bus frequencies.

Note: Only pipeline frequencies that are integer multiples (2x, 3x, 4x) of bus frequencies are supported.
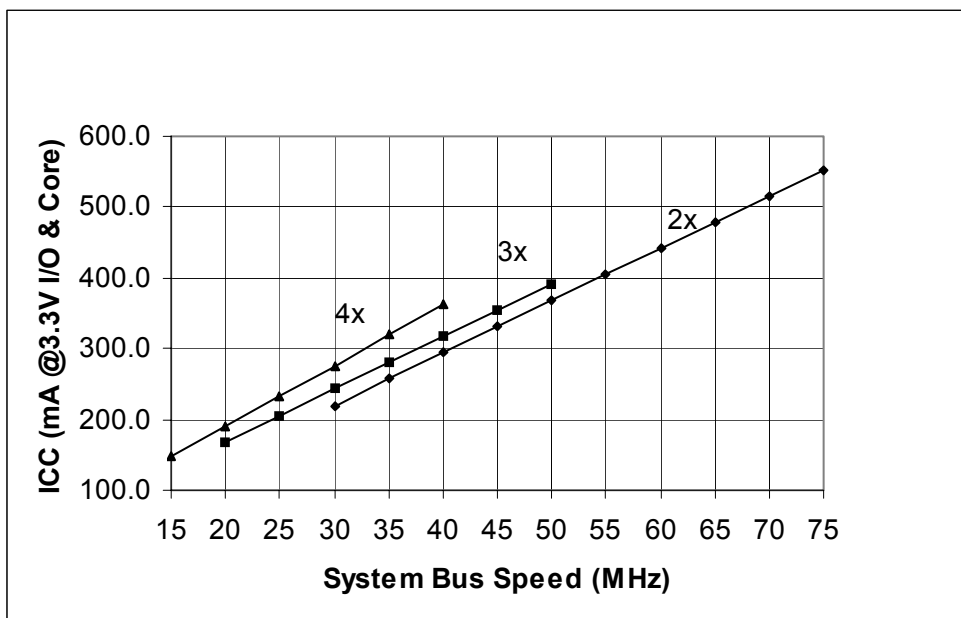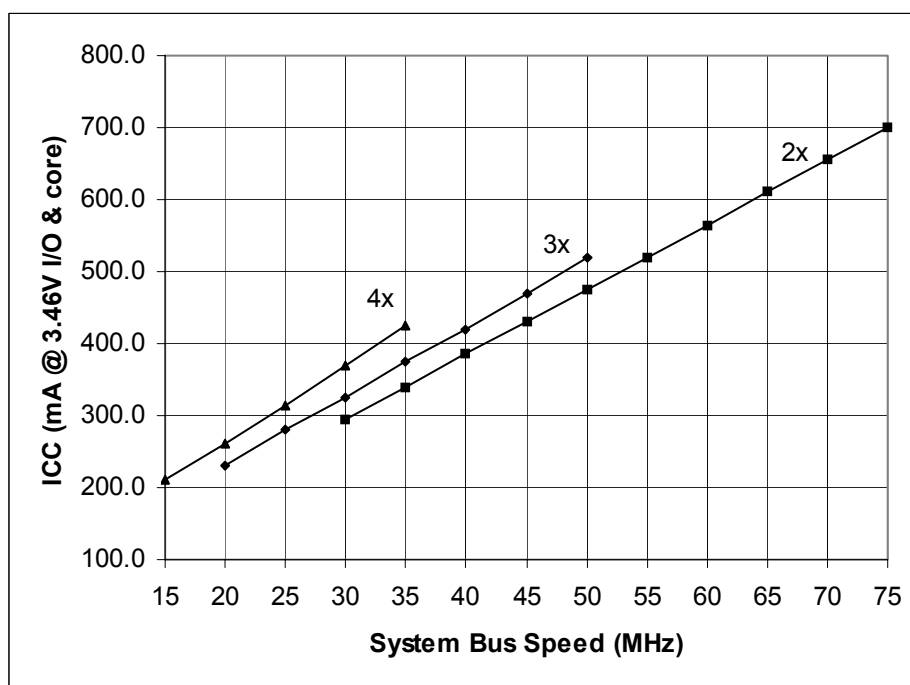

Figure 6 Typical Power Usage - RC32334



Figure 7 Maximum Power Usage - RC32334

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
B9	sdram_addr_12		F9	V_{ss}		K9	V_{ss}		P9	pci_cbe_n[2]	
B10	sdram_bemask_n[3]		F10	V_{ss}		K10	V_{ss}		P10	pci_devsel_n	
B11	mem_addr[16]	1	F11	V_{ss}		K11	V_{ss}		P11	pci_serr_n	
B12	mem_addr[20]	1	F12	V_{cc} IO		K12	V_{cc} IO		P12	pci_ad[14]	
B13	mem_data[11]		F13	mem_data[1]		K13	cpu_dt_r_n	2	P13	pci_ad[11]	
B14	cpu_coldreset_n		F14	mem_data[30]		K14	mem_data[6]		P14	cpu_int_n[5]	
B15	mem_addr[25]		F15	mem_data[31]		K15	mem_data[24]		P15	pci_ad[6]	
B16	mem_data[12]		F16	mem_data[0]		K16	mem_data[25]		P16	pci_ad[5]	
C1	uart_rx[0]	1	G1	dma_ready_n[0]	2	L1	ejtag_pcst[0]		R1	pci_req_n[2]	1
C2	uart_tx[0]	1	G2	mem_245_oe_n		L2	jtag_trst_n		R2	cpu_int_n[2]	
C3	uart_dtr_n[0]	1	G3	spi_mosi	2	L3	ejtag_pcst[1]	1	R3	pci_gnt_n[1]	2
C4	sdram_cs_n[0]		G4	spi_miso	2	L4	ejtag_pcst[2]	1	R4	pci_gnt_n[0]	
C5	sdram_s_n[0]		G5	V_{cc} IO		L5	V_{cc} IO		R5	pci_ad[29]	
C6	mem_addr[4]	1	G6	V_{ss}		L6	V_{ss}		R6	pci_ad[25]	
C7	mem_addr[9]	1	G7	V_{ss}		L7	V_{ss}		R7	pci_ad[22]	
C8	output_clk		G8	V_{ss}		L8	V_{ss}		R8	pci_ad[18]	
C9	mem_addr[12]		G9	V_{ss}		L9	V_{ss}		R9	pci_irdy_n	
C10	sdram_cs_n[3]		G10	V_{ss}		L10	V_{ss}		R10	pci_lock_n	
C11	mem_addr[14]	1	G11	V_{ss}		L11	V_{ss}		R11	pci_cbe_n[1]	
C12	mem_addr[18]	1	G12	V_{cc} IO		L12	V_{cc} IO		R12	pci_ad[12]	
C13	mem_addr[22]	1	G13	mem_data[3]		L13	mem_data[7]		R13	pci_ad[10]	
C14	mem_addr[24]		G14	mem_data[28]		L14	mem_data[8]		R14	pci_cbe_n[0]	
C15	mem_data[19]		G15	mem_data[29]		L15	mem_data[22]		R15	uart_tx[1]	1
C16	mem_data[13]		G16	mem_data[2]		L16	mem_data[23]		R16	cpu_int_n[4]	
D1	mem_we_n[1]		H1	spi_ss_n	1	M1	jtag_tms		T1	V_{ss}	
D2	mem_we_n[3]		H2	spi_sck	2	M2	jtag_tdo		T2	pci_req_n[1]	1
D3	mem_we_n[2]		H3	V_{cc} IO		M3	ejtag_tms		T3	pci_clk	
D4	mem_we_n[0]		H4	V_{cc} core		M4	jtag_tck		T4	pci_ad[31]	
D5	sdram_s_n[1]		H5	V_{cc} IO		M5	V_{cc} IO		T5	pci_ad[28]	
D6	mem_addr[5]	1	H6	V_{ss}		M6	V_{cc} IO		T6	pci_ad[24]	
D7	mem_addr[8]	1	H7	V_{ss}		M7	V_{cc} IO		T7	pci_ad[21]	
D8	V_{ss}		H8	V_{ss}		M8	V_{cc} IO		T8	pci_ad[17]	
D9	V_{cc} core		H9	V_{ss}		M9	V_{cc} IO		T9	pci_frame_n	
D10	sdram_cs_n[2]		H10	V_{ss}		M10	V_{cc} IO		T10	pci_stop_n	
D11	mem_addr[13]	1	H11	V_{ss}		M11	V_{cc} IO		T11	pci_par	
D12	mem_addr[17]	1	H12	V_{cc} IO		M12	V_{cc} IO		T12	pci_ad[13]	
D13	mem_addr[21]	1	H13	V_{ss}P		M13	mem_data[9]		T13	pci_ad[9]	

Table 11 RC32334 256-pin PBGA Package Pin-Out (Part 2 of 3)

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
D14	mem_data[17]		H14	$V_{cc}P$		M14	cpu_nmi_n		T14	pci_ad[8]	
D15	mem_data[14]		H15	mem_data[27]		M15	pci_ad[0]		T15	pci_ad[7]	
D16	mem_data[18]		H16	mem_data[4]		M16	mem_data[21]		T16	uart_rx[1]	1

Table 11 RC32334 256-pin PBGA Package Pin-Out (Part 3 of 3)

Pin Layout
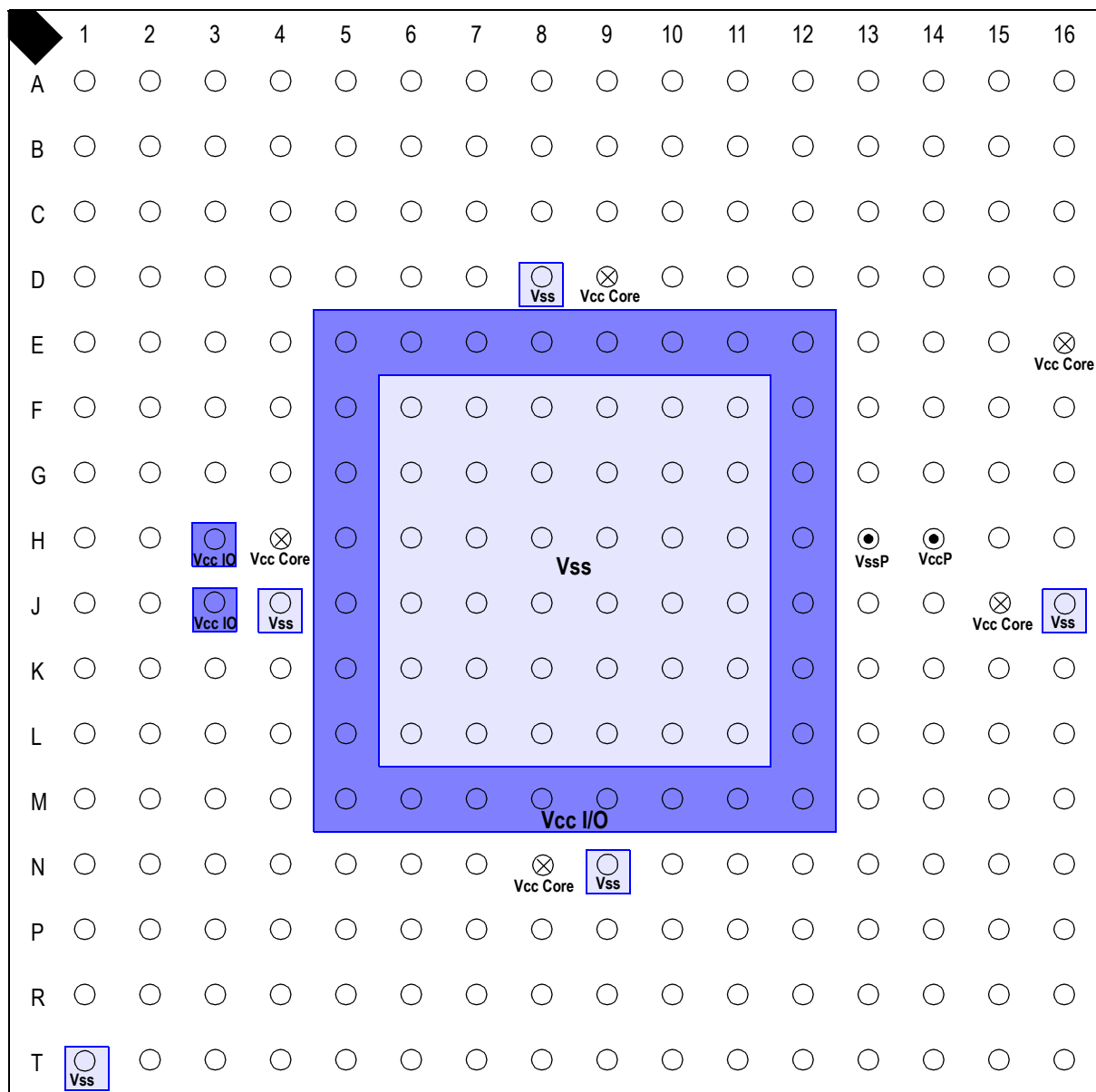
Figure 8 RC32334 Chip — Top View

RC32334 Alternate Signal Functions

Pin	Alt #1	Alt #2	Pin	Alt #1	Alt #2	Pin	Alt #1	Alt #2
A1	PIO[15]		C3	PIO[13]	C3	H2	PIO[9]	pci_eeprom_sk
A6	sdram_addr[3]		C6	sdram_addr[4]		J1	modebit[6]	
A7	sdram_addr[7]		C7	sdram_addr[9]		J2	modebit[4]	
A8	sdram_addr[11]		C11	sdram_addr[14]		K3	modebit[3]	
A11	sdram_addr[15]		C12	modebit[8]		K4	modebit[5]	
A12	modebit[9]		C13	reset_boot_mode[1]		K13	mem_245_dt_r_n	sdram_245_dt_r_n
A16	PIO[2]	timer_gate_n[0]	D6	sdram_addr[5]		L1	modebit[0]	
B1	PIO[12]		D7	sdram_addr[8]		L3	modebit[1]	
B2	PIO[14]		D11	sdram_addr[13]		L4	modebit[2]	
B6	sdram_addr[2]		D12	modebit[7]		P2	pci_inta_n (satellite)	
B7	sdram_addr[6]		D13	reset_boot_mode[0]		P3	PIO[0]	dma_done_n[1]
B8	sdram_addr[10]		F4	sdram_wait_n		R1	pci_idsel (satellite)	
B11	sdram_addr[16]		G1	PIO[1]	dma_done_n[0]	R3	pci_eeprom_cs (satellite)	PIO[11]
B12	reset_pci_host_mode		G3	PIO[10]	pci_eeprom_mdo	R15	PIO[3]	
C1	PIO[6]		G4	PIO[7]	pci_eeprom_mdi	T2	Unused (satellite)	
C2	PIO[5]		H1	PIO[8]		T16	PIO[4]	

RC32334 Package Drawing — 256-pin PBGA
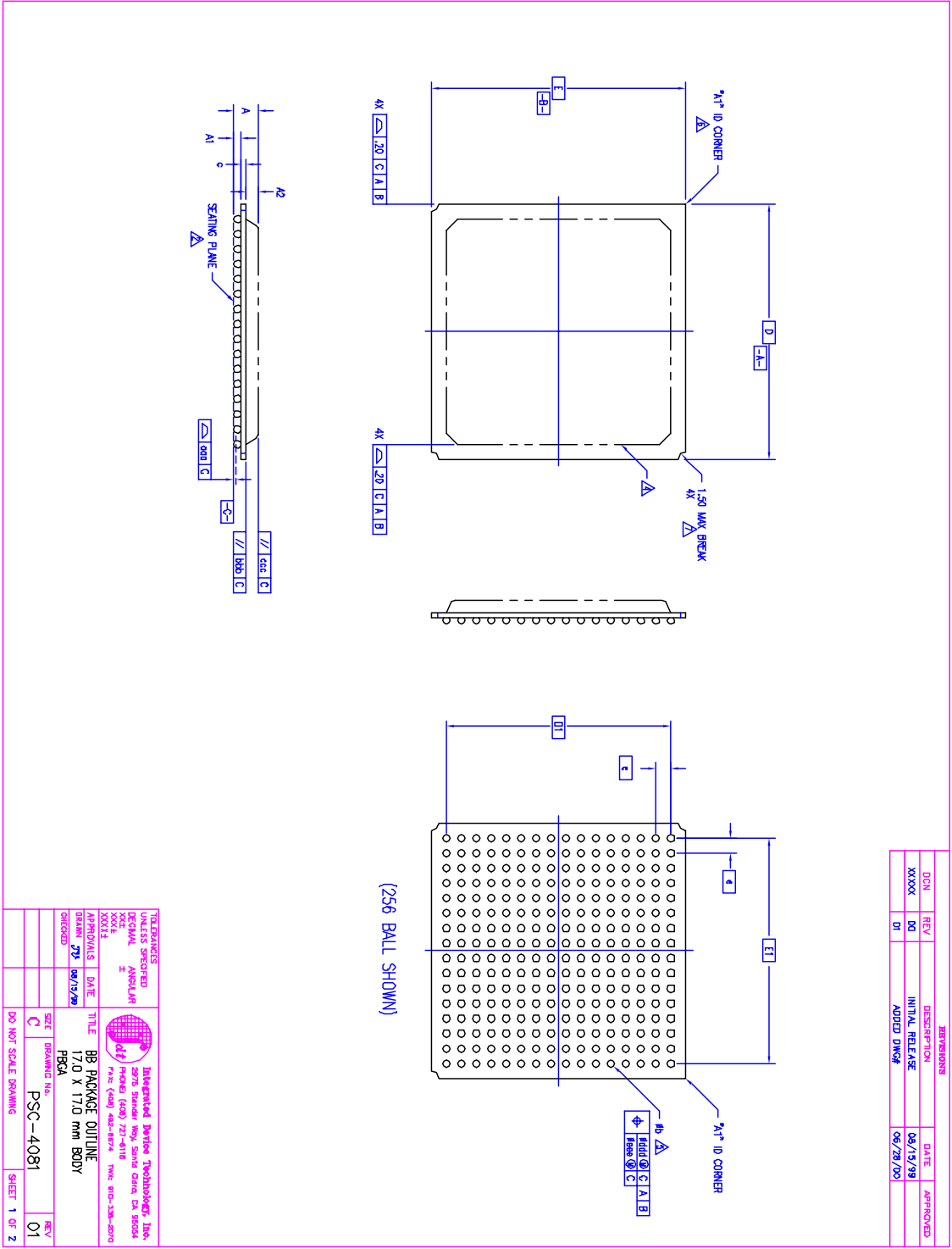
Ordering Information

79RCXX	V	DDD	SSS	PP	
Product Type	Operating Voltage	Device Type	CPU Frequency	Package	Temp range/ Process

Blank = Commercial Temperature (0° C to +70° C Ambient)
I = Industrial Temperature   (-40° C to +85° C Ambient)

BB = 256-pin PBGA
BBG = 256-pin PBGA (Green package)

100 MHz
133MHz
150MHz

334

V = 3.3V ±5%

79RC32 =   32-bit family product

Valid Combinations

79RC32V334 - 100BB, 133BB, 150BB	Commercial
79RC32V334 - 100BBG, 133BBG, 150BBG	Commercial Green
79RC32V334 - 100BBI, 133BBI, 150BBI	Industrial
79RC32V334 - 100BBGI, 133BBGI, 150BBGI	Industrial Green