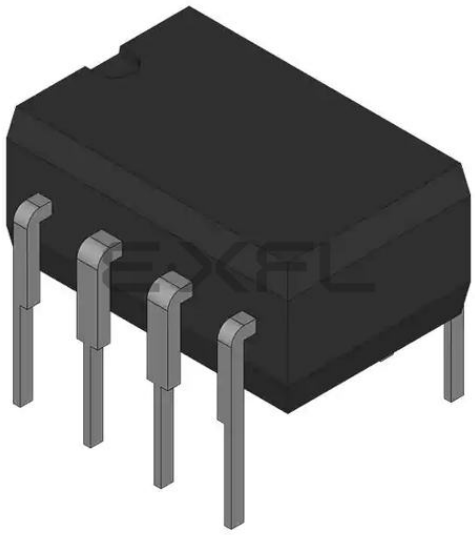
Atmel - ATTINY15L-1PI Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	AVR
Core Size	8-Bit
Speed	1.6MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	6
Program Memory Size	1KB (512 x 16)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	-
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	8-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/atmel/attiny15l-1pi

Pin Descriptions

VCC

Supply voltage pin.

GND

Ground pin.

Port B (PB5..PB0)

Port B is a 6-bit I/O port. PB4..0 are I/O pins that can provide internal pull-ups (selected for each bit). PB5 is input or open-drain output. The use of pin PB5 is defined by a fuse and the special function associated with this pin is External Reset. The port pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also accommodates analog I/O pins. The Port B pins with alternate functions are shown in Table 1.

Table 1. Port B Alternate Functions

Port Pin	Alternate Function
PB0	MOSI (Data Input Line for Memory Downloading) AREF (ADC Voltage Reference) AIN0 (Analog Comparator Positive Input)
PB1	MISO (Data Output Line for Memory Downloading) OC1A (Timer/Counter PWM Output) AIN1 (Analog Comparator Negative Input)
PB2	SCK (Serial Clock Input for Serial Programming) INT0 (External Interrupt0 Input) ADC1 (ADC Input Channel 1) T0 (Timer/Counter0 External Counter Input)
PB3	ADC2 (ADC Input Channel 2)
PB4	ADC3 (ADC Input Channel 3)
PB5	$\overline{\text{RESET}}$ (External Reset Pin) ADC0 (ADC Input Channel 0)

Analog Pins

Up to four analog inputs can be selected as inputs to Analog-to-Digital Converter (ADC).

Internal Oscillators

The internal Oscillator provides a clock rate of nominally 1.6 MHz for the system clock (CK). Due to large initial variation (0.8 -1.6 MHz) of the internal Oscillator, a tuning capability is built in. Through an 8-bit control register – OSCCAL – the system clock rate can be tuned with less than 1% steps of the nominal clock.

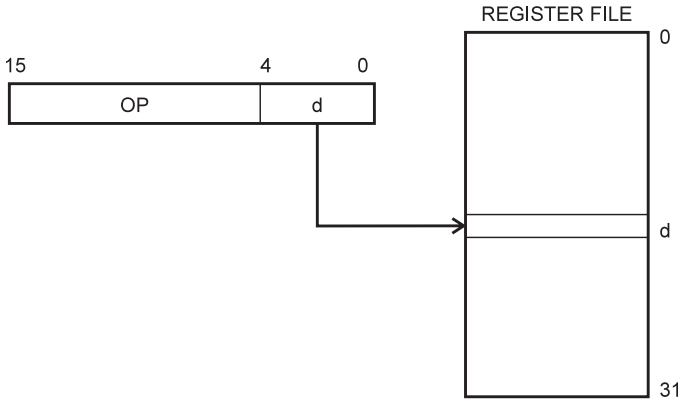
There is an internal PLL that provides a 16x clock rate locked to the system clock (CK) for the use of the Peripheral Timer/Counter1. The nominal frequency of this peripheral clock, PCK, is 25.6 MHz.

The Program and Data Addressing Modes

The ATtiny15L AVR RISC Microcontroller supports powerful and efficient addressing modes. This section describes the various addressing modes supported in the ATtiny15L. In the figures, OP means the operation code part of the instruction word. To simplify, not all figures show the exact location of the addressing bits.

Register Direct, Single-register Rd

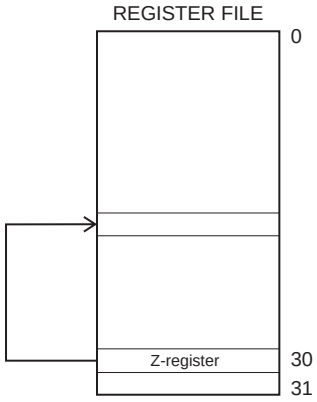
Figure 4. Direct Single-register Addressing



The operand is contained in register d (Rd).

Register Indirect

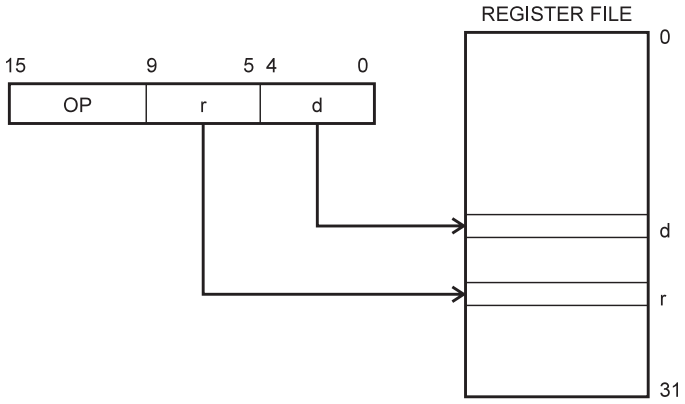
Figure 5. Indirect Register Addressing



The register accessed is the one pointed to by the Z-register low byte (R30).

Register Direct, Two Registers Rd and Rr

Figure 6. Direct Register Addressing, Two Registers



The most typical and general program setup for the Reset and Interrupt Vector Addresses are:

```
Address   Labels    Code                 Comments
$000              rjmp     RESET        ; Reset handler
$001              rjmp     EXT_INT0     ; IRQ0 handler
$002              rjmp     PIN_CHANGE   ; Pin change handler
$003              rjmp     TIM1_CMP     ; Timer1 compare match
$004              rjmp     TIM1_OVF     ; Timer1 overflow handler
$005              rjmp     TIM0_OVF     ; Timer0 overflow handler
$006              rjmp     EE_RDY       ; EEPROM Ready handler
$007              rjmp     ANA_COMP     ; Analog Comparator handler
$008              rjmp     ADC          ; ADC Conversion Handler
;
$009      MAIN:   <instr>  xxx          ; Main program start
  …         …       …      …
```

ATtiny15L Reset Sources

The ATtiny15L has four sources of Reset:

- Power-on Reset. The MCU is reset when the supply voltage is below the Power-on Reset threshold (V_{POR}).
- External Reset. The MCU is reset when a low-level is present on the $\overline{\text{RESET}}$ pin for more than 500 ns.
- Watchdog Reset. The MCU is reset when the Watchdog Timer period expires, and the Watchdog is enabled.
- Brown-out Reset. The MCU is reset when the supply voltage V_{CC} is below the Brown-out Reset threshold (V_{BOT}).

During Reset, all I/O Registers are then set to their initial values, and the program starts execution from address $000. The instruction placed in address $000 must be an RJMP (relative jump) instruction to the reset handling routine. If the program never enables an interrupt source, the Interrupt Vectors are not used, and regular program code can be placed at these locations. The circuit diagram in Figure 12 shows the reset logic. Table 4 and Table 5 define the timing and electrical parameters of the reset circuitry. Note that the Register File is unchanged by a reset.

Table 5. Reset Delay Selections[1]

BODEN[2]	CKSEL [1:0][2]	Start-up Time, t_{TOUT} at V_{CC} = 2.7V	Start-up Time, t_{TOUT} at V_{CC} = 5.0V	Recommended Usage
x	00	256 ms + 18 CK	64 ms + 18 CK	BOD disabled, slowly rising power
x	01	256 ms + 18 CK	64 ms + 18 CK	BOD disabled, slowly rising power
x	10	16 ms + 18 CK	4 ms + 18 CK	BOD disabled, quickly rising power
1	11	18 CK + 32 µs	18 CK + 8 µs	BOD disabled
0	11	18 CK + 128 µs	18 CK + 32 µs	BOD enabled

Notes: 1. On Power-up, the start-up time is increased with typical 0.6 ms.
2. "0" means programmed, "1" means unprogrammed.

Table 5 shows the start-up times from Reset. When the CPU wakes up from Power-down, only the clock-counting part of the start-up time is used. The Watchdog Oscillator is used for timing the real-time part of the start-up time. The number Watchdog Oscillator cycles used for each time-out is shown in Table 6.

The frequency of the Watchdog Oscillator is voltage dependent as shown in the Electrical Characteristics section on page 64. The device is shipped with CKSEL = "00".

Table 6. Number of Watchdog Oscillator Cycles

V_{CC} Conditions	Time-out	Number of Cycles
2.7V	32 µs	8
2.7V	128 µs	32
2.7V	16 ms	4K
2.7V	256 ms	64K
5.0V	8 µs	8
5.0V	32 µs	32
5.0V	4 ms	4K
5.0V	64 ms	64K

Power-on Reset

A Power-on Reset (POR) pulse is generated by an On-chip Detection circuit. The detection level is nominally defined in Table 4. The POR is activated whenever V_{CC} is below the detection level. The POR circuit can be used to trigger the Start-up Reset, as well as detect a failure in supply voltage.

A Power-on Reset (POR) circuit ensures that the device is Reset from Power-on. Reaching the Power-on Reset threshold voltage invokes a delay counter, which determines the delay, for which the device is kept in RESET after V_{CC} rise. The Time-out period of the delay counter can be defined by the user through the CKSEL Fuses. The different selections for the delay period are presented in Table 5. The RESET signal is activated again, without any delay, when the V_{CC} decreases below detection level.

vector $003) is executed if a compare match A in Timer/Counter1 occurs, i.e., when the OCF1A bit is set (one) in the Timer/Counter Interrupt Flag Register (TIFR).

- **Bit 5..3 – Res: Reserved Bits**

These bits are reserved bits in the ATtiny15L and always read as zero.

- **Bit 2 – TOIE1: Timer/Counter1 Overflow Interrupt Enable**

When the TOIE1 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter1 Overflow interrupt is enabled. The corresponding interrupt (at vector $004) is executed if an overflow in Timer/Counter1 occurs, i.e., when the TOV1 bit is set (one) in the Timer/Counter Interrupt Flag Register (TIFR).

- **Bit 1 – TOIE0: Timer/Counter0 Overflow Interrupt Enable**

When the TOIE0 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter0 Overflow interrupt is enabled. The corresponding interrupt (at vector $005) is executed if an overflow in Timer/Counter0 occurs, i.e., when the TOV0 bit is set (one) in the Timer/Counter Interrupt Flag Register (TIFR).

- **Bit 0 – Res: Reserved Bit**

This bit is a reserved bit in the ATtiny15L and always reads as zero.

The Timer/Counter Interrupt Flag Register – TIFR

Bit	7	6	5	4	3	2	1	0	
$38	–	OCF1A	–	–	–	TOV1	TOV0	–	TIFR
Read/Write	R	R/W	R	R	R	R/W	R/W	R	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – Res: Reserved Bit**

This bit is a reserved bit in the ATtiny15L and always reads as zero.

- **Bit 6 – OCF1A: Output Compare Flag 1A**

The OCF1A bit is set (one) when compare match occurs between Timer/Counter1 and the data value in OCR1A (Output Compare Register 1A). OCF1A is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, OCF1A is cleared by writing a logical “1” to the flag. When the I-bit in SREG, OCIE1A, and OCF1A are set (one), the Timer/Counter1 compare match A interrupt is executed.

- **Bits 5..3 – Res: Reserved bits**

These bits are reserved bits in the ATtiny15L and always read as zero.

- **Bit 2 – TOV1: Timer/Counter1 Overflow Flag**

The bit TOV1 is set (one) when an overflow occurs in Timer/Counter1. TOV1 is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, TOV1 is cleared by writing a logical “1” to the flag. When the SREG I-bit, TOIE1 (Timer/Counter1 Overflow Interrupt Enable) and TOV1 are set (one), the Timer/Counter1 Overflow Interrupt is executed.

- **Bits 4, 3 – SM1, SM0: Sleep Mode Select Bits 1 and 0**

These bits select between the three available sleep modes, as shown in Table 7.

Table 7. Sleep Modes

SM1	SM0	Sleep Mode
0	0	Idle mode
0	1	ADC Noise Reduction mode
1	0	Power-down mode
1	1	Reserved

For details, refer to “Sleep Modes” below.

- **Bit 2 – Res: Reserved Bit**

This bit is a reserved bit in the ATtiny15L and always reads as zero.

- **Bits 1, 0 – ISC01, ISC00: Interrupt Sense Control 0 Bit 1 and Bit 0**

The External Interrupt 0 is activated by the external pin INT0 if the SREG I-flag and the corresponding interrupt mask is set (one). The activity on the external INT0 pin that activates the interrupt is defined in Table 8:

Table 8. Interrupt 0 Sense Control(1)

ISC01	ISC00	Description
0	0	The low level of INT0 generates an interrupt request.
0	1	Any change on INT0 generates an interrupt request
1	0	The falling edge of INT0 generates an interrupt request.
1	1	The rising edge of INT0 generates an interrupt request.

Note: 1. When changing the ISC10/ISC00 bits, INT0 must be disabled by clearing its Interrupt Enable bit in the GIMSK Register. Otherwise an interrupt can occur when the bits are changed.

Sleep Modes

To enter any of the three sleep modes, the SE bit in MCUCR must be set (one) and a SLEEP instruction must be executed. The SM1 and SM0 bits in the MCUCR Register select which sleep mode (Idle, ADC Noise Reduction or Power-down) will be activated by the SLEEP instruction (see Table 7). If an enabled interrupt occurs while the MCU is in a sleep mode, the MCU wakes up. The MCU is then halted for four cycles, executes the interrupt routine and resumes execution from the instruction following SLEEP. On wake-up from Power-down mode on pin change, two instruction cycles are executed before the Pin Change Interrupt Flag is updated. The contents of the Register File, SRAM, and I/O memory are unaltered when the device wakes up from sleep. If a reset occurs during sleep mode, the MCU wakes up and executes from the Reset Vector.

Idle Mode

When the SM1/SM0 bits are “00”, the SLEEP instruction forces the MCU into the Idle mode, stopping the CPU but allowing the ADC, Analog Comparator, Timer/Counters, Watchdog and the Interrupt system to continue operating. This enables the MCU to wake-up from external triggered interrupts as well as internal ones like the Timer Overflow Interrupt and Watchdog Reset. If the ADC is enabled, a conversion starts automatically when this mode is entered. If wake-up from the Analog Comparator interrupt is not required, the Analog Comparator can be powered down by setting the ACD-bit in the Analog Comparator Control and Status Register (ACSR). This will reduce power consumption in Idle mode.

- **Bits 3, 2, 1, 0 – CS13, CS12, CS11, CS10: Clock Select Bits 3, 2, 1, and 0**

The Clock Select bits 3, 2, 1, and 0 define the prescaling source of Timer/Counter1.

Table 11. Timer/Counter1 Prescale Select

CS13	CS12	CS11	CS10	Description
0	0	0	0	Timer/Counter1 is stopped.
0	0	0	1	CK*16 (=PCK)
0	0	1	0	CK*8 (=PCK/2)
0	0	1	1	CK*4 (=PCK/4)
0	1	0	0	CK*2 (=PCK/8)
0	1	0	1	CK
0	1	1	0	CK/2
0	1	1	1	CK/4
1	0	0	0	CK/8
1	0	0	1	CK/16
1	0	1	0	CK/32
1	0	1	1	CK/64
1	1	0	0	CK/128
1	1	0	1	CK/256
1	1	1	0	CK/512
1	1	1	1	CK/1024

The Stop condition provides a Timer Enable/Disable function. The prescaled CK modes are scaled directly from the CK oscillator clock.

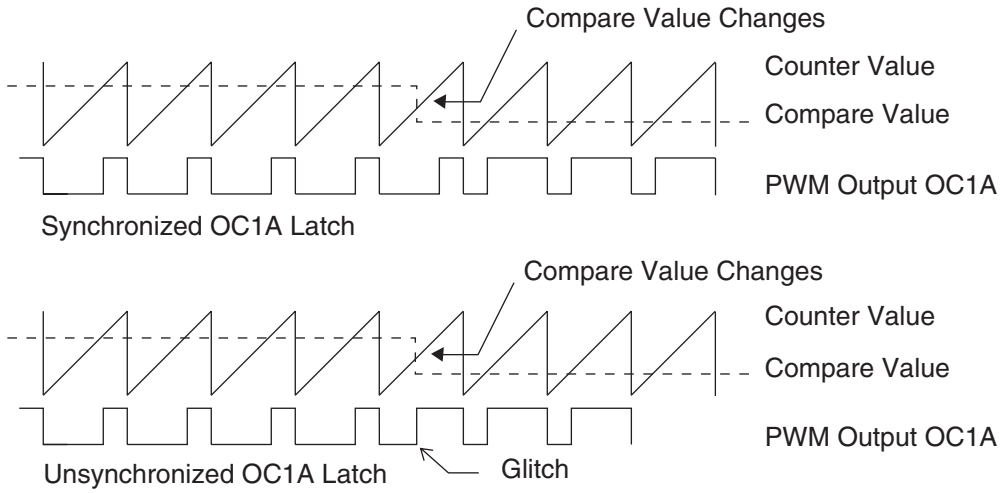
The Timer/Counter1 – TCNT1

Bit	7	6	5	4	3	2	1	0	
$2F	MSB							LSB	TCNT1
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

This 8-bit register contains the value of Timer/Counter1.

Timer/Counter1 is implemented as an up-counter with read and write access. Due to synchronization of the CPU and Timer/Counter1, data written into Timer/Counter1 is delayed by one CPU clock cycle.

Figure 22. Effects of Unsynchronized OCR Latching



During the time between the write and the latch operation, a read from OCR1A will read the contents of the temporary location. This means that the most recently written value always will read out of OCR1A.

When OCR1A contains $00 or the top value, as specified in OCR1B Register, the output PB1(OC1A) is held low or high according to the settings of COM1A1/COM1A0. This is shown in Table 13.

Timer/Counter1 Output Compare RegisterB – OCR1B

Bit	7	6	5	4	3	2	1	0	
$2D	MSB							LSB	OCR1B
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	1	1	1	1	1	1	1	1	

The Output Compare Register1 (OCR1B) is an 8-bit read/write register. This register is used in the PWM mode only, and it limits the top value to which the Timer/Counter1 keeps counting. After reaching OCR1B in PWM mode, the counter starts from $00.

Table 13. PWM Outputs when OCR1A = $00 or OCR1B

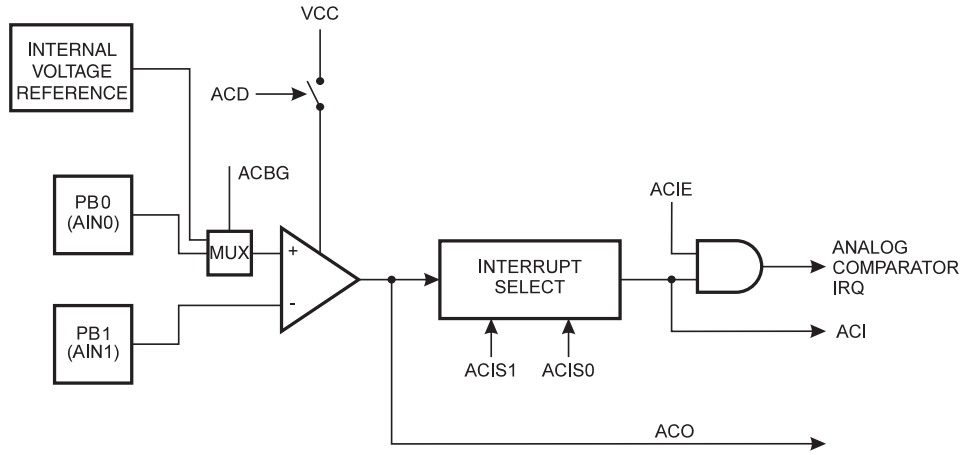
COM1A1	COM1A0	OCR1B	Output PWMn
1	0	$00	L
1	0	OCR1B	H
1	1	$00	H
1	1	OCR1B	L

In PWM mode, the Timer Overflow Flag (TOV1) is set as in normal Timer/Counter mode. Timer Overflow Interrupt1 operates exactly as in normal Timer/Counter mode, i.e., it is executed when TOV1 is set provided that Timer Overflow Interrupt and global interrupts are enabled. This also applies to the Timer Output Compare A Flag and interrupt.

The Analog Comparator

The Analog Comparator compares the input values on the positive pin PB0 (AIN0) and negative pin PB1 (AIN1). When the voltage on the positive pin PB0 (AIN0) is higher than the voltage on the negative pin PB1 (AIN1), the Analog Comparator Output (ACO) is set (one). The comparator's output can trigger a separate interrupt, exclusive to the Analog Comparator. The user can select interrupt triggering on comparator output rise, fall or toggle. A block diagram of the Comparator and its surrounding logic is shown in Figure 24.

Figure 24. Analog Comparator Block Diagram



The Analog Comparator Control and Status Register – ACSR

Bit	7	6	5	4	3	2	1	0	
$08	ACD	ACBG	ACO	ACI	ACIE	–	ACIS1	ACIS0	ACSR
Read/Write	R/W	R/W	R	R/W	R/W	R	R/W	R/W	
Initial Value	0	0	X	0	0	0	0	0	

- **Bit 7 – ACD: Analog Comparator Disable**

When this bit is set (one), the power to the Analog Comparator is switched off. This bit can be set at any time to turn off the Analog Comparator. This will reduce power consumption in Active and Idle mode. When changing the ACD-bit, the Analog Comparator Interrupt must be disabled by clearing the ACIE bit in ACSR. Otherwise an interrupt can occur when the bit is changed.

- **Bit 6 – ACBG: Analog Comparator Bandgap Select**

When this bit is set, a fixed bandgap voltage of 1.22 ± 0.05V replaces the normal input to the positive pin (AIN0) of the comparator. When this bit is cleared, the normal input pin PB0 is applied to the positive pin of the comparator.

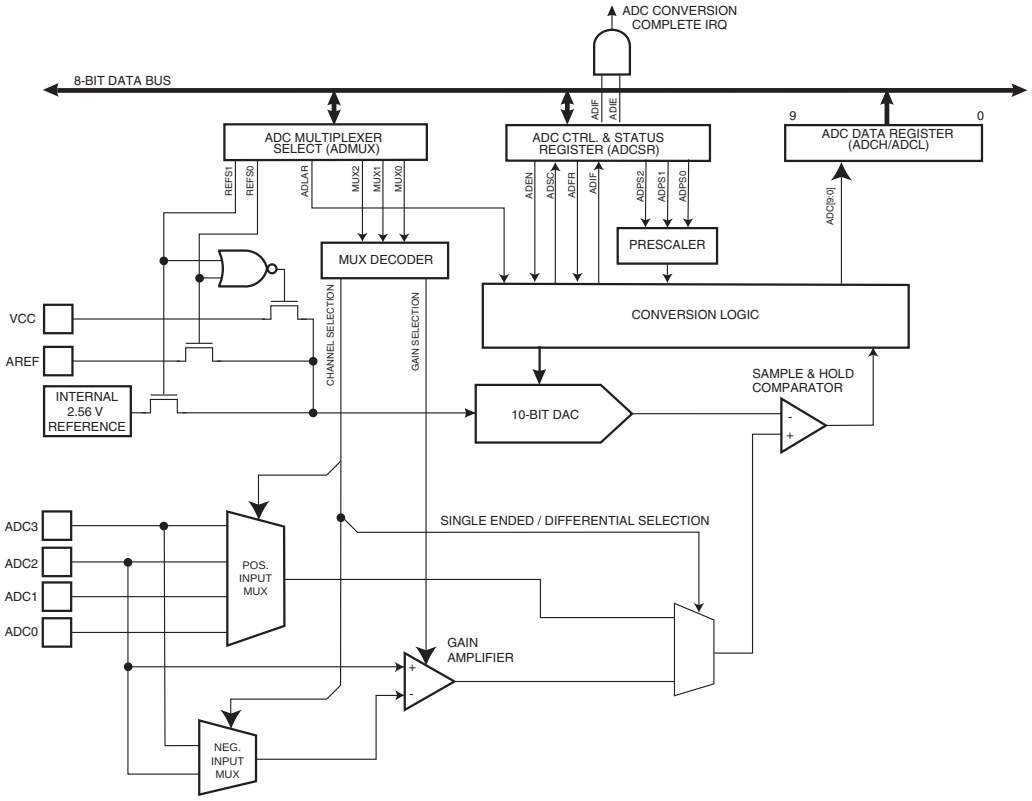
- **Bit 5 – ACO: Analog Comparator Output**

ACO is directly connected to the comparator output.

- **Bit 4 – ACI: Analog Comparator Interrupt Flag**

This bit is set (one) when a comparator output event triggers the interrupt mode defined by ACI1 and ACI0. The Analog Comparator Interrupt routine is executed if the ACIE bit is set (one) and the I-bit in SREG is set (one). ACI is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, ACI is cleared by writing a logical "1" to the flag.

Figure 25. Analog-to-Digital Converter Block Schematic



Operation

The ADC converts an analog input voltage to a 10-bit digital value through successive approximation. The minimum value represents GND and the maximum value represents the selected reference voltage minus 1 LSB.

The voltage reference for the ADC may be selected by writing to the REFS1..0 bits in ADMUX. V_{CC}, the AREF pin, or an internal 2.56V reference may be selected as the ADC voltage reference. Optionally, the 2.56V internal voltage reference may be decoupled by an external capacitor at the AREF pin to improve noise immunity.

The analog input channel and differential gain are selected by writing to the MUX2..0 bits in ADMUX. Any of the four ADC input pins ADC3..0 can be selected as single-ended inputs to the ADC. ADC2 and ADC3 can be selected as positive and negative input, respectively, to the differential gain amplifier.

If differential channels are selected, the differential gain stage amplifies the voltage difference between the selected input pair by the selected gain factor, 1x or 20x, according to the setting of the MUX2..0 bits in ADMUX. This amplified value then becomes the analog input to the ADC. If single-ended channels are used, the gain amplifier is bypassed altogether.

If ADC2 is selected as both the positive and negative input to the differential gain amplifier (ADC2 - ADC2), the remaining offset in the gain stage and conversion circuitry can be measured directly as the result of the conversion. This figure can be subtracted from subsequent conversions with the same gain setting to reduce offset error to below 1 LSB.

The ADC can operate in two modes – Single Conversion and Free Running. In Single Conversion mode, each conversion will have to be initiated by the user. In Free Running

the ADC is switched on by setting the ADEN bit in ADCSR. The prescaler keeps running for as long as the ADEN bit is set, and is continuously reset when ADEN is low.

When initiating a conversion by setting the ADSC bit in ADCSR, the conversion starts at the following rising edge of the ADC clock cycle. If differential channels are selected, the conversion will only start at every other rising edge of the ADC clock cycle after ADEN was set.

A normal conversion takes 13 ADC clock cycles. In certain situations, the ADC needs more clock cycles to perform initialization and minimize offset errors. These extended conversions take 25 ADC clock cycles and occur as the first conversion after one of the following events:

- The ADC is switched on (ADEN in ADCSR is set).
- The voltage reference source is changed (the REFS1..0 bits in ADMUX change value).
- A differential channel is selected (MUX2 in ADMUX is “1”). Note that subsequent conversions on the same channel are not extended conversions.

The actual sample-and-hold takes place 1.5 ADC clock cycles after the start of a normal conversion and 13.5 ADC clock cycles after the start of an extended conversion. When a conversion is complete, the result is written to the ADC Data Registers, and ADIF is set. In Single Conversion mode, ADSC is cleared simultaneously. The software may then set ADSC again, and a new conversion will be initiated on the first rising ADC clock edge. In Free Running mode, a new conversion will be started immediately after the conversion completes while ADSC remains high. Using Free Running mode and an ADC clock frequency of 200 kHz gives the lowest conversion time, 65 µs, equivalent to 15 kSPS. For a summary of conversion times, see Table 18.

Figure 27. ADC Timing Diagram, First Conversion (Single Conversion Mode)

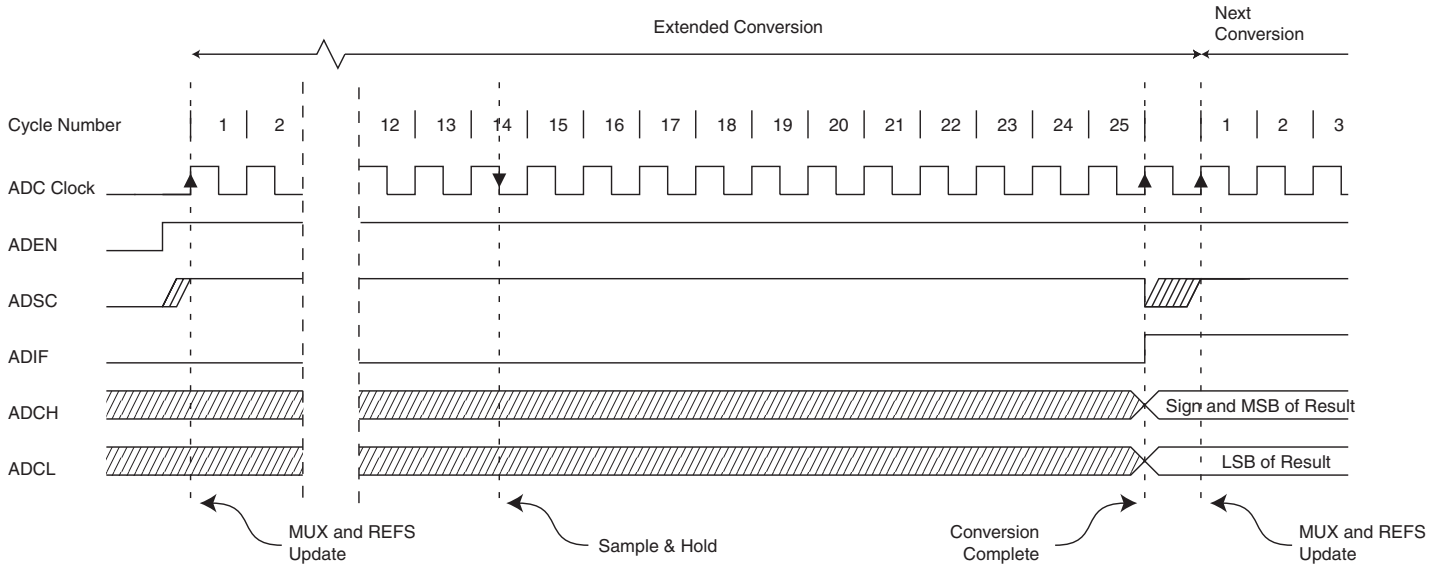


Figure 28. ADC Timing Diagram, Single Conversion

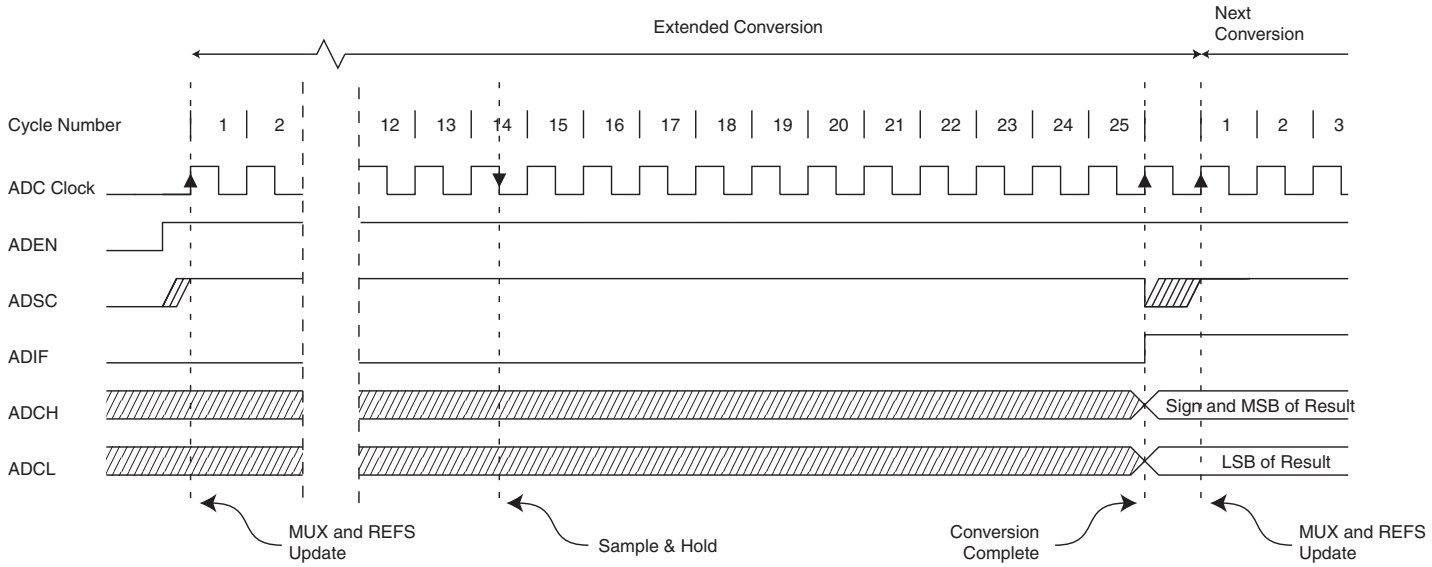


Figure 29. ADC Timing Diagram, Free Running Conversion

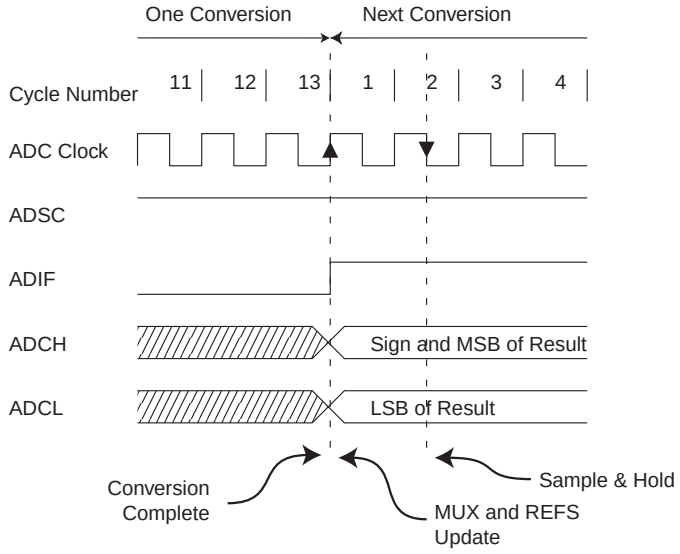


Table 18. ADC Conversion Time

Condition	Sample & Hold (Cycles from Start of Conversion)	Conversion Time (Cycles)	Conversion Time (µs)
Extended Conversion	13.5	25.0	125 - 500
Normal Conversions	1.5	13.0	65 - 260

- **Bits 4..3 – Res: Reserved Bits**

These bits are reserved bits in the ATtiny15L and always read as zero.

- **Bits 2..0 – MUX2..MUX0: Analog Channel and Gain Selection Bits 2..0**

The value of these bits selects which analog input is connected to the ADC. In case of differential input (PB3 - PB4), gain selection is also made with these bits. Selecting PB3 as both inputs to the differential gain stage enables offset measurements. Refer to Table 20 for details. If these bits are changed during a conversion, the change will not go into effect until this conversion is complete (ADIF in ADCSR is set).

Table 20. Input Channel and Gain Selections

MUX2..0	Single-ended Input	Positive Differential Input	Negative Differential Input	Gain
000	ADC0 (PB5)	N/A		
001	ADC1 (PB2)			
010	ADC2 (PB3)			
011	ADC3 (PB4)			
100(1)	N/A	ADC2 (PB3)	ADC2 (PB3)	1x
101(1)		ADC2 (PB3)	ADC2 (PB3)	20x
110		ADC2 (PB3)	ADC3 (PB4)	1x
111		ADC2 (PB3)	ADC3 (PB4)	20x

Note: 1. For offset calibration only. See “Operation” on page 42.

The ADC Control and Status Register – ADCSR

Bit	7	6	5	4	3	2	1	0	
$06	ADEN	ADSC	ADFR	ADIF	ADIE	ADPS2	ADPS1	ADPS0	ADCSR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

- **Bit 7 – ADEN: ADC Enable**

Writing a logical “1” to this bit enables the ADC. By clearing this bit to zero, the ADC is turned off. Turning the ADC off while a conversion is in progress will terminate this conversion.

- **Bit 6 – ADSC: ADC Start Conversion**

In Single Conversion mode, a logical “1” must be written to this bit to start each conversion. In Free Running mode, a logical “1” must be written to this bit to start the first conversion.

When the conversion completes, ADSC returns to zero in Single Conversion mode and stays high in Free Running mode.

Writing a “0” to this bit has no effect.

- **Bit 5 – ADFR: ADC Free Running Select**

When this bit is set (one), the ADC operates in Free Running mode. In this mode, the ADC samples and updates the Data Registers continuously. Clearing this bit (zero) will terminate Free Running mode. If active channels are used (MUX2 in ADMUX set), the

In Normal mode, this pin can serve as the external counter clock input. See the Timer/Counter0 description for further details. If external Timer/Counter clocking is selected, activity on this pin will clock the counter even if it is configured as an output.

- **MISO/OC1A/AIN1 – PORT B, Bit 1**

In Serial Programming mode, this pin serves as the serial data output, MISO.

In Normal mode, this pin can serve as Timer/Counter1 output compare match output (OC1A). See the Timer/Counter1 description for further details, and how to enable the output. The OC1A pin is also the output pin for PWM mode timer function.

This pin also serves as the negative input of the On-chip Analog Comparator.

- **MOSI/AIN0/AREF – PORT B, Bit 0**

In Serial Programming mode, this pin serves as the serial data input, MOSI.

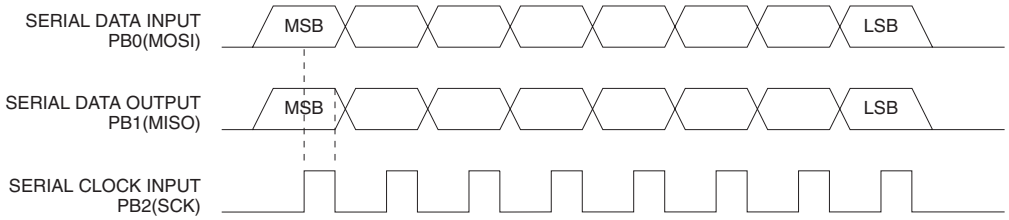
In Normal mode, this pin also serves as the positive input of the On-chip Analog Comparator.

In ATtiny15L, this pin can be chosen to be the reference voltage for the ADC. Refer to the section “The Analog-to-Digital Converter, Analog Multiplexer, and Gain Stages” for details.

Data Polling

When a byte is being programmed into the Flash or EEPROM, reading the address location being programmed will give the value $FF. At the time the device is ready for a new byte, the programmed value will read correctly. This is used to determine when the next byte can be written. This will not work for the value $FF so when programming this value, the user will have to wait for at least $t_{WD\_PROG\_FL}$ before programming the next Flash byte, or $t_{WD\_PROG\_EE}$ before the next EEPROM byte. As a chip-erased device contains $FF in all locations, programming of addresses that are meant to contain $FF can be skipped. This does not apply if the EEPROM is reprogrammed without chip-erasing the device. In that case, data polling cannot be used for the value $FF and the user will have to wait at least $t_{WD\_PROG\_EE}$ before programming the next byte. See Table 30 for $t_{WD\_PROG\_FL}$ and $t_{WD\_PROG\_EE}$ values.

Figure 34. Low-voltage Serial Programming Waveforms



Low-voltage Serial Programming Characteristics

Figure 35. Low-voltage Serial Programming Timing

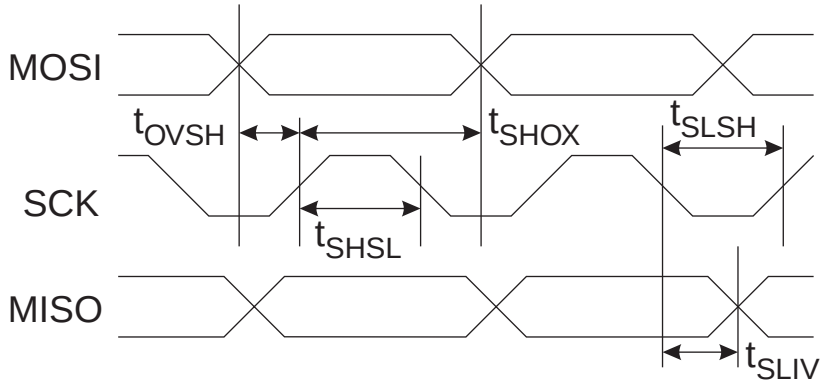


Table 28. Low-voltage Serial Programming Characteristics, T_A = -40°C to 85°C, V_{CC} = 2.7 - 5.5V (Unless Otherwise Noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	RC Oscillator Frequency (V_{CC} = 2.7 - 5.5V)	0.8	1.6		MHz
t_{CLCL}	RC Oscillator Period (V_{CC} = 2.7 - 5.5V)		625.0	1250.0	ns
t_{SHSL}	SCK Pulse Width High	2.0 t_{CLCL}			ns
t_{SLSH}	SCK Pulse Width Low	2.0 t_{CLCL}			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	2.0 t_{CLCL}			ns
t_{SLIV}	SCK Low to MISO Valid	10.0	16.0	32.0	ns

Table 29. Minimum Wait Delay after the Chip Erase Instruction

Symbol	Minimum Wait Delay
t_{WD_ERASE}	8.2 ms

Table 30. Minimum Wait Delay after Writing a Flash or EEPROM Location

Symbol	Minimum Wait Delay
t_{WD_FLASH}	4.1 ms
t_{WD_EEPROM}	8.2 ms

Figure 39. Bandgap Voltage vs. V_{CC}

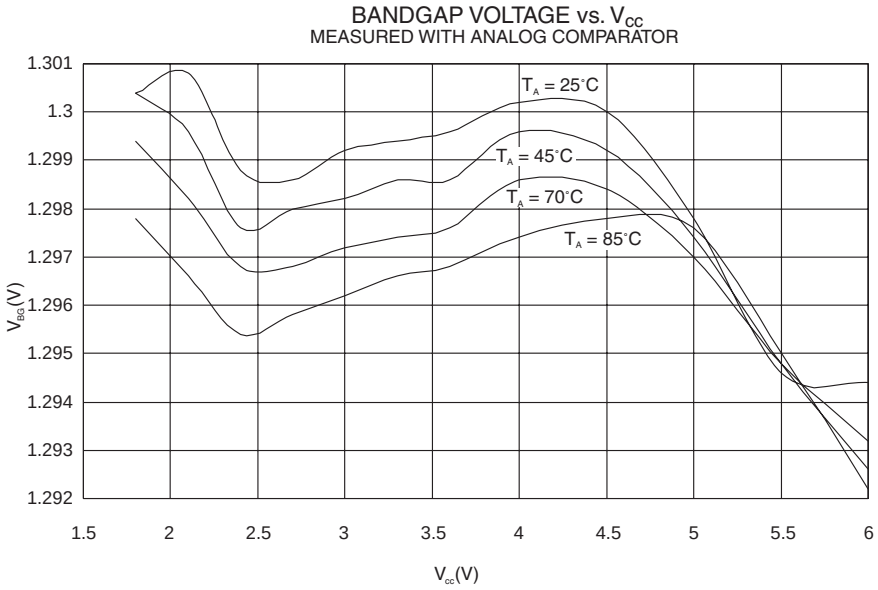
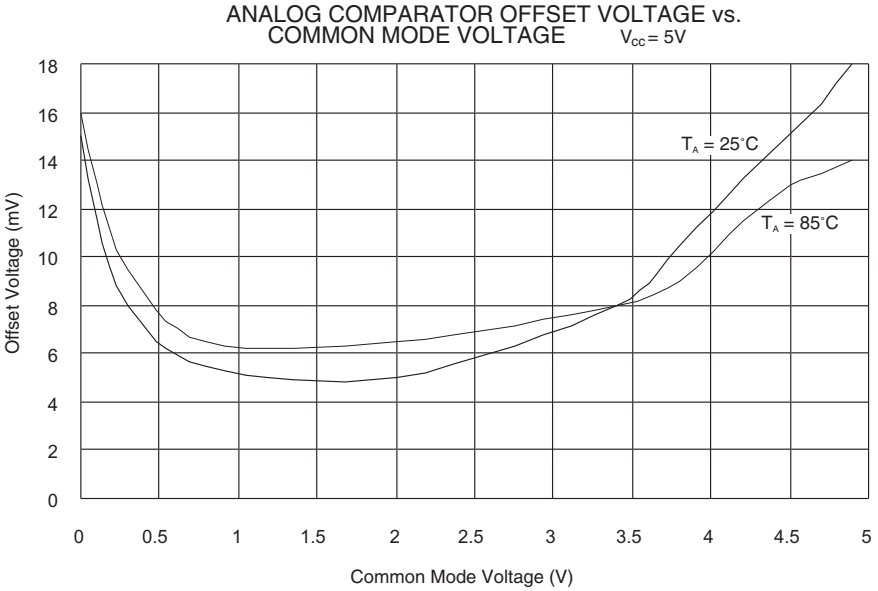


Figure 40. Analog Comparator Offset Voltage vs. Common Mode Voltage



Note: 1. Analog Comparator offset voltage is measured as absolute offset.

Figure 47. I/O Pin Source Current vs. Output Voltage

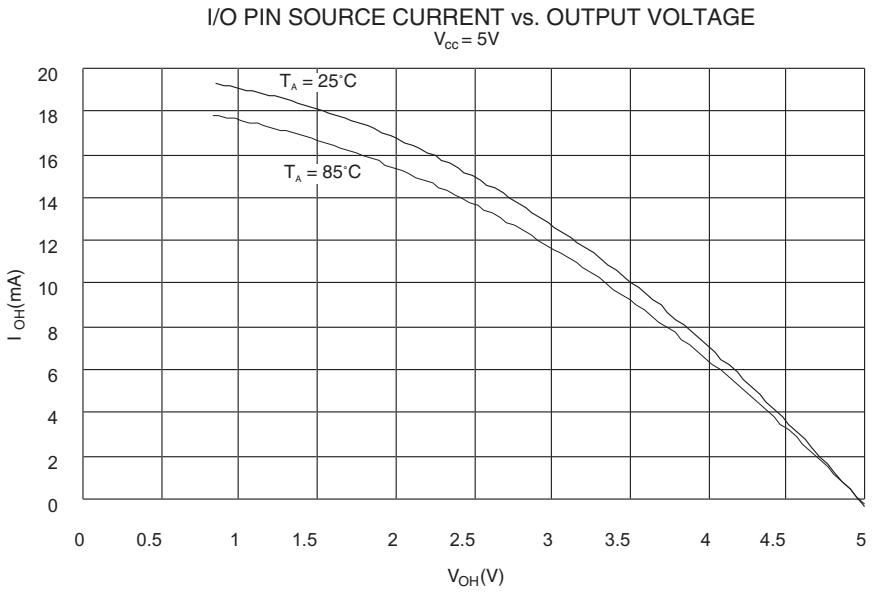


Figure 48. I/O Pin Sink Current vs. Output Voltage

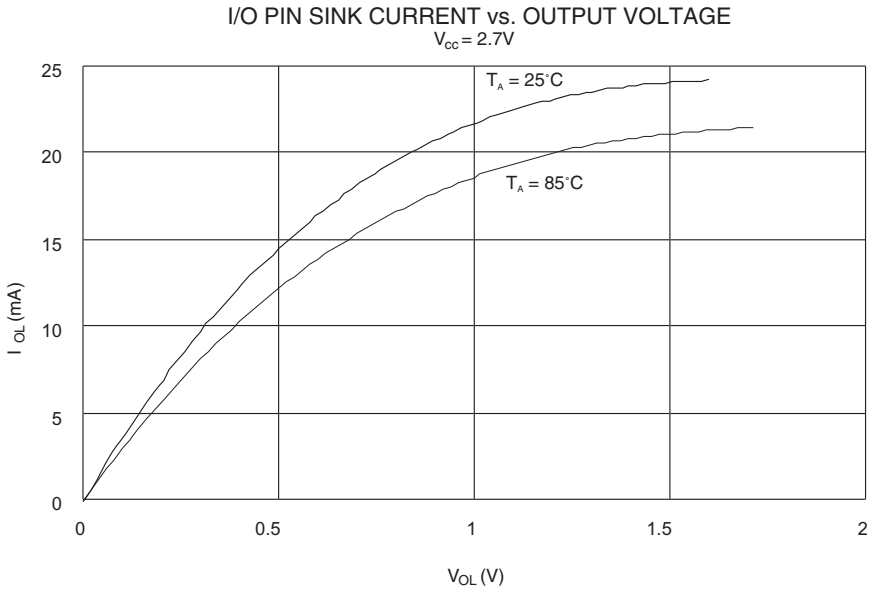


Figure 51. I/O Pin Input Hysteresis vs. V_{CC}