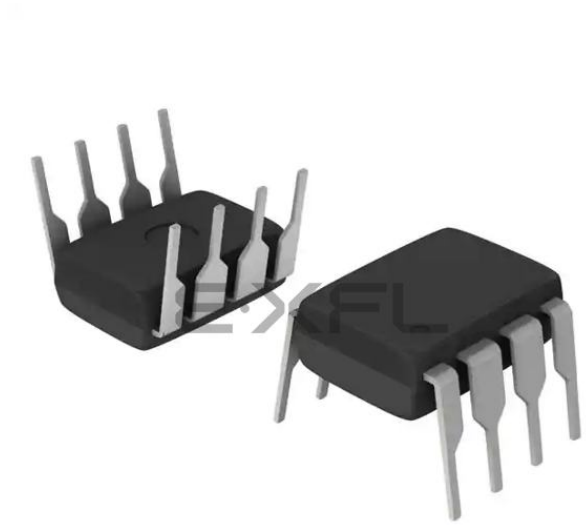

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

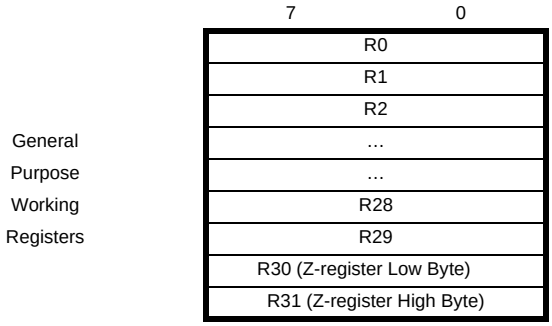
Details	
Product Status	Obsolete
Core Processor	AVR
Core Size	8-Bit
Speed	1.6MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	6
Program Memory Size	1KB (512 x 16)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	-
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	8-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/attiny15l-1pu

A flexible interrupt module has its control registers in the I/O space with an additional Global Interrupt Enable bit in the Status Register. All the different interrupts have a separate Interrupt Vector in the Interrupt Vector table at the beginning of the program memory. The different interrupts have priority in accordance with their Interrupt Vector position. The lower the Interrupt Vector address, the higher the priority.

The General Purpose Register File

Figure 3 shows the structure of the 32 general purpose registers in the CPU.

Figure 3. AVR CPU General Purpose Working Registers



All the register operating instructions in the instruction set have direct- and single-cycle access to all registers. The only exception is the five constant arithmetic and logic instructions SBCI, SUBI, CPI, ANDI, and ORI between a constant and a register and the LDI instruction for load-immediate constant data. These instructions apply to the second half of the registers in the Register File – R16..R31. The general SBC, SUB, CP, AND, OR, and all other operations between two registers or on a single-register apply to the entire Register File.

Registers 30 and 31 form a 16-bit pointer (the Z-pointer) which is used for indirect Flash memory and Register File access. When the Register File is accessed, the contents of R31 is discarded by the CPU.

The ALU – Arithmetic Logic Unit

The high-performance AVR ALU operates in direct connection with all the 32 general purpose working registers. Within a single clock cycle, ALU operations between registers in the Register File are executed. The ALU operations are divided into three main categories – arithmetic, logic and bit-functions. Some microcontrollers in the AVR product family feature a hardware multiplier in the arithmetic part of the ALU.

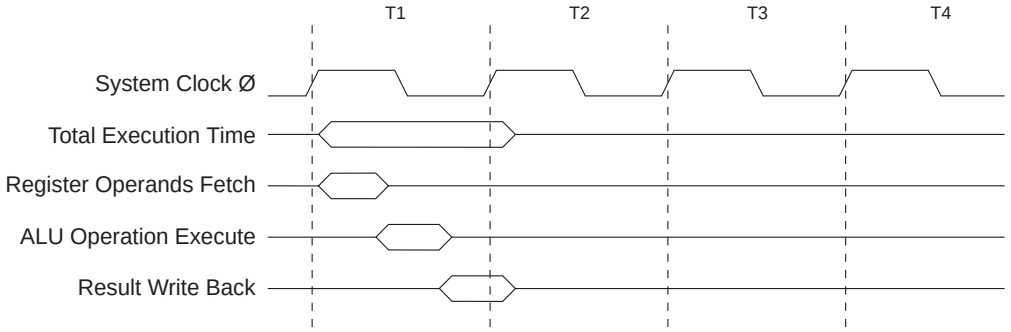
The Flash Program Memory

The ATtiny15L contains 1K byte On-chip, In-System Programmable Flash memory for program storage. Since all instructions are single 16-bit words, the Flash is organized as 512 x 16 words. The Flash memory has an endurance of at least 1,000 write/erase cycles.

The ATtiny15L Program Counter is nine bits wide, thus addressing the 512 words Flash Program memory.

See page 54 for a detailed description on Flash memory programming.

Figure 11. Single Cycle ALU Operation



I/O Memory

The I/O space definition of the ATtiny15L is shown in Table 2.

Table 2. ATtiny15L I/O Space[1]

Address Hex	Name	Function
$3F	SREG	Status Register
$3B	GIMSK	General Interrupt Mask Register
$3A	GIFR	General Interrupt Flag Register
$39	TIMSK	Timer/Counter Interrupt Mask Register
$38	TIFR	Timer/Counter Interrupt Flag Register
$35	MCUCR	MCU Control Register
$34	MCUSR	MCU Status Register
$33	TCCR0	Timer/Counter0 Control Register
$32	TCNT0	Timer/Counter0 (8-bit)
$31	OSCCAL	Oscillator Calibration Register
$30	TCCR1	Timer/Counter1 Control Register
$2F	TCNT1	Timer/Counter1 (8-bit)
$2E	OCR1A	Timer/Counter1 Output Compare Register A
$2D	OCR1B	Timer/Counter1 Output Compare Register B
$2C	SFIOR	Special Function I/O Register
$21	WDTCR	Watchdog Timer Control Register
$1E	EEAR	EEPROM Address Register
$1D	EEDR	EEPROM Data Register
$1C	EECR	EEPROM Control Register
$18	PORTB	Data Register, Port B
$17	DDRB	Data Direction Register, Port B
$16	PINB	Input Pins, Port B
$08	ACSR	Analog Comparator Control and Status Register
$07	ADMUX	ADC Multiplexer Select Register

Figure 13. "MCU Start-up, $\overline{\text{RESET}}$ Tied to V_{CC}

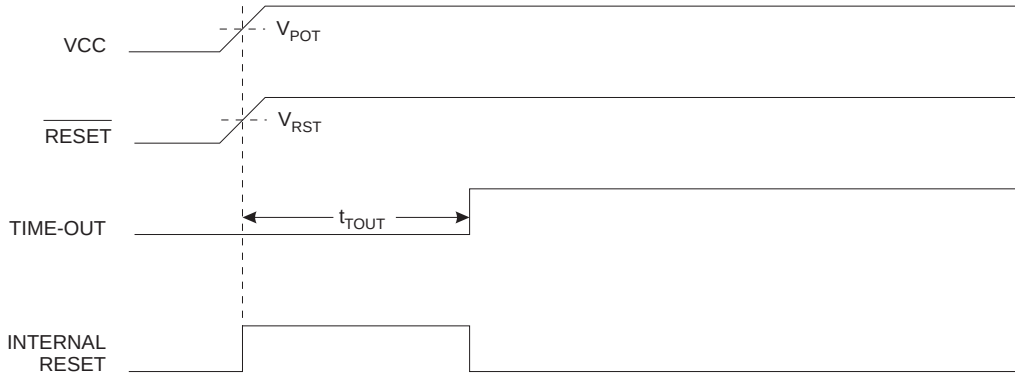
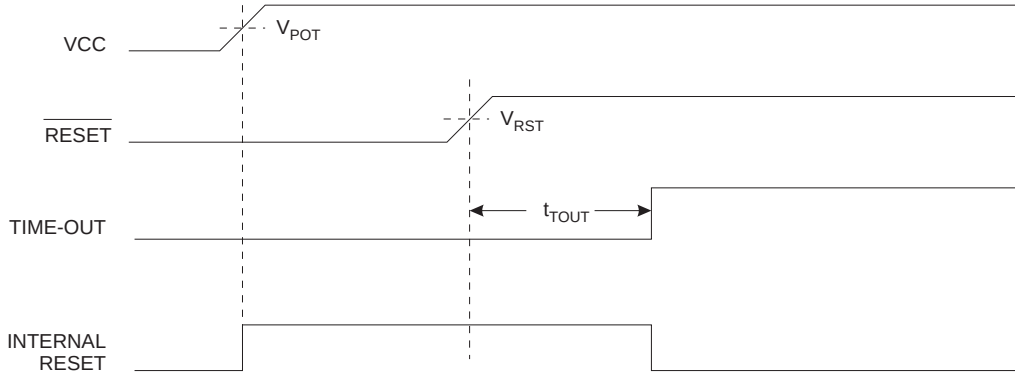


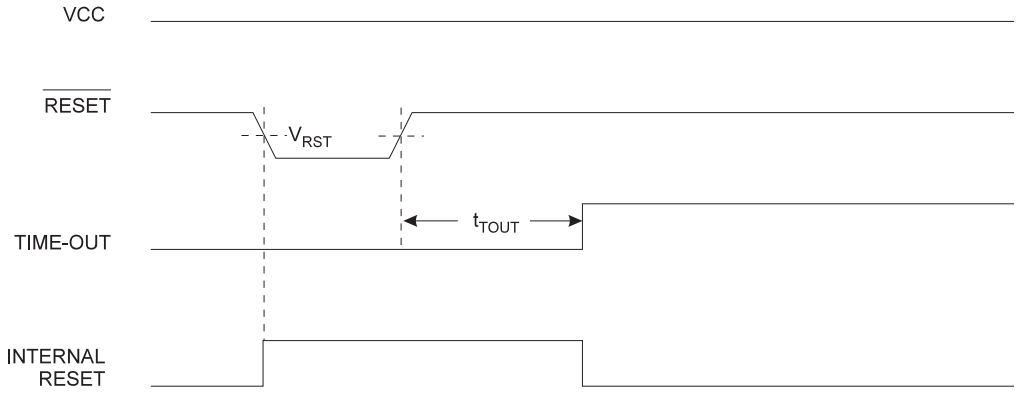
Figure 14. MCU Start-up, $\overline{\text{RESET}}$ Extended Externally



External Reset

An External Reset is generated by a low-level on the $\overline{\text{RESET}}$ pin. Reset pulses longer than 500 ns will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset. When the applied signal reaches the Reset Threshold Voltage (V_{RST}) on its positive edge, the delay timer starts the MCU after the Time-out period t_{TOUT} has expired.

Figure 15. External Reset during Operation



MCU Status Register – MCUSR

The MCU Status Register provides information on which reset source caused an MCU Reset.

Bit	7	6	5	4	3	2	1	0	
$34	–	–	–	–	WDRF	BORF	EXTRF	PORF	MCUSR
Read/Write	R	R	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	See Bit Description				

- **Bit 7..4 – Res: Reserved Bits**

These bits are reserved bits in the ATtiny15L and always read as zero.

- **Bit 3 – WDRF: Watchdog Reset Flag**

This bit is set (one) if a Watchdog Reset occurs. The bit is reset (zero) by a Power-on Reset, or by writing a logical “0” to the flag.

- **Bit 2 – BORF: Brown-out Reset Flag**

This bit is set (one) if a Brown-out Reset occurs. The bit is reset (zero) by a Power-on Reset, or by writing a logical “0” to the flag.

- **Bit 1 – EXTRF: External Reset Flag**

This bit is set (one) if a External Reset occurs. The bit is reset (zero) by a Power-on Reset, or by writing a logical “0” to the flag.

- **Bit 0 – PORF: Power-on Reset Flag**

This bit is set (one) if a Power-on Reset occurs. The bit is reset (zero) by writing a logical “0” to the flag.

To make use of the Reset Flags to identify a reset condition, the user should read and then reset the MCUSR as early as possible in the program. If the register is cleared before another reset occurs, the source of the reset can be found by examining the Reset Flags.

Internal Voltage Reference

ATtiny15L features an internal bandgap reference with a nominal voltage of 1.22V. This reference is used for Brown-out Detection, and it can be used as an input to the Analog Comparator. The 2.56V reference to the ADC is generated from the internal bandgap reference.

Voltage Reference Enable Signals and Start-up Time

The voltage reference has a start-up time that may influence the way it should be used. The maximum start-up time is 10 µs. To save power, the reference is not always turned on. The reference is on during the following situations:

1. When the BOD is enabled (by programming the BODEN Fuse).
2. When the bandgap reference is connected to the Analog Comparator (by setting the AINBG bit in ACSR).
3. When the ADC is enabled.

Thus, when the BOD is not enabled, after setting the AINBG bit, the user must always allow the reference to start-up before the output from the Analog Comparator is used. The bandgap reference uses typically 10 µA, and to reduce power consumption in Power-down mode, the user can avoid the three conditions above to ensure that the reference is turned off before entering Power-down mode.

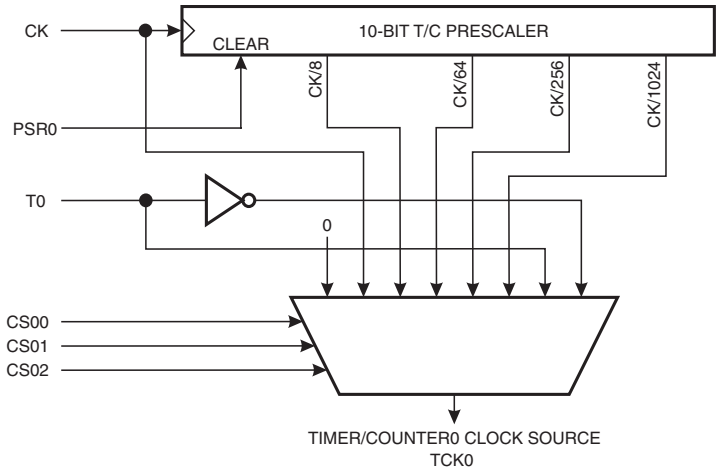
Timer/Counters

The ATtiny15L provides two general purpose 8-bit Timer/Counters. The Timer/Counters have separate prescaling selection from separate 10-bit prescalers. The Timer/Counter0 uses internal clock (CK) as the clock time base. The Timer/Counter1 may use either the internal clock (CK) or the fast peripheral clock (PCK) as the clock time base.

The Timer/Counter0 Prescaler

Figure 18 shows the Timer/Counter prescaler.

Figure 18. Timer/Counter0 Prescaler

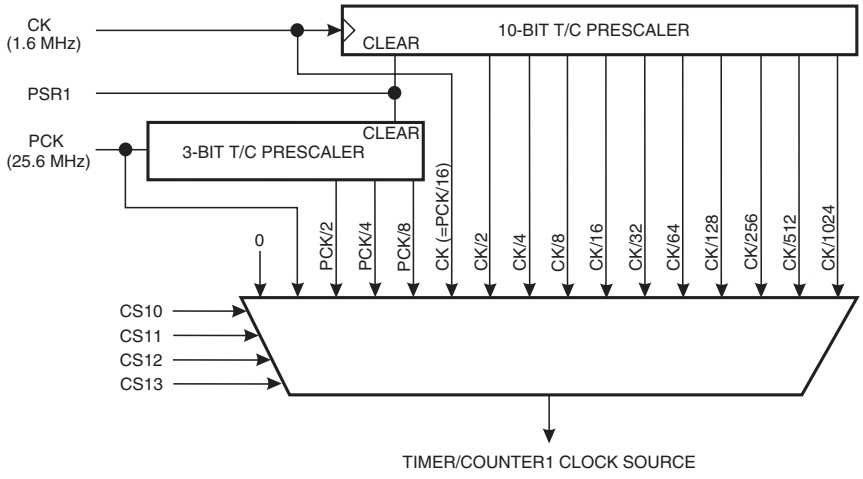


The four prescaled selections are: CK/8, CK/64, CK/256, and CK/1024, where CK is the Oscillator clock. CK, external source and stop, can also be selected as clock sources. Setting the PSR10 bit in SFIOR resets the prescaler. This allows the user to operate with a predictable prescaler.

The Timer/Counter1 Prescaler

Figure 19 shows the Timer/Counter1 prescaler. For Timer/Counter1 the clock selections are: PCK, PCK/2, PCK/4, PCK/8, CK (=PCK/16), CK/2, CK/4, CK/8,CK/16, CK/32, CK/64, CK/128, CK/256, CK/512, CK/1024, and stop. The clock options are described in Table 12 on page 31 and the Timer/Counter1 Control Register (TCCR1). Setting the PSR1 bit in the SFIOR Register resets the 10-bit prescaler. This allows the user to operate with a predictable prescaler.

Figure 19. Timer/Counter1 Prescaler



The Timer Counter 0 – TCNT0

Bit	7	6	5	4	3	2	1	0	
$32	MSB							LSB	TCNT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

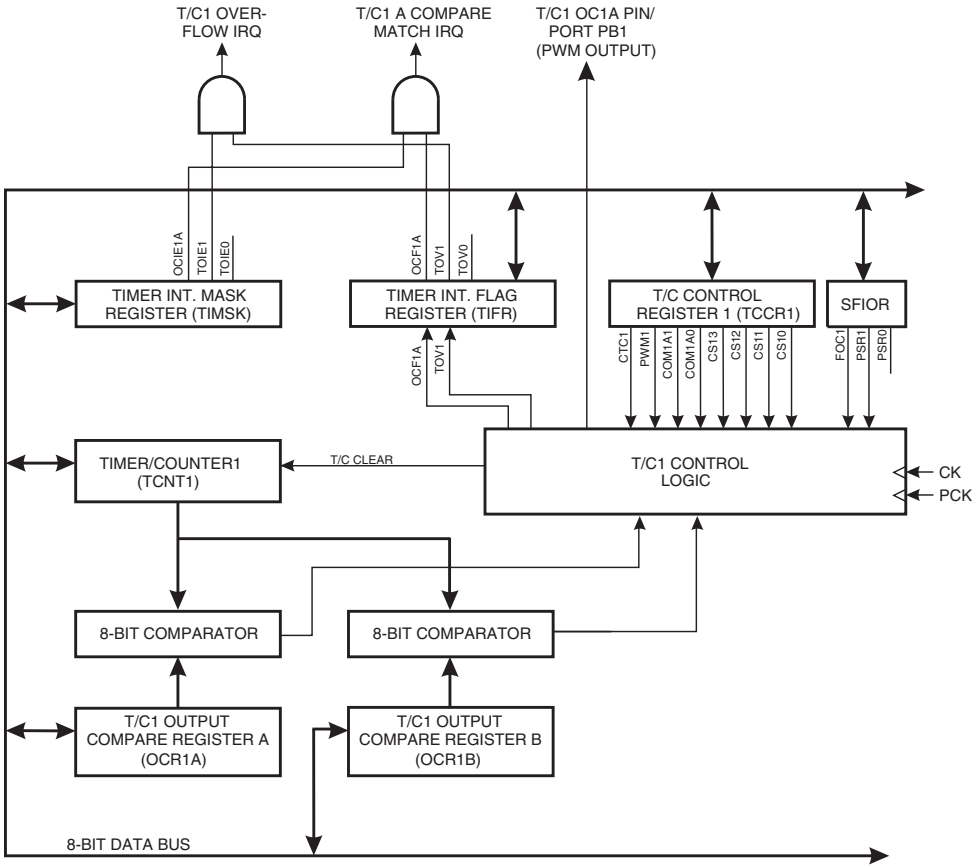
The Timer/Counter0 is implemented as an up-counter with read and write access. If the Timer/Counter0 is written and a clock source is present, the Timer/Counter0 continues counting in the timer clock cycle following the write operation.

The 8-bit Timer/Counter1

This module features a high-resolution and a high-accuracy usage with the lower prescaling opportunities. Timer/Counter1 can also be used as an accurate, high speed, 8-bit Pulse Width Modulator (PWM) using clock speeds up to 25.6 MHz. In this mode, Timer/Counter1 and the Output Compare Registers serve as a standalone PWM. Refer to page 34 for a detailed description of this function. Similarly, the high-prescaling opportunities make this unit useful for lower-speed functions or exact-timing functions with infrequent actions.

Figure 21 shows the block diagram for Timer/Counter1.

Figure 21. Timer/Counter1 Block Diagram



The two Status Flags (Overflow and Compare Match) are found in the Timer/Counter Interrupt Flag Register (TIFR). Control signals are found in the Timer/Counter Control Register (TCCR1). The interrupt enable/disable settings are found in the Timer/Counter Interrupt Mask Register (TIMSK).

The frequency of the PWM will be Timer Clock Frequency divided by OCR1B value + 1.

Table 14. Timer/Counter1 Clock Prescale Select

Clock Selection	OCR1B	PWM Frequency
CK	159	10 kHz
PCK/8	159	20 kHz
PCK/4	213	30 kHz
PCK/4	159	40 kHz
PCK/2	255	50 kHz
PCK/2	213	60 kHz
PCK/2	181	70 kHz
PCK/2	159	80 kHz
PCK/2	141	90 kHz
PCK	255	100 kHz
PCK	231	110 kHz
PCK	213	120 kHz
PCK	195	130 kHz
PCK	181	140 kHz
PCK	169	150 kHz

The exact duty-cycle of the non-inverted PWM output is:

$$\frac{(\text{OCR1A} + 1) \times T_{T1} - T_{PCK}}{(\text{OCR1B} + 1) \times T_{T1}}$$

Where:

T_{T1} is the period of the selected Timer/Counter1 Clock Source.

T_{PCK} is the period of the PCK Clock (39.1 ns).

1. In the same operation, write a logical “1” to WDTOE and WDE. A logical “1” must be written to WDE even though it is set to one before the disable operation starts.
2. Within the next four clock cycles, write a logical “0” to WDE. This disables the Watchdog.

- **Bits 2..0 – WDP2, WDP1, WDP0: Watchdog Timer Prescaler Bits 2, 1, and 0**

The WDP2, WDP1 and WDP0 bits determine the Watchdog Timer prescaling when the Watchdog Timer is enabled. The different prescaling values and their corresponding time-out periods are shown in Table 15.

Table 15. Watchdog Timer Prescale Select

WDP2	WDP1	WDP0	Time-out Period
0	0	0	16K cycles
0	0	1	32K cycles
0	1	0	64K cycles
0	1	1	128K cycles
1	0	0	256K cycles
1	0	1	512K cycles
1	1	0	1,024K cycles
1	1	1	2,048K cycles

The user should poll the EEWE bit before starting the read operation. If a write operation is in progress when new data or address is written to the EEPROM I/O Registers, the write operation will be interrupted and the result is undefined.

The calibrated oscillator is used to time EEPROM. In Table 16 the typical programming time is listed for EEPROM access from the CPU.

Table 16. Typical EEPROM Programming Times

Parameter	Number of Calibrated RC Oscillator Cycles	Min Programming Time	Max Programming Time
EEPROM write (from CPU)	8192	4.6 ms	8.2 ms

Preventing EEPROM Corruption

During periods of low V_{CC}, the EEPROM data can be corrupted because the supply voltage is too low for the CPU and the EEPROM to operate properly. These issues are the same as for board-level systems using the EEPROM and the same design solutions should be applied.

An EEPROM data corruption can be caused by two situations when the voltage is too low. First, a regular write sequence to the EEPROM requires a minimum voltage to operate correctly. Second, the CPU itself can execute instructions incorrectly if the supply voltage for executing instructions is too low.

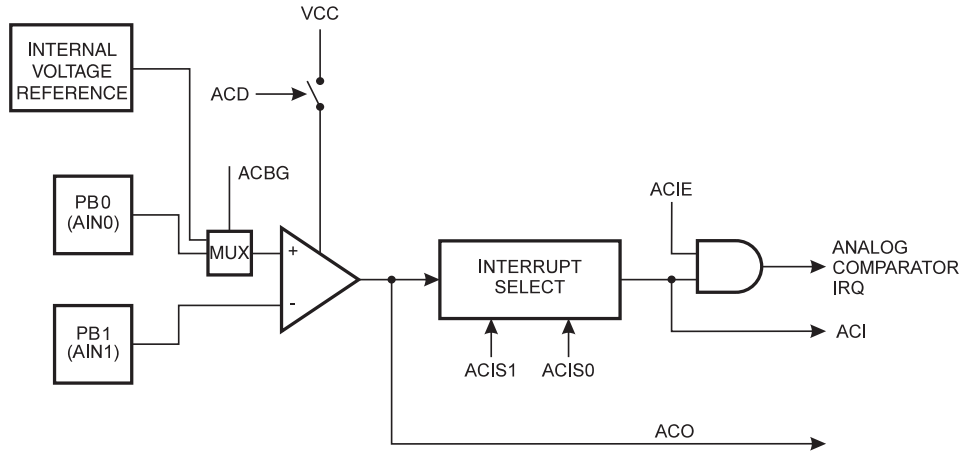
EEPROM data corruption can easily be avoided by following these design recommendations (one is sufficient):

1. Keep the AVR RESET active (low) during periods of insufficient power supply voltage. This can be done by enabling the internal Brown-out Detector (BOD) if the operating voltage matches the detection level. If not, an external low V_{CC} Reset Protection circuit can be applied.
2. Keep the AVR core in Power-down sleep mode during periods of low V_{CC}. This will prevent the CPU from attempting to decode and execute instructions, effectively protecting the EEPROM Registers from unintentional writes.
3. Store constants in Flash memory if the ability to change memory contents from software is not required. Flash memory cannot be updated by the CPU and will not be subject to corruption.

The Analog Comparator

The Analog Comparator compares the input values on the positive pin PB0 (AIN0) and negative pin PB1 (AIN1). When the voltage on the positive pin PB0 (AIN0) is higher than the voltage on the negative pin PB1 (AIN1), the Analog Comparator Output (ACO) is set (one). The comparator's output can trigger a separate interrupt, exclusive to the Analog Comparator. The user can select interrupt triggering on comparator output rise, fall or toggle. A block diagram of the Comparator and its surrounding logic is shown in Figure 24.

Figure 24. Analog Comparator Block Diagram



The Analog Comparator Control and Status Register – ACSR

Bit	7	6	5	4	3	2	1	0	
$08	ACD	ACBG	ACO	ACI	ACIE	–	ACIS1	ACIS0	ACSR
Read/Write	R/W	R/W	R	R/W	R/W	R	R/W	R/W	
Initial Value	0	0	X	0	0	0	0	0	

- **Bit 7 – ACD: Analog Comparator Disable**

When this bit is set (one), the power to the Analog Comparator is switched off. This bit can be set at any time to turn off the Analog Comparator. This will reduce power consumption in Active and Idle mode. When changing the ACD-bit, the Analog Comparator Interrupt must be disabled by clearing the ACIE bit in ACSR. Otherwise an interrupt can occur when the bit is changed.

- **Bit 6 – ACBG: Analog Comparator Bandgap Select**

When this bit is set, a fixed bandgap voltage of 1.22 ± 0.05V replaces the normal input to the positive pin (AIN0) of the comparator. When this bit is cleared, the normal input pin PB0 is applied to the positive pin of the comparator.

- **Bit 5 – ACO: Analog Comparator Output**

ACO is directly connected to the comparator output.

- **Bit 4 – ACI: Analog Comparator Interrupt Flag**

This bit is set (one) when a comparator output event triggers the interrupt mode defined by ACI1 and ACI0. The Analog Comparator Interrupt routine is executed if the ACIE bit is set (one) and the I-bit in SREG is set (one). ACI is cleared by hardware when executing the corresponding interrupt handling vector. Alternatively, ACI is cleared by writing a logical "1" to the flag.

I/O Port B

All AVR ports have true read-modify-write functionality when used as general digital I/O ports. This means that the direction of one port pin can be changed without unintentionally changing the direction of any other pin with the SBI and CBI instructions. The same applies for changing drive value (if configured as output) or enabling/disabling of pull-up resistors (if configured as input).

Port B is a 6-bit bi-directional I/O port.

Three data memory address locations are allocated for Port B, one each for the Data Register – PORTB, $18, Data Direction Register – DDRB, $17, and the Port B Input Pins – PINB, $16. The Port B Input Pins address is read-only, while the Data Register and the Data Direction Register are read/write.

Ports PB5..0 have special functions as described in the section “Pin Descriptions” on page 4. If PB5 is not configured as External Reset, it is input with no pull-up or as an open-drain output. All I/O pins have individually selectable pull-ups, which can be overridden with pull-up disable.

The Port B output buffers on PB0 to PB4 can sink 20 mA and thus drive LED displays directly. PB5 can sink 12 mA. When pins PB0 to PB4 are used as inputs and are externally pulled low, they will source current (I_{IL}) if the internal pull-ups are activated.

Unconnected Pins

If some pins are unused, it is recommended to ensure that these pins have a defined level. The simplest method to ensure a defined level of an unused pin, is to enable the internal pull-up. In this case, the pull-up will be disabled during reset. If low power consumption during reset is important, it is recommended to use an external pull-up or pull-down. Connecting unused pins directly to Vcc or GND is not recommended, since this may cause excessive currents if the pin is accidentally configured as an output.

Alternative Functions of Port B

In ATtiny15L four Port B pins – PB2, PB3, PB4, and PB5 – have alternative functions as inputs for the ADC. If some Port B pins are configured as outputs, it is essential that these do not switch when a conversion is in progress. This might corrupt the result of the conversion. During Power-down mode and ADC Noise Reduction mode, the Schmitt triggers of the digital inputs are disconnected on these pins. This allows an analog input voltage close to $V_{CC}/2$ to be present during Power-down without causing excessive power consumption. The Port B pins with alternate functions are shown in Table 1 on page 4.

When the pins PB4..0 are used for the alternate function, the DDRB and PORTB Registers have to be set according to the alternate function description. When PB5 is used as External Reset pin, the values in the corresponding DDRB and PORTB bit are ignored.

The Port B Data Register – PORTB

Bit	7	6	5	4	3	2	1	0	
$18	–	–	–	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	PORTB
Read/Write	R	R	R	R/W	R/WS	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The Port B Data Direction Register – DDRB

Bit	7	6	5	4	3	2	1	0	
$17	–	–	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	DDRB
Read/Write	R	R	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

Memory Programming

Program and Data Memory Lock Bits

The ATtiny15L MCU provides two Lock bits that can be left unprogrammed, “1”, or can be programmed, “0”, to obtain the additional features listed in Table 23. The Lock bits can only be erased with the Chip Erase command.

Table 23. Lock Bit Protection Modes

Memory Lock Bits			
Mode	**LB1**	**LB2**	**Protection Type**
1	1	1	No memory lock features enabled.
2	0	1	Further programming of the Flash and EEPROM is disabled.
3	0	0	Same as mode 2, but verify is also disabled.

Fuse Bits

The ATtiny15L has six Fuse bits (BODLEVEL, BODEN, SPIEN, RSTDSBL, and CKSEL1..0). All the Fuse bits are programmable in both High-voltage and Low-voltage Serial Programming modes. Changing the Fuses does not have effect while in programming mode.

- The BODLEVEL Fuse selects the Brown-out Detection level and changes the start-up times. See “Brown-out Detection” on page 17. See Table 5 on page 15. Default value is programmed “0”.
- When the BODEN Fuse is programed “0”, the Brown-out Detector is enabled. See “Brown-out Detection” on page 17. Default value is unprogrammed “1”.
- When the SPIEN Fuse bit is programmed “0”, Low-voltage Serial Program and Data Downloading is enabled. Default value is programmed “0”. Unprogramming this fuse while in the Low-voltage Serial Programming mode will disable future In-System downloading attempts.
- When the RSTDISBL Fuse is programmed “0”, the External Reset function of pin PB5 is disabled(1). Default value is unprogrammed “1”. Programming this fuse while in the Low-voltage Serial Programming mode will disable future In-System downloading attempts.
- CKSEL1..0 Fuses: See Table 5 on page 15 for which combination of CKSEL1..0 to use. Default value is “00”, 64 ms + 18 CK.

The status of the Fuse bits is not affected by Chip Erase.

Note: 1. If the RSTDISBL Fuse is programmed, then the programming hardware should apply +12V to PB5 while the ATtiny15L is in Power-on Reset. If not, the part can fail to enter Programming mode caused by drive contention on PB0 and/or PB5.

Signature Bytes

All Atmel microcontrollers have a three-byte signature code that identifies the device.

The three bytes reside in a separate address space, and for the ATtiny15L they are:

1. $000 : $1E (indicates manufactured by Atmel).
2. $001 : $90 (indicates 1 Kb Flash memory).
3. $002 : $06 (indicates ATtiny15L device when $001 is $90).

High-voltage Serial Programming Characteristics

Figure 32. High-voltage Serial Programming Timing

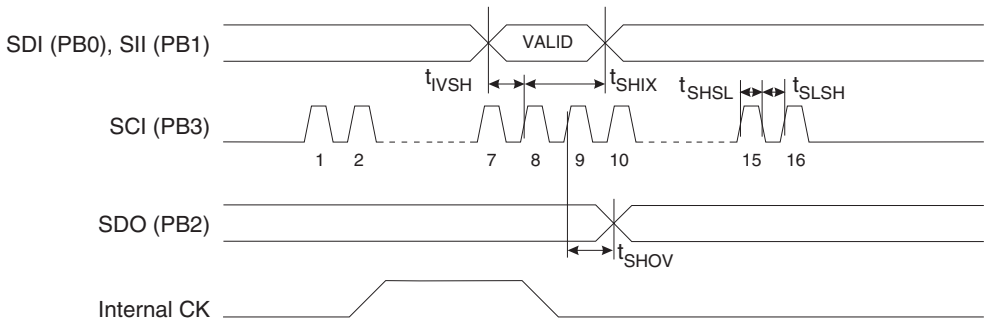


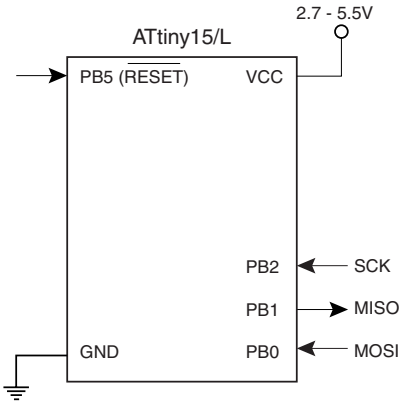
Table 26. High-voltage Serial Programming Characteristics, T_A = 25°C ± 10%, V_{CC} = 5.0V ± 10% (unless otherwise noted)

Symbol	Parameter	Min	Typ	Max	Units
t_{SHSL}	SCI (PB3) Pulse Width High	25.0			ns
t_{SLSH}	SCI (PB3) Pulse Width Low	25.0			ns
t_{IVSH}	SDI (PB0), SII (PB1) Valid to SCI (PB3) High (8th edge)	50.0			ns
t_{SHIX}	SDI (PB0), SII (PB1) Hold after SCI (PB3) High (8th edge)	50.0			ns
t_{SHOV}	SCI (PB3) High (9th edge) to SDO (PB2) Valid	10.0	16.0	32.0	ns

Low-voltage Serial Downloading

Both the program and data memory arrays can be programmed using the SPI bus while $\overline{\text{RESET}}$ is pulled to GND. The serial interface consists of pins SCK, MOSI (input) and MISO (output). See Figure 33. After $\overline{\text{RESET}}$ is set low, the Programming Enable instruction needs to be executed first before program/erase instructions can be executed.

Figure 33. Serial Programming and Verify



For the EEPROM, an auto-erase cycle is provided within the self-timed write instruction and there is no need to first execute the Chip Erase instruction. The Chip Erase instruction turns the content of every memory location in both the program and EEPROM arrays into $FF.

The program and EEPROM memory arrays have separate address spaces: $0000 to $01FF for Program memory and $000 to $03F for EEPROM memory.

The device is clocked from the internal clock at the uncalibrated minimum frequency (0.8 - 1.6 MHz). The minimum low and high periods for the serial clock (SCK) input are defined as follows:

Low: > 2 MCU clock cycles

High: > 2 MCU clock cycles

Low-voltage Serial Programming Algorithm

When writing serial data to the ATtiny15L, data is clocked on the rising edge of SCK. When reading data from the ATtiny15L, data is clocked on the falling edge of SCK. See Figure 34, Figure 35, and Table 28 for timing details. To program and verify the ATtiny15L in the Serial Programming mode, the following sequence is recommended (See 4-byte instruction formats in Table 27):

1. Power-up sequence:

   Apply power between V_{CC} and GND while $\overline{\text{RESET}}$ and SCK are set to “0”. If the programmer cannot guarantee that SCK is held low during Power-up, $\overline{\text{RESET}}$ must be given a positive pulse of at least two MCU cycles duration after SCK has been set to “0”.
2. Wait for at least 20 ms and enable serial programming by sending the Programming Enable serial instruction to the MOSI (PB0) pin. Refer to the above section for minimum low and high periods for the serial clock input SCK.
3. The serial programming instructions will not work if the communication is out of synchronization. When in sync, the second byte ($53) will echo back when issuing the third byte of the Programming Enable instruction. Whether the echo is correct or not, all four bytes of the instruction must be transmitted. If the $53 did not echo back, give SCK a positive pulse and issue a new Programming Enable instruction. If the $53 is not seen within 32 attempts, there is no functional device connected.
4. If a Chip Erase is performed (must be done to erase the Flash), wait t_{WD_ERASE} after the instruction, give $\overline{\text{RESET}}$ a positive pulse, and start over from step 2. See Table 29 on page 63 for t_{WD_ERASE} value.
5. The Flash or EEPROM array is programmed one byte at a time by supplying the address and data together with the appropriate write instruction. An EEPROM memory location is first automatically erased before new data is written. Use data polling to detect when the next byte in the Flash or EEPROM can be written. If polling is not used, wait $t_{WD\_PROG\_FL}$ or $t_{WD\_PROG\_EE}$, respectively, before transmitting the next instruction. See Table 30 on page 63 for the $t_{WD\_PROG\_FL}$ and $t_{WD\_PROG\_EE}$ values. In an erased device, no $FFs in the data file(s) need to be programmed.
6. Any memory location can be verified by using the Read instruction, which returns the content at the selected address at the serial output MISO (PB1) pin.
7. At the end of the programming session, $\overline{\text{RESET}}$ can be set high to commence normal operation.
8. Power-off sequence (if needed):

   Set $\overline{\text{RESET}}$ to “1”.

   Turn V_{CC} power off.

Low-voltage Serial Programming Characteristics

Figure 35. Low-voltage Serial Programming Timing

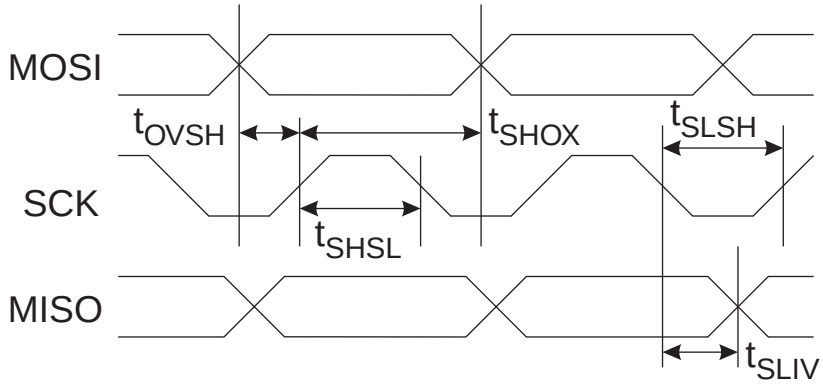


Table 28. Low-voltage Serial Programming Characteristics, T_A = -40°C to 85°C, V_{CC} = 2.7 - 5.5V (Unless Otherwise Noted)

Symbol	Parameter	Min	Typ	Max	Units
$1/t_{CLCL}$	RC Oscillator Frequency (V_{CC} = 2.7 - 5.5V)	0.8	1.6		MHz
t_{CLCL}	RC Oscillator Period (V_{CC} = 2.7 - 5.5V)		625.0	1250.0	ns
t_{SHSL}	SCK Pulse Width High	2.0 t_{CLCL}			ns
t_{SLSH}	SCK Pulse Width Low	2.0 t_{CLCL}			ns
t_{OVSH}	MOSI Setup to SCK High	t_{CLCL}			ns
t_{SHOX}	MOSI Hold after SCK High	2.0 t_{CLCL}			ns
t_{SLIV}	SCK Low to MISO Valid	10.0	16.0	32.0	ns

Table 29. Minimum Wait Delay after the Chip Erase Instruction

Symbol	Minimum Wait Delay
t_{WD_ERASE}	8.2 ms

Table 30. Minimum Wait Delay after Writing a Flash or EEPROM Location

Symbol	Minimum Wait Delay
t_{WD_FLASH}	4.1 ms
t_{WD_EEPROM}	8.2 ms

Typical Characteristics

The following charts show typical behavior. These data are characterized but not tested. All current consumption measurements are performed with all I/O pins configured as inputs and with internal pull-ups enabled.

The current consumption is a function of several factors such as: Operating voltage, operating frequency, loading of I/O pins, switching rate of I/O pins, code executed and ambient temperature. The dominating factors are operating voltage and frequency.

The current drawn from capacitive loaded pins may be estimated (for one pin) as $C_L \bullet V_{CC} \bullet f$ where C_L = load capacitance, V_{CC} = operating voltage and f = average switching frequency of I/O pin.

The difference between current consumption in Power-down mode with Watchdog Timer enabled and Power-down mode with Watchdog Timer disabled represents the differential current drawn by the Watchdog Timer.

Figure 36. Active Supply Current vs. V_{CC}

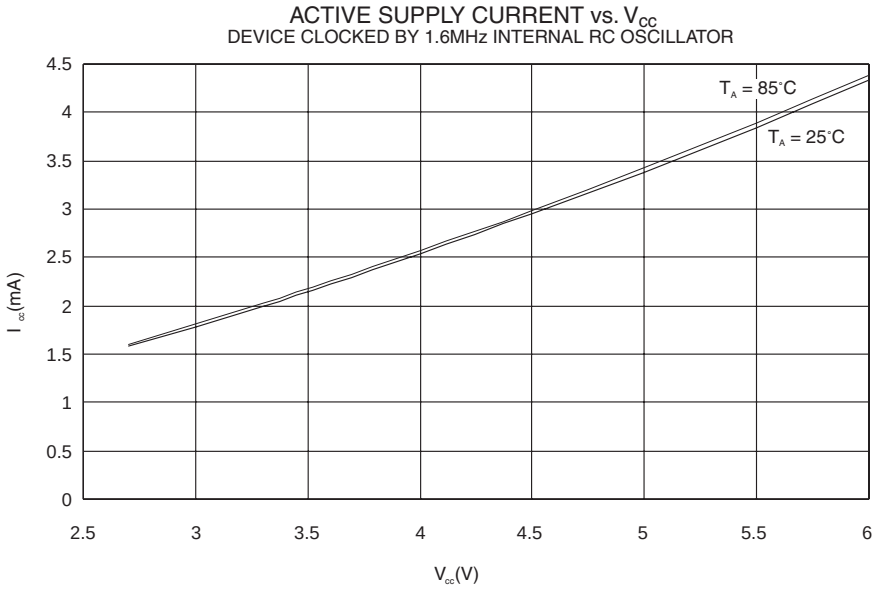


Figure 49. I/O Pin Source Current vs. Output Voltage

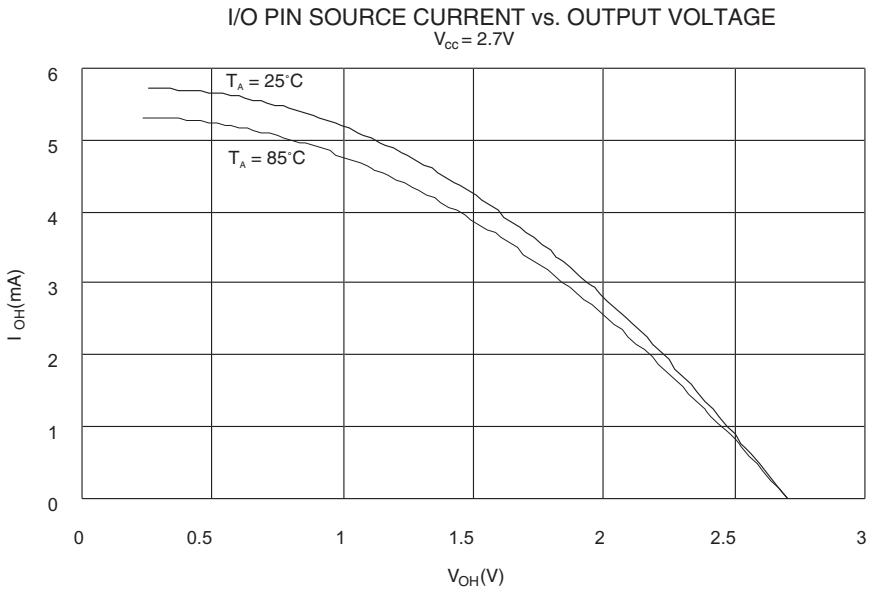
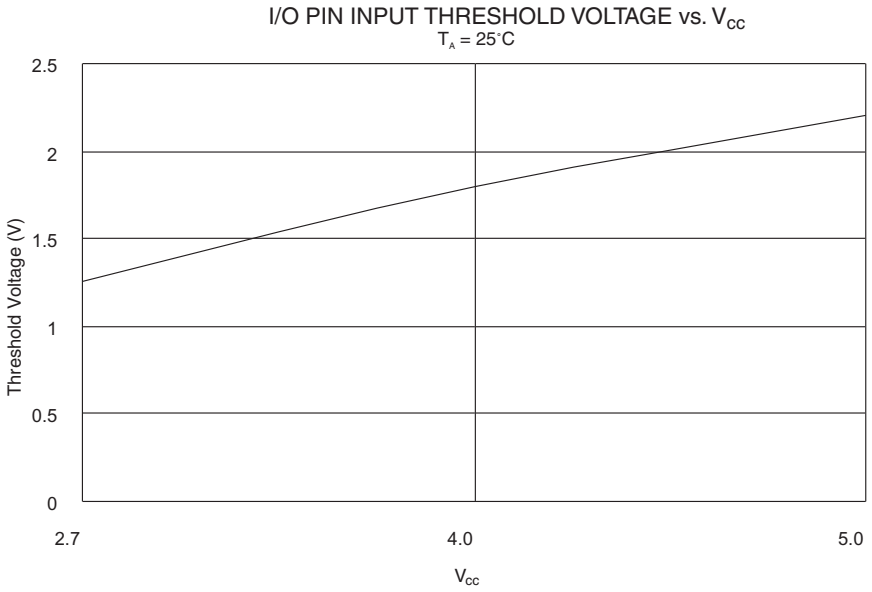


Figure 50. I/O Pin Input Threshold Voltage vs. V_{CC}

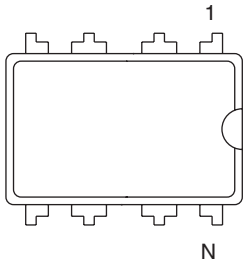


ATtiny15L Register Summary

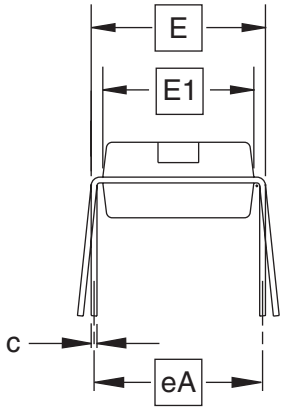
Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
$3F	SREG	I	T	H	S	V	N	Z	C	page 11
$3E	Reserved									
$3C	Reserved									
$3B	GIMSK	-	INT0	PCIE	-	-	-	-	-	page 19
$3A	GIFR	-	INTF0	PCIF	-	-	-	-	-	page 20
$39	TIMSK	-	OCIE1A	-	-	-	TOIE1	TOIE0	-	page 20
$38	TIFR	-	OCF1A	-	-	-	TOV1	TOV0	-	page 21
$37	Reserved									
$36	Reserved									
$35	MCUCR	-	PUD	SE	SM1	SM0	-	ISC01	ISC00	page 22
$34	MCUSR	-	-	-	-	WDRF	BORF	EXTRF	PORF	page 18
$33	TCCR0	-	-	-	-	-	CS02	CS01	CS00	page 27
$32	TCNT0	Timer/Counter0 (8-Bit)								page 28
$31	OSCCAL	Oscillator Calibration Register								page 24
$30	TCCR1	CTC1	PWM1	COM1A1	COM1A0	CS13	CS12	CS11	CS10	page 29
$2F	TCNT1	Timer/Counter1 (8-Bit)								page 30
$2E	OCR1A	Timer/Counter1 Output Compare Register A (8-Bit)								page 31
$2D	OCR1B	Timer/Counter1 Output Compare Register B (8-Bit)								page 32
$2C	SFIOR	-	-	-	-	-	FOC1A	PSR1	PSR0	page 26
$2B	Reserved									
$2A	Reserved									
$29	Reserved									
$28	Reserved									
$27	Reserved									
$26	Reserved									
$25	Reserved									
$24	Reserved									
$23	Reserved									
$22	Reserved									
$21	WDTCR	-	-	-	WDTOE	WDE	WDP2	WDP1	WDP0	page 34
$20	Reserved									
$1F	Reserved									
$1E	EEAR	-	-	EEAR5	EEAR4	EEAR3	EEAR2	EEAR1	EEAR0	page 36
$1D	EEDR	EEPROM Data Register (8-Bit)								page 36
$1C	EECR	-	-	-	-	EERIE	EEMWE	EEWE	EERE	page 37
$1B	Reserved									
$1A	Reserved									
$19	Reserved									
$18	PORTB	-	-	-	PORTB4	PORTB3	PORTB2	PORTB1	PORTB0	page 51
$17	DDRB	-	-	DDB5	DDB4	DDB3	DDB2	DDB1	DDB0	page 51
$16	PINB	-	-	PINB5	PINB4	PINB3	PINB2	PINB1	PINB0	page 52
$15	Reserved									
$14	Reserved									
$13	Reserved									
$12	Reserved									
$11	Reserved									
$10	Reserved									
$0F	Reserved									
$0E	Reserved									
$0D	Reserved									
$0C	Reserved									
$0B	Reserved									
$0A	Reserved									
$09	Reserved									
$08	ACSR	ACD	ACBG	ACO	ACI	ACIE	-	ACIS1	ACIS0	page 39
$07	ADMUX	REFS1	REFS0	ADLAR	-	-	MUX2	MUX1	MUX0	page 46
$06	ADCSR	ADEN	ADSC	ADFR	ADIF	ADIE	ADPS2	ADPS1	ADPS0	page 47
$05	ADCH	ADC Data Register High Byte								page 49
$04	ADCL	ADC Data Register Low Byte								page 49
...	Reserved									
$00	Reserved									

Packaging Information

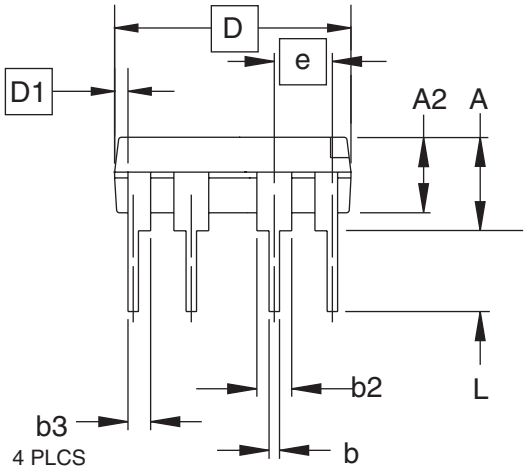
8P3



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = inches)

SYMBOL	MIN	NOM	MAX	NOTE
A			0.210	2
A2	0.115	0.130	0.195	
b	0.014	0.018	0.022	5
b2	0.045	0.060	0.070	6
b3	0.030	0.039	0.045	6
c	0.008	0.010	0.014	
D	0.355	0.365	0.400	3
D1	0.005			3
E	0.300	0.310	0.325	4
E1	0.240	0.250	0.280	3
e	0.100 BSC			
eA	0.300 BSC			4
L	0.115	0.130	0.150	2

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

01/09/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8P3**, 8-lead, 0.300" Wide Body, Plastic Dual In-line Package (PDIP)	8P3	B