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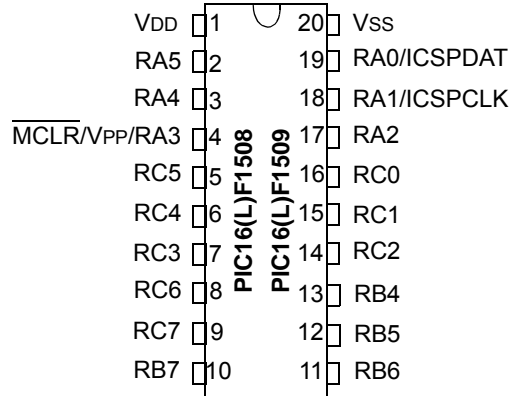
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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 12x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1508-e-so

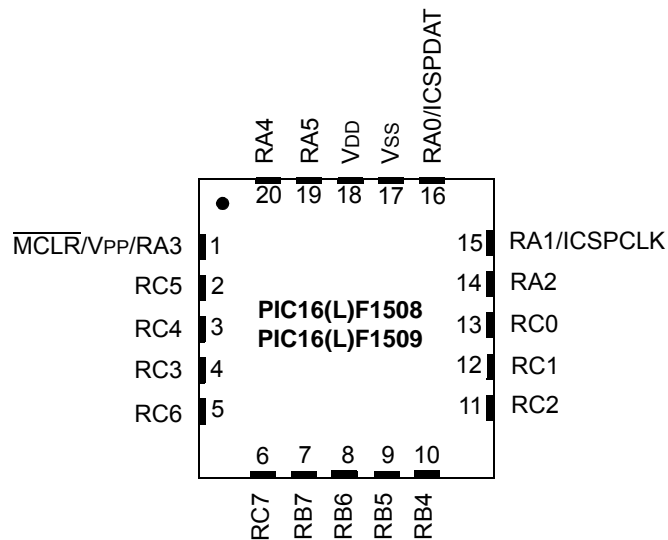
PIN DIAGRAMS

20-pin PDIP, SOIC, SSOP



Note: See Table 1 for location of all peripheral functions.

20-pin QFN, UQFN



Note 1: See Table 1 for location of all peripheral functions.

2: It is recommended that the exposed bottom pad be connected to Vss.

PIC16(L)F1508/9

TABLE 3-9: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 31											
F8Ch — FE3h	—	Unimplemented								—	—
FE4h	STATUS_SHAD	—	—	—	—	—	Z_SHAD	DC_SHAD	C_SHAD	---- -xxx	---- -uuu
FE5h	WREG_SHAD	Working Register Shadow								xxxx xxxx	uuuu uuuu
FE6h	BSR_SHAD	—	—	—	Bank Select Register Shadow					---x xxxx	---u uuuu
FE7h	PCLATH_SHAD	—	Program Counter Latch High Register Shadow							-xxx xxxx	uuuu uuuu
FE8h	FSR0L_SHAD	Indirect Data Memory Address 0 Low Pointer Shadow								xxxx xxxx	uuuu uuuu
FE9h	FSR0H_SHAD	Indirect Data Memory Address 0 High Pointer Shadow								xxxx xxxx	uuuu uuuu
FEAh	FSR1L_SHAD	Indirect Data Memory Address 1 Low Pointer Shadow								xxxx xxxx	uuuu uuuu
FEBh	FSR1H_SHAD	Indirect Data Memory Address 1 High Pointer Shadow								xxxx xxxx	uuuu uuuu
FECh	—	Unimplemented								—	—
FEDh	STKPTR	—	—	—	Current Stack Pointer					---1 1111	---1 1111
FEEh	TOSL	Top-of-Stack Low byte								xxxx xxxx	uuuu uuuu
FEFh	TOSH	—	Top-of-Stack High byte							-xxx xxxx	-uuu uuuu

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: PIC16F1508/9 only.

Note 2: Unimplemented, read as '1'.

5.3.5 CLOCK SWITCHING BEFORE SLEEP

When clock switching from an old clock to a new clock is requested just prior to entering Sleep mode, it is necessary to confirm that the switch is complete before the `SLEEP` instruction is executed. Failure to do so may result in an incomplete switch and consequential loss of the system clock altogether. Clock switching is confirmed by monitoring the clock status bits in the `OSCSTAT` register. Switch confirmation can be accomplished by sensing that the ready bit for the new clock is set or the ready bit for the old clock is cleared. For example, when switching between the internal oscillator with the PLL and the internal oscillator without the PLL, monitor the `PLLR` bit. When `PLLR` is set, the switch to 32 MHz operation is complete. Conversely, when `PPLR` is cleared, the switch from 32 MHz operation to the selected internal clock is complete.

5.4 Two-Speed Clock Start-up Mode

Two-Speed Start-up mode provides additional power savings by minimizing the latency between external oscillator start-up and code execution. In applications that make heavy use of the Sleep mode, Two-Speed Start-up will remove the external oscillator start-up time from the time spent awake and can reduce the overall power consumption of the device. This mode allows the application to wake-up from Sleep, perform a few instructions using the `INTOSC` internal oscillator block as the clock source and go back to Sleep without waiting for the external oscillator to become stable.

Two-Speed Start-up provides benefits when the oscillator module is configured for LP, XT, or HS modes. The Oscillator Start-up Timer (OST) is enabled for these modes and must count 1024 oscillations before the oscillator can be used as the system clock source.

If the oscillator module is configured for any mode other than LP, XT or HS mode, then Two-Speed Start-up is disabled. This is because the external clock oscillator does not require any stabilization time after POR or an exit from Sleep.

If the OST count reaches 1024 before the device enters Sleep mode, the `OSTS` bit of the `OSCSTAT` register is set and program execution switches to the external oscillator. However, the system may never operate from the external oscillator if the time spent awake is very short.

Note: Executing a <code>SLEEP</code> instruction will abort the oscillator start-up time and will cause the <code>OSTS</code> bit of the <code>OSCSTAT</code> register to remain clear.
--

FIGURE 6-3: RESET START-UP SEQUENCE

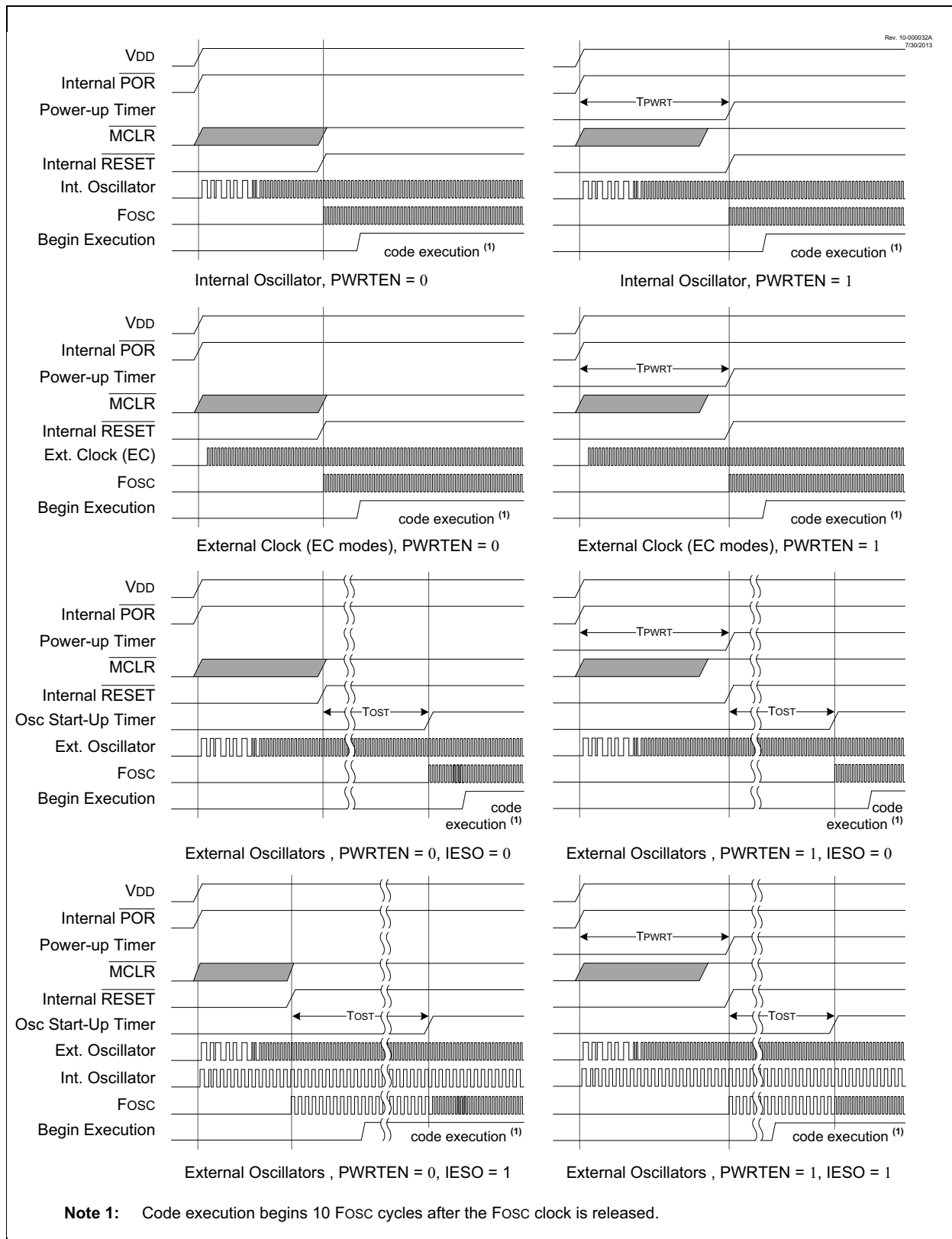


TABLE 9-3: SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON	—	IRCF<3:0>				—	SCS<1:0>		59
PCON	STKOVF	STKUNF	—	RWD \overline{T}	RMCLR	R \overline{I}	POR	BOR	68
STATUS	—	—	—	T \overline{O}	P \overline{D}	Z	DC	C	19
WDTCON	—	—	WDTPS<4:0>					SWDTEN	88

Legend: x = unknown, u = unchanged, — = unimplemented locations read as '0'. Shaded cells are not used by Watchdog Timer.

TABLE 9-4: SUMMARY OF CONFIGURATION WORD WITH WATCHDOG TIMER

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	—	—	FCMEN	IESO	CLKOUTEN	BOREN<1:0>		—	41
	7:0	CP	MCLRE	PWRT \overline{E}	WDTE<1:0>		FOSC<2:0>			

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Watchdog Timer.

FIGURE 15-4: ANALOG INPUT MODEL

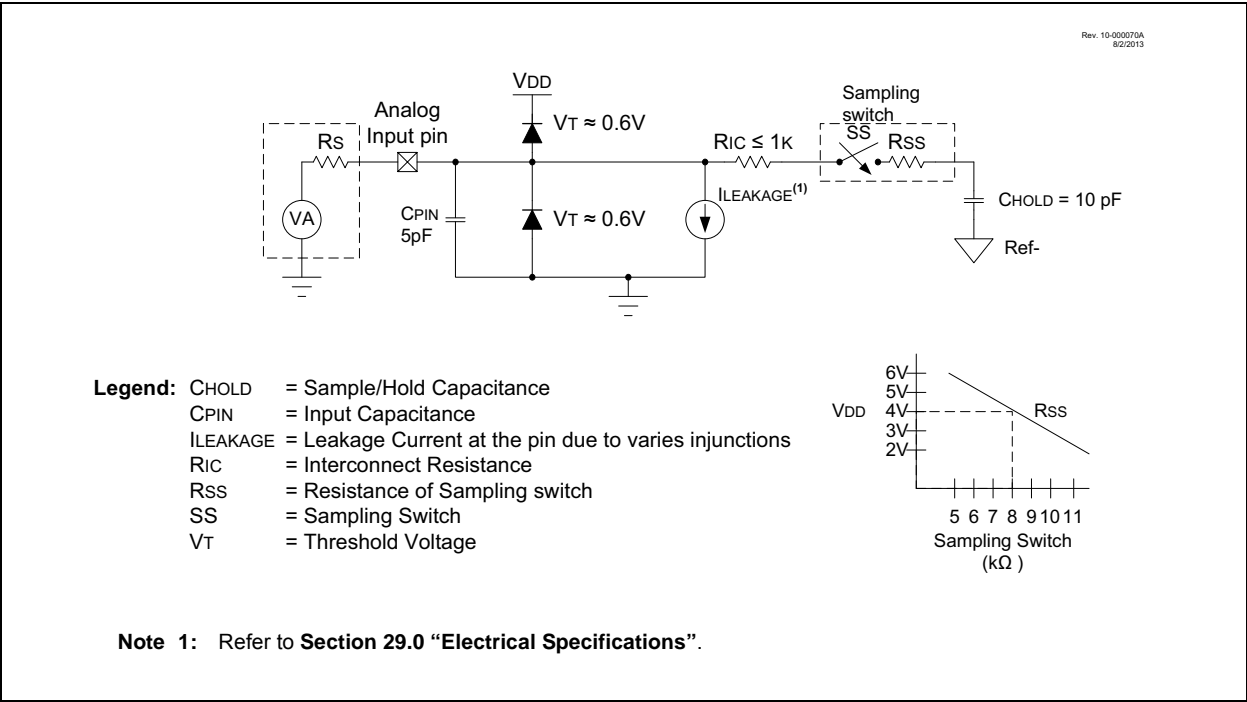
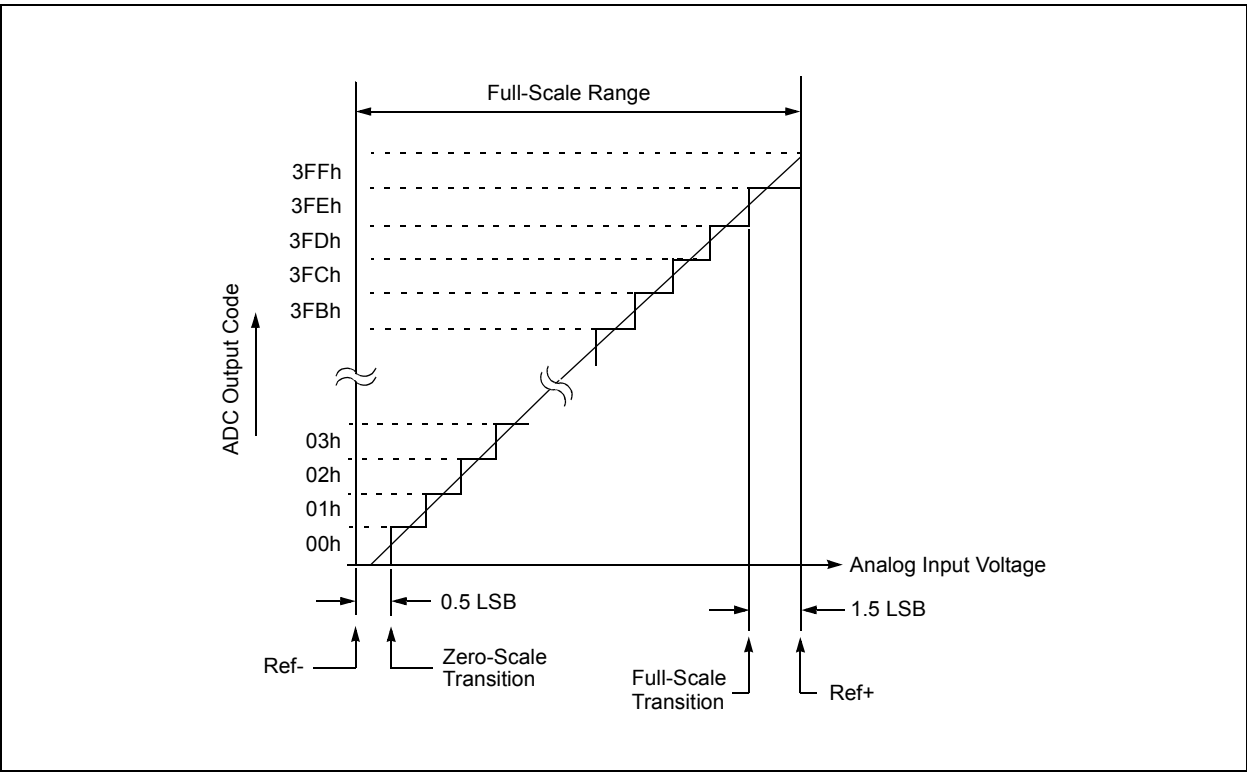


FIGURE 15-5: ADC TRANSFER FUNCTION



17.8 Register Definitions: Comparator Control

REGISTER 17-1: CMxCON0: COMPARATOR Cx CONTROL REGISTER 0

R/W-0/0	R-0/0	R/W-0/0	R/W-0/0	U-0	R/W-1/1	R/W-0/0	R/W-0/0
CxON	CxOUT	CxOE	CxPOL	—	CxSP	CxHYS	CxSYNC
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

- bit 7 **CxON:** Comparator Enable bit
 1 = Comparator is enabled
 0 = Comparator is disabled and consumes no active power
- bit 6 **CxOUT:** Comparator Output bit
If CxPOL = 1 (inverted polarity):
 1 = CxVP < CxVN
 0 = CxVP > CxVN
If CxPOL = 0 (non-inverted polarity):
 1 = CxVP > CxVN
 0 = CxVP < CxVN
- bit 5 **CxOE:** Comparator Output Enable bit
 1 = CxOUT is present on the CxOUT pin. Requires that the associated TRIS bit be cleared to actually drive the pin. Not affected by CxON.
 0 = CxOUT is internal only
- bit 4 **CxPOL:** Comparator Output Polarity Select bit
 1 = Comparator output is inverted
 0 = Comparator output is not inverted
- bit 3 **Unimplemented:** Read as '0'
- bit 2 **CxSP:** Comparator Speed/Power Select bit
 1 = Comparator mode in normal power, higher speed
 0 = Comparator mode in low-power, low-speed
- bit 1 **CxHYS:** Comparator Hysteresis Enable bit
 1 = Comparator hysteresis enabled
 0 = Comparator hysteresis disabled
- bit 0 **CxSYNC:** Comparator Output Synchronous Mode bit
 1 = Comparator output to Timer1 and I/O pin is synchronous to changes on Timer1 clock source. Output updated on the falling edge of Timer1 clock source.
 0 = Comparator output to Timer1 and I/O pin is asynchronous

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REGISTER 17-2: CMxCON1: COMPARATOR Cx CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
CxINTP	CxINTN	CxPCH<1:0>		—	CxNCH<2:0>		
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
 '1' = Bit is set '0' = Bit is cleared

- bit 7 **CxINTP:** Comparator Interrupt on Positive Going Edge Enable bits
 1 = The CxIF interrupt flag will be set upon a positive going edge of the CxOUT bit
 0 = No interrupt flag will be set on a positive going edge of the CxOUT bit
- bit 6 **CxINTN:** Comparator Interrupt on Negative Going Edge Enable bits
 1 = The CxIF interrupt flag will be set upon a negative going edge of the CxOUT bit
 0 = No interrupt flag will be set on a negative going edge of the CxOUT bit
- bit 5-4 **CxPCH<1:0>:** Comparator Positive Input Channel Select bits
 11 = CxVP connects to Vss
 10 = CxVP connects to FVR Voltage Reference
 01 = CxVP connects to DAC Voltage Reference
 00 = CxVP connects to CxIN+ pin
- bit 3 **Unimplemented:** Read as '0'
- bit 2-0 **CxNCH<2:0>:** Comparator Negative Input Channel Select bits
 111 = Reserved
 110 = Reserved
 101 = Reserved
 100 = CxVN connects to FVR Voltage reference
 011 = CxVN connects to CxIN3- pin
 010 = CxVN connects to CxIN2- pin
 001 = CxVN connects to CxIN1- pin
 000 = CxVN connects to CxIN0- pin

REGISTER 17-3: CMOUT: COMPARATOR OUTPUT REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R-0/0	R-0/0
—	—	—	—	—	—	MC2OUT	MC1OUT
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
 '1' = Bit is set '0' = Bit is cleared

- bit 7-2 **Unimplemented:** Read as '0'
- bit 1 **MC2OUT:** Mirror Copy of C2OUT bit
- bit 0 **MC1OUT:** Mirror Copy of C1OUT bit

FIGURE 21-22: I²C SLAVE, 10-BIT ADDRESS, TRANSMISSION (SEN = 0, AHEN = 0, DHEN = 0)

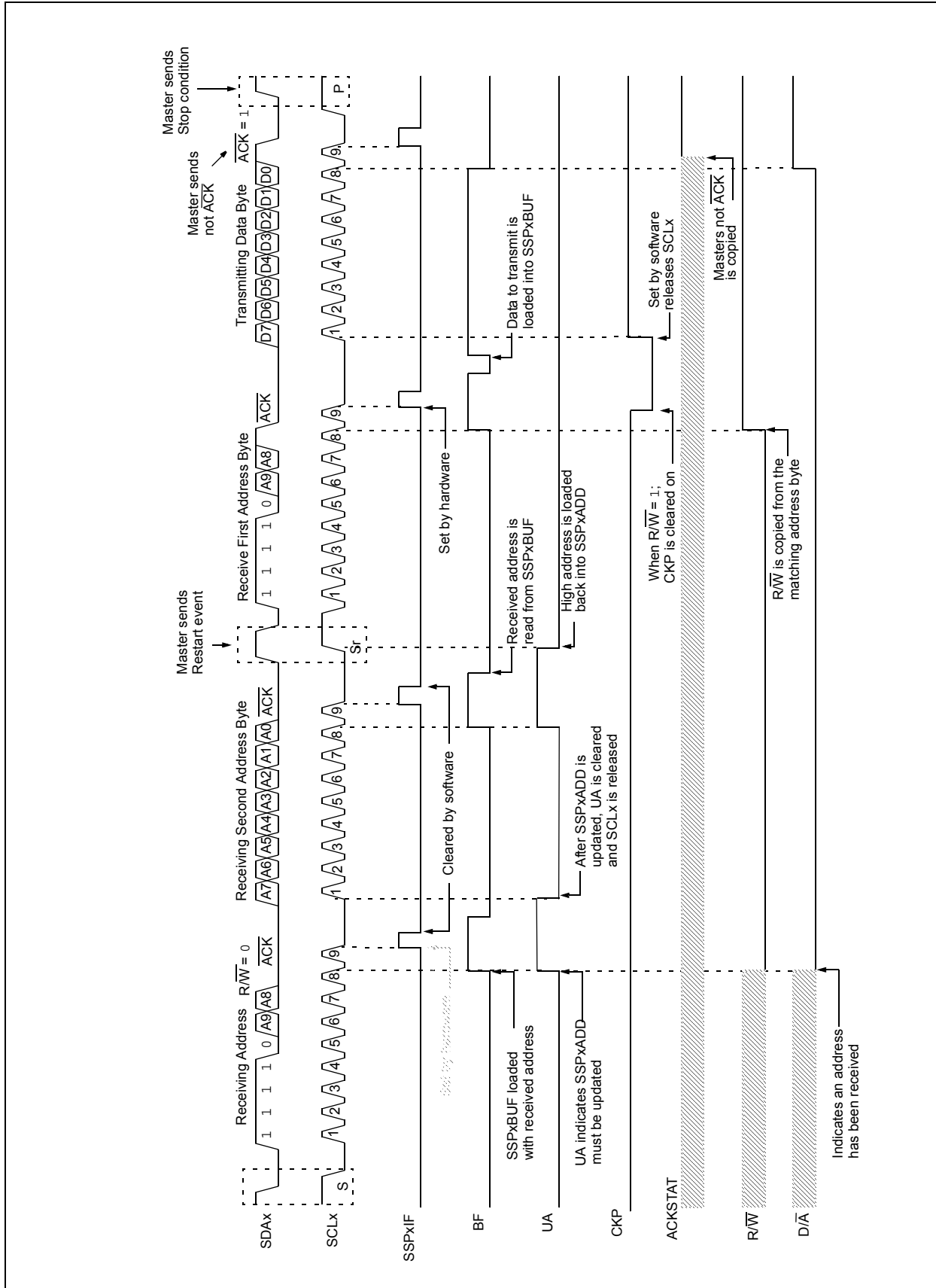
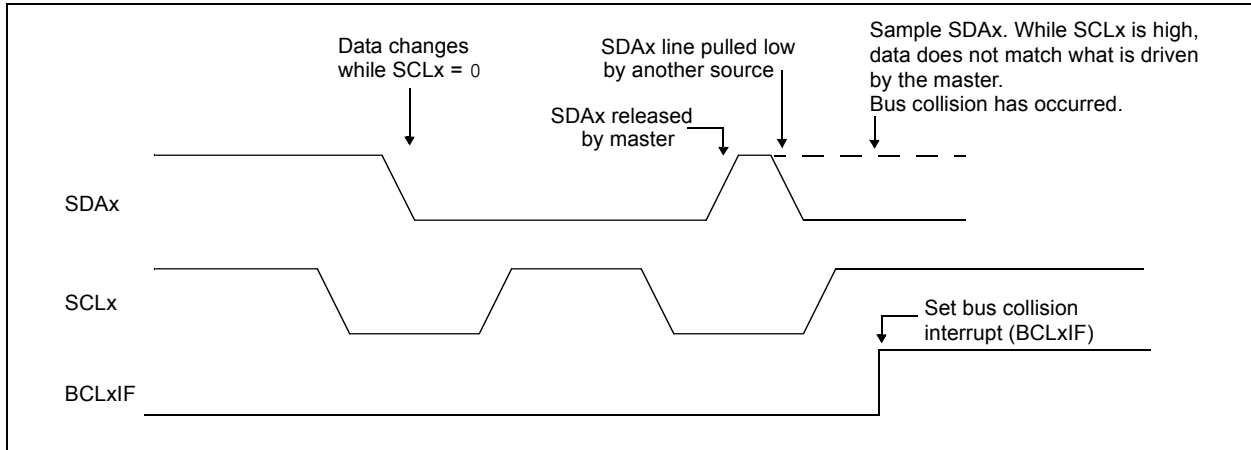


FIGURE 21-32: BUS COLLISION TIMING FOR TRANSMIT AND ACKNOWLEDGE



22.0 ENHANCED UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (EUSART)

The Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) module is a serial I/O communications peripheral. It contains all the clock generators, shift registers and data buffers necessary to perform an input or output serial data transfer independent of device program execution. The EUSART, also known as a Serial Communications Interface (SCI), can be configured as a full-duplex asynchronous system or half-duplex synchronous system. Full-Duplex mode is useful for communications with peripheral systems, such as CRT terminals and personal computers. Half-Duplex Synchronous mode is intended for communications with peripheral devices, such as A/D or D/A integrated circuits, serial EEPROMs or other microcontrollers. These devices typically do not have internal clocks for baud rate generation and require the external clock signal provided by a master synchronous device.

The EUSART module includes the following capabilities:

- Full-duplex asynchronous transmit and receive
- Two-character input buffer
- One-character output buffer
- Programmable 8-bit or 9-bit character length
- Address detection in 9-bit mode
- Input buffer overrun error detection
- Received character framing error detection
- Half-duplex synchronous master
- Half-duplex synchronous slave
- Programmable clock polarity in synchronous modes
- Sleep operation

The EUSART module implements the following additional features, making it ideally suited for use in Local Interconnect Network (LIN) bus systems:

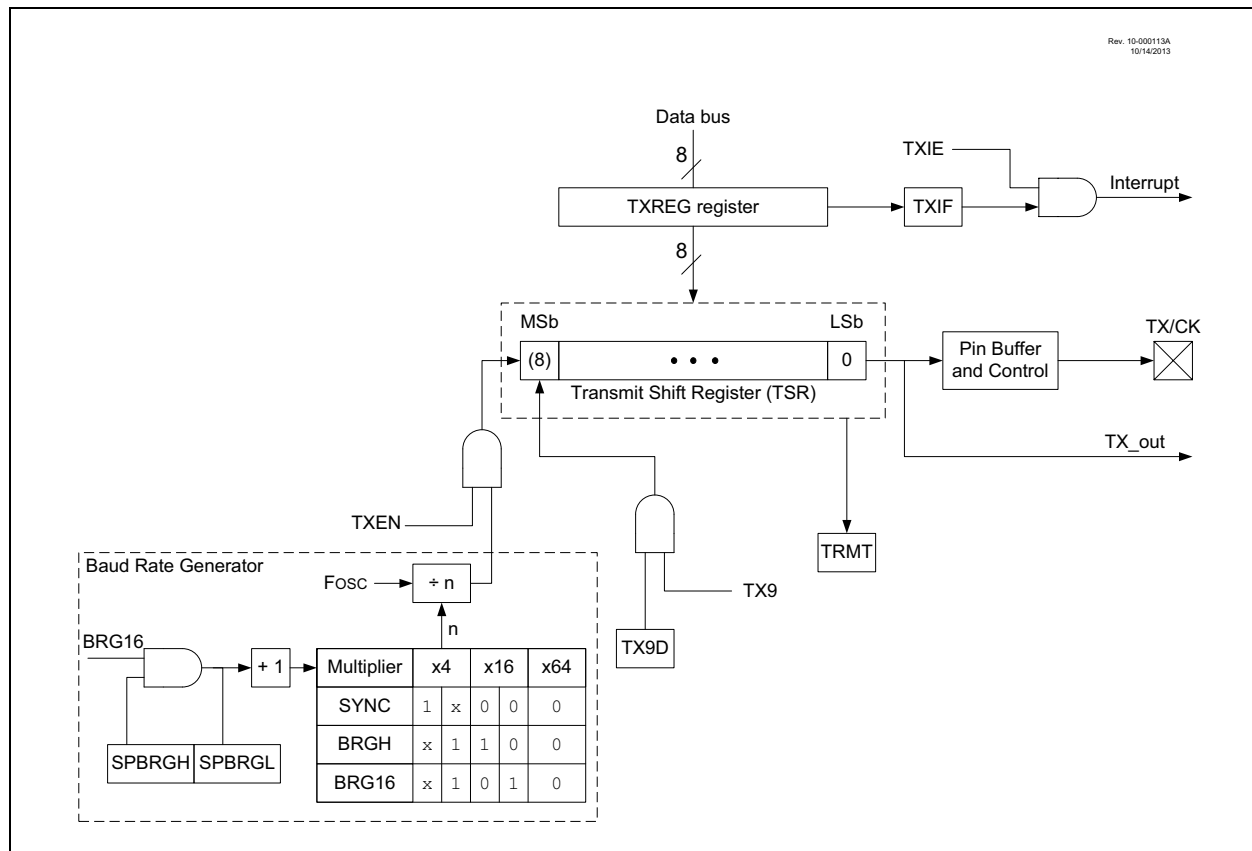
- Automatic detection and calibration of the baud rate
- Wake-up on Break reception
- 13-bit Break character transmit

Block diagrams of the EUSART transmitter and receiver are shown in Figure 22-1 and Figure 22-2.

The EUSART transmit output (TX_out) is available to the TX/CK pin and internally to the following peripherals:

- Configurable Logic Cell (CLC)

FIGURE 22-1: EUSART TRANSMIT BLOCK DIAGRAM



22.1.2.8 Asynchronous Reception Set-up:

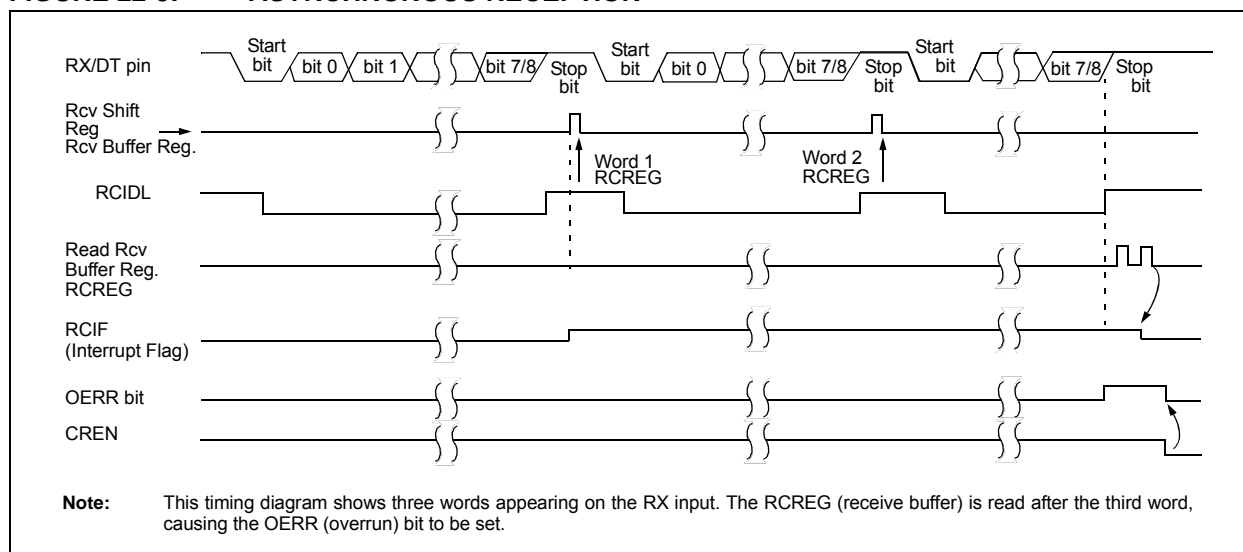
1. Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see **Section 22.4 “EUSART Baud Rate Generator (BRG)”**).
2. Clear the ANSEL bit for the RX pin (if applicable).
3. Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
4. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
5. If 9-bit reception is desired, set the RX9 bit.
6. Enable reception by setting the CREN bit.
7. The RCIF interrupt flag bit will be set when a character is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE interrupt enable bit was also set.
8. Read the RCSTA register to get the error flags and, if 9-bit data reception is enabled, the ninth data bit.
9. Get the received eight Least Significant data bits from the receive buffer by reading the RCREG register.
10. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.

22.1.2.9 9-bit Address Detection Mode Set-up

This mode would typically be used in RS-485 systems. To set up an Asynchronous Reception with Address Detect Enable:

1. Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see **Section 22.4 “EUSART Baud Rate Generator (BRG)”**).
2. Clear the ANSEL bit for the RX pin (if applicable).
3. Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
4. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
5. Enable 9-bit reception by setting the RX9 bit.
6. Enable address detection by setting the ADDEN bit.
7. Enable reception by setting the CREN bit.
8. The RCIF interrupt flag bit will be set when a character with the ninth bit set is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE interrupt enable bit was also set.
9. Read the RCSTA register to get the error flags. The ninth data bit will always be set.
10. Get the received eight Least Significant data bits from the receive buffer by reading the RCREG register. Software determines if this is the device's address.
11. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.
12. If the device has been addressed, clear the ADDEN bit to allow all received data into the receive buffer and generate interrupts.

FIGURE 22-5: ASYNCHRONOUS RECEPTION



22.2 Clock Accuracy with Asynchronous Operation

The factory calibrates the internal oscillator block output (INTOSC). However, the INTOSC frequency may drift as V_{DD} or temperature changes, and this directly affects the asynchronous baud rate.

The Auto-Baud Detect feature (see **Section 22.4.1 “Auto-Baud Detect”**) can be used to compensate for changes in the INTOSC frequency.

There may not be fine enough resolution when adjusting the Baud Rate Generator to compensate for a gradual change in the peripheral clock frequency.

22.4.1 AUTO-BAUD DETECT

The EUSART module supports automatic detection and calibration of the baud rate.

In the Auto-Baud Detect (ABD) mode, the clock to the BRG is reversed. Rather than the BRG clocking the incoming RX signal, the RX signal is timing the BRG. The Baud Rate Generator is used to time the period of a received 55h (ASCII “U”) which is the Sync character for the LIN bus. The unique feature of this character is that it has five rising edges including the Stop bit edge.

Setting the ABDEN bit of the BAUDCON register starts the auto-baud calibration sequence (Figure 22-6). While the ABD sequence takes place, the EUSART state machine is held in Idle. On the first rising edge of the receive line, after the Start bit, the SPBRG begins counting up using the BRG counter clock as shown in Table 22-6. The fifth rising edge will occur on the RX pin at the end of the eighth bit period. At that time, an accumulated value totaling the proper BRG period is left in the SPBRGH, SPBRGL register pair, the ABDEN bit is automatically cleared and the RCIF interrupt flag is set. The value in the RCREG needs to be read to clear the RCIF interrupt. RCREG content should be discarded. When calibrating for modes that do not use the SPBRGH register the user can verify that the SPBRGL register did not overflow by checking for 00h in the SPBRGH register.

The BRG auto-baud clock is determined by the BRG16 and BRGH bits as shown in Table 22-6. During ABD, both the SPBRGH and SPBRGL registers are used as a 16-bit counter, independent of the BRG16 bit setting. While calibrating the baud rate period, the SPBRGH

and SPBRGL registers are clocked at 1/8th the BRG base clock rate. The resulting byte measurement is the average bit time when clocked at full speed.

Note 1: If the WUE bit is set with the ABDEN bit, auto-baud detection will occur on the byte following the Break character (see **Section 22.4.3 “Auto-Wake-up on Break”**).

2: It is up to the user to determine that the incoming character baud rate is within the range of the selected BRG clock source. Some combinations of oscillator frequency and EUSART baud rates are not possible.

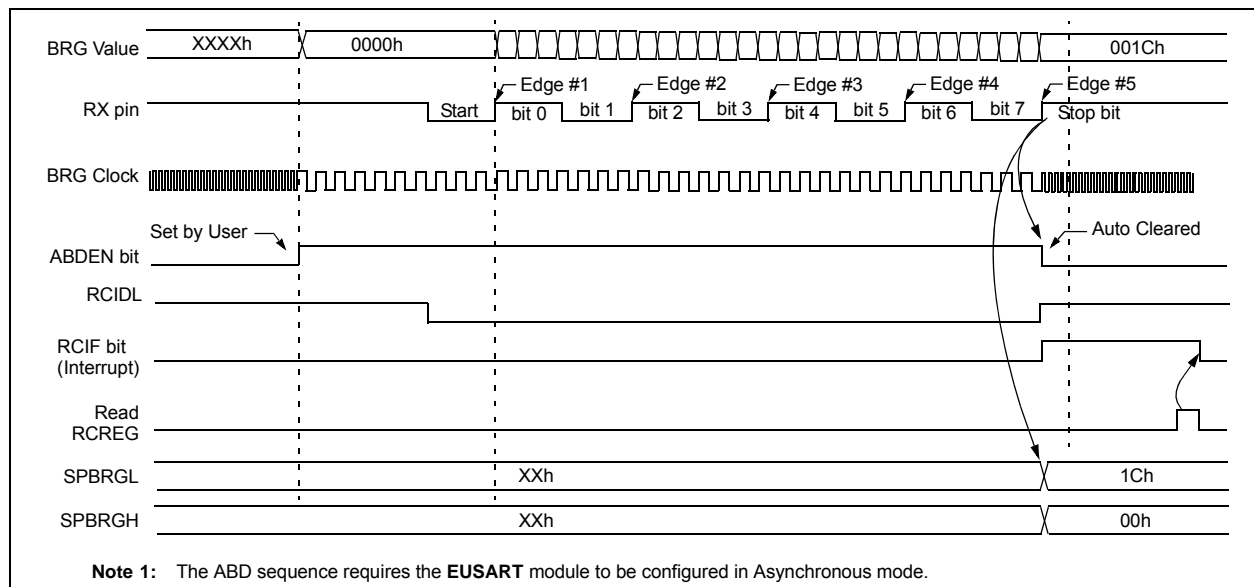
3: During the auto-baud process, the auto-baud counter starts counting at 1. Upon completion of the auto-baud sequence, to achieve maximum accuracy, subtract 1 from the SPBRGH:SPBRGL register pair.

TABLE 22-6: BRG COUNTER CLOCK RATES

BRG16	BRGH	BRG Base Clock	BRG ABD Clock
0	0	Fosc/64	Fosc/512
0	1	Fosc/16	Fosc/128
1	0	Fosc/16	Fosc/128
1	1	Fosc/4	Fosc/32

Note: During the ABD sequence, SPBRGL and SPBRGH registers are both used as a 16-bit counter, independent of BRG16 setting.

FIGURE 22-6: AUTOMATIC BAUD RATE CALIBRATION



23.0 PULSE-WIDTH MODULATION (PWM) MODULE

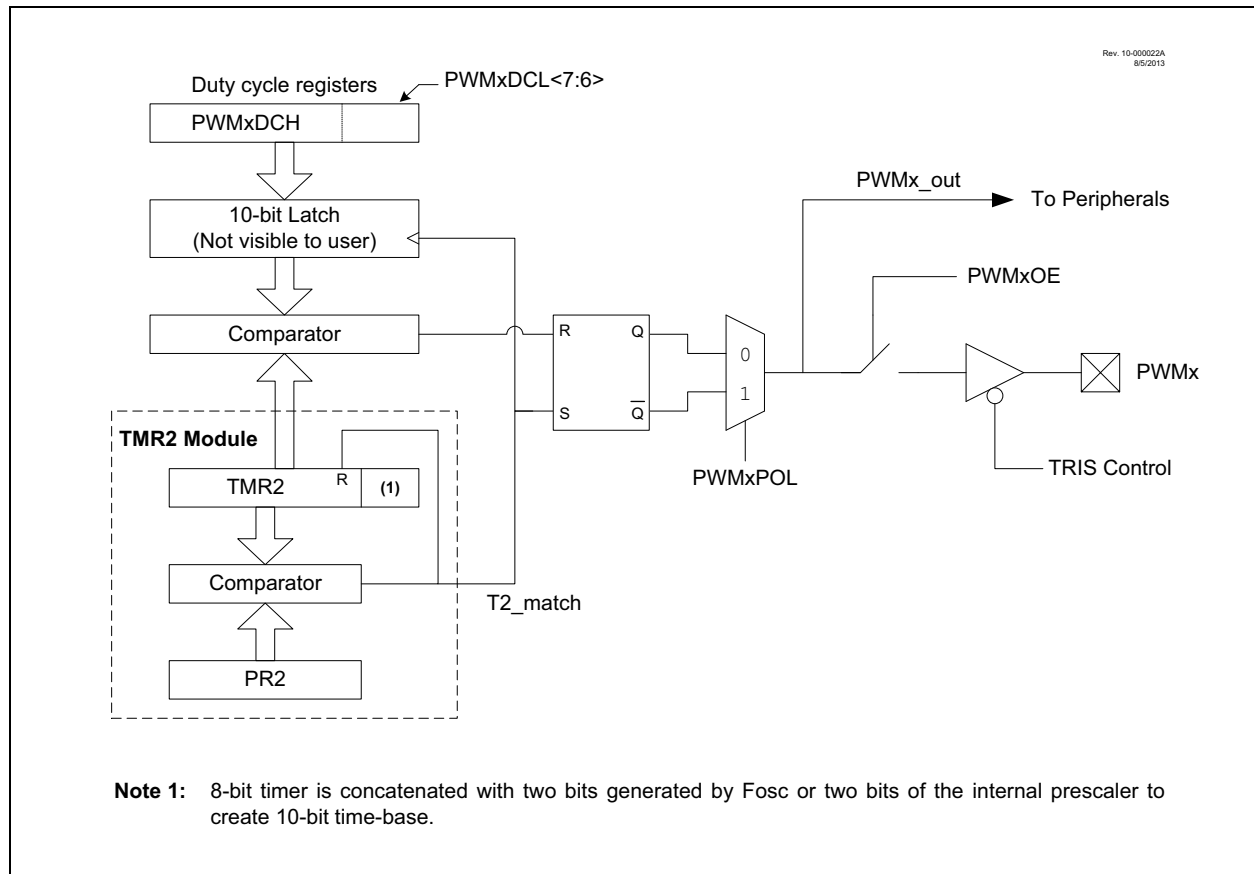
The PWM module generates a Pulse-Width Modulated signal determined by the duty cycle, period, and resolution that are configured by the following registers:

- PR2
- T2CON
- PWMxDCH
- PWMxDCL
- PWMxCON

Figure 23-1 shows a simplified block diagram of PWM operation.

For a step-by-step procedure on how to set up this module for PWM operation, refer to **Section 23.1.9 “Setup for PWM Operation using PWMx Pins”**.

FIGURE 23-1: SIMPLIFIED PWM BLOCK DIAGRAM



REGISTER 26-3: CWGxCON2: CWG CONTROL REGISTER 2

R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
GxASE	GxARSEN	—	—	GxASDSC2	GxASDSC1	GxASDSFLT	GxASDSCLC2
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

q = Value depends on condition

- bit 7 **GxASE:** Auto-Shutdown Event Status bit
1 = An auto-shutdown event has occurred
0 = No auto-shutdown event has occurred
- bit 6 **GxARSEN:** Auto-Restart Enable bit
1 = Auto-restart is enabled
0 = Auto-restart is disabled
- bit 5-4 **Unimplemented:** Read as '0'
- bit 3 **GxASDSC2:** CWG Auto-shutdown on Comparator C2 Enable bit
1 = Shutdown when Comparator C2 output (C2OUT_async) is high
0 = Comparator C2 output has no effect on shutdown
- bit 2 **GxASDSC1:** CWG Auto-shutdown on Comparator C1 Enable bit
1 = Shutdown when Comparator C1 output (C1OUT_async) is high
0 = Comparator C1 output has no effect on shutdown
- bit 1 **GxASDSFLT:** CWG Auto-shutdown on FLT Enable bit
1 = Shutdown when $\overline{\text{CWG1FLT}}$ input is low
0 = $\overline{\text{CWG1FLT}}$ input has no effect on shutdown
- bit 0 **GxASDSCLC2:** CWG Auto-shutdown on CLC2 Enable bit
1 = Shutdown when CLC2 output (LC2_out) is high
0 = CLC2 output has no effect on shutdown

TABLE 29-3: POWER-DOWN CURRENTS (I_{PD})^(1,2)

PIC16LF1508/9		Operating Conditions: (unless otherwise stated) Low-Power Sleep Mode						
PIC16F1508/9		Low-Power Sleep Mode, VREGPM = 1						
Param. No.	Device Characteristics	Min.	Typ†	Max. +85°C	Max. +125°C	Units	Conditions	
							V _{DD}	Note
D022	Base I _{PD}	—	0.020	1.0	8.0	μA	1.8	WDT, BOR, FVR and SOSC disabled, all Peripherals inactive
		—	0.025	2.0	9.0	μA	3.0	
D022	Base I _{PD}	—	0.25	3.0	10	μA	2.3	WDT, BOR, FVR and SOSC disabled, all Peripherals inactive, Low-Power Sleep mode
		—	0.30	4.0	12	μA	3.0	
		—	0.40	6.0	15	μA	5.0	
D022A	Base I _{PD}	—	9.8	16	18	μA	2.3	WDT, BOR, FVR and SOSC disabled, all Peripherals inactive, Normal Power Sleep mode, VREGPM = 0
		—	10.3	18	20	μA	3.0	
		—	11.5	21	26	μA	5.0	
D023		—	0.26	2.0	9.0	μA	1.8	WDT Current
		—	0.44	3.0	10	μA	3.0	
D023		—	0.43	6.0	15	μA	2.3	WDT Current
		—	0.53	7.0	20	μA	3.0	
		—	0.64	8.0	22	μA	5.0	
D023A		—	15	28	30	μA	1.8	FVR Current
		—	18	30	33	μA	3.0	
D023A		—	18	33	35	μA	2.3	FVR Current
		—	19	35	37	μA	3.0	
		—	20	37	39	μA	5.0	
D024		—	6.0	17	20	μA	3.0	BOR Current
D024		—	7.0	17	30	μA	3.0	BOR Current
		—	8.0	20	40	μA	5.0	
D24A		—	0.1	4.0	10	μA	3.0	LPBOR Current
D24A		—	0.35	5.0	14	μA	3.0	LPBOR Current
		—	0.45	8.0	17	μA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note**
- 1: The peripheral Δ current can be determined by subtracting the base I_{PD} current from this limit. Max. values should be used when calculating total current consumption.
 - 2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{SS}.
 - 3: ADC clock source is FRC.

FIGURE 30-15: I_{DD} TYPICAL, EXTERNAL CLOCK (ECH), HIGH-POWER MODE, PIC16LF1508/9 ONLY

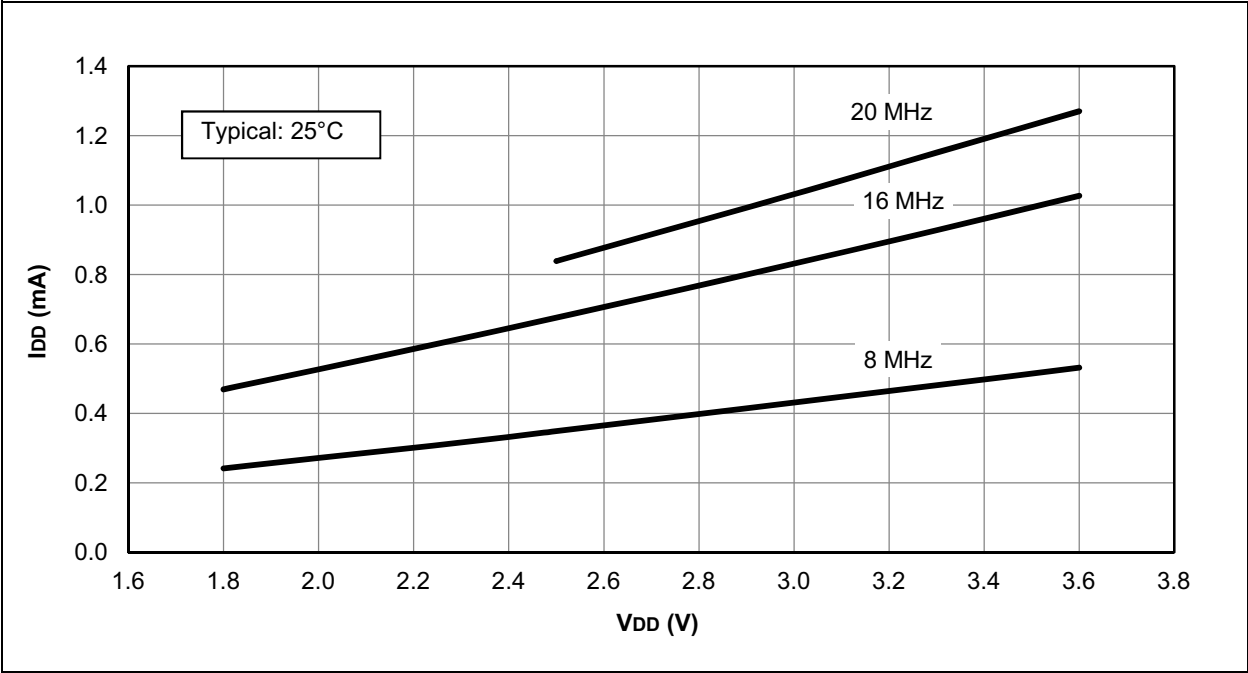


FIGURE 30-16: I_{DD} MAXIMUM, EXTERNAL CLOCK (ECH), HIGH-POWER MODE, PIC16LF1508/9 ONLY

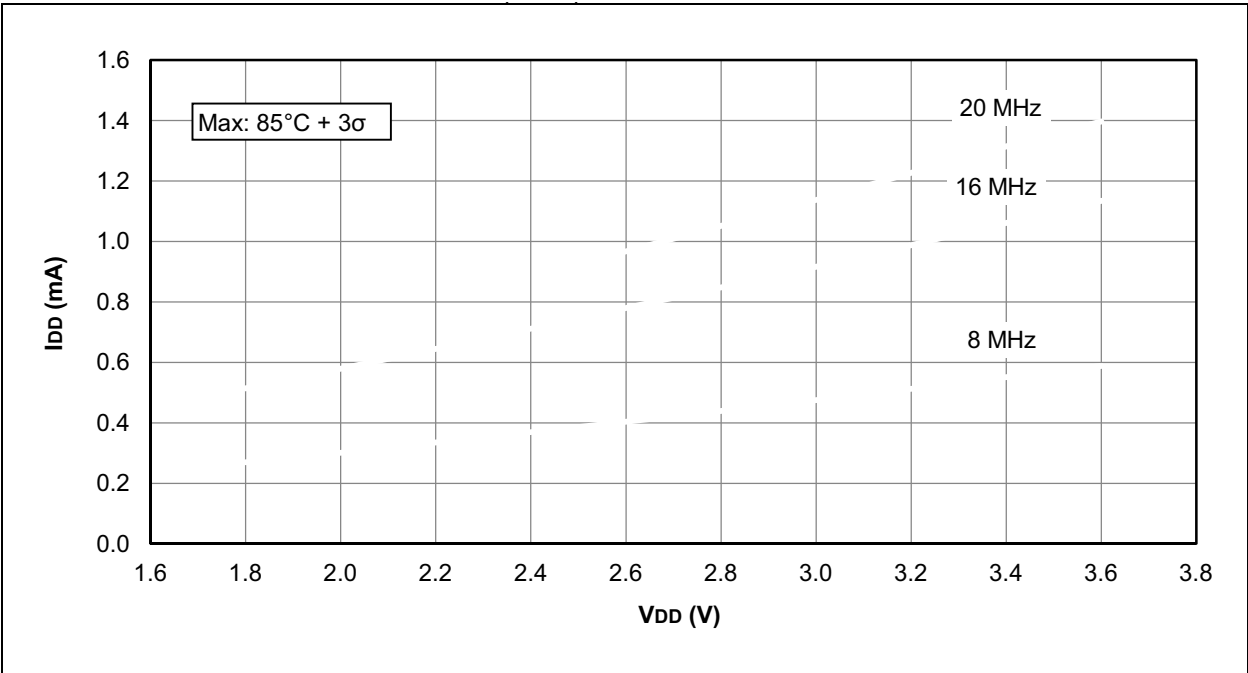


FIGURE 30-31: I_{PD} BASE, LOW-POWER SLEEP MODE, PIC16LF1508/9 ONLY

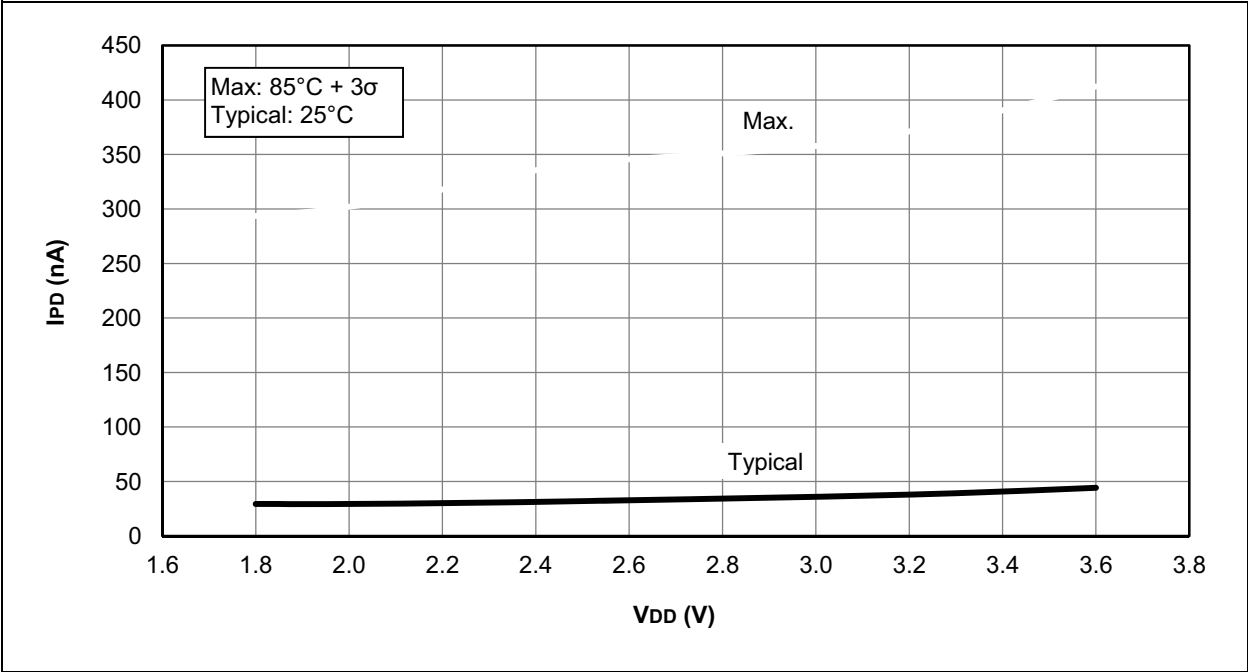
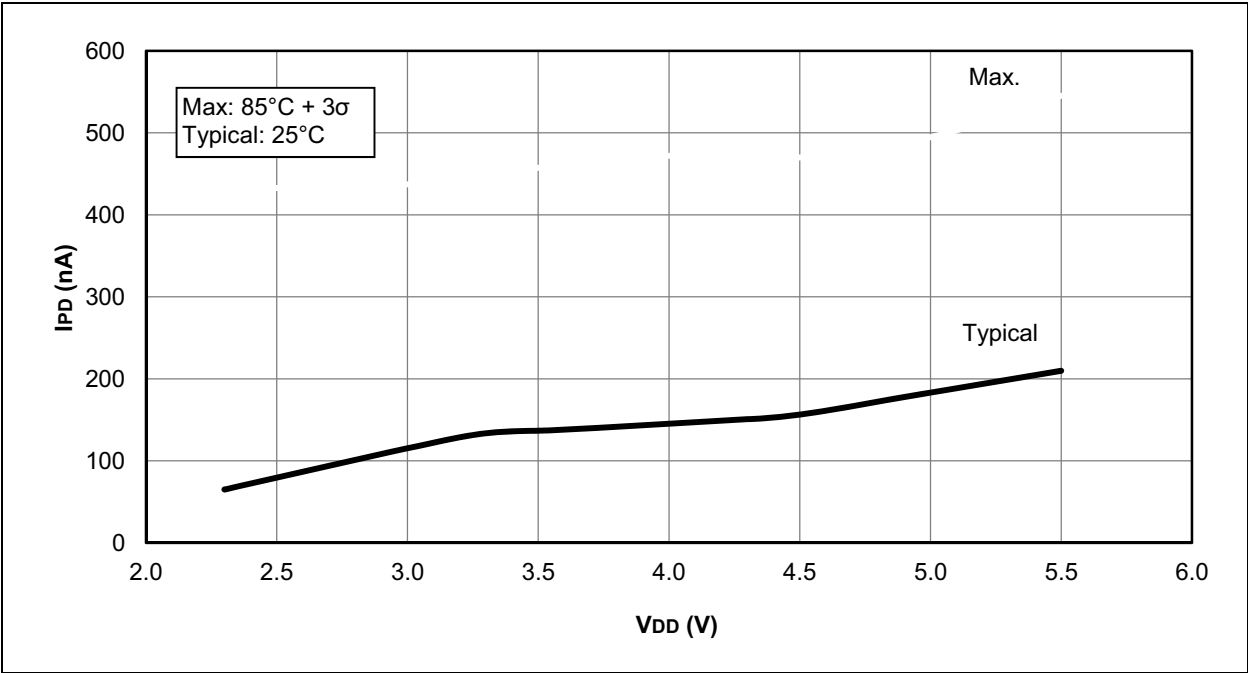


FIGURE 30-32: I_{PD} BASE, LOW-POWER SLEEP MODE, V_{REGPM} = 1, PIC16F1508/9 ONLY



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