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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 12x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1508t-i-so

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1.0 DEVICE OVERVIEW

The block diagram of these devices are shown in Figure 1-1, the available peripherals are shown in Table 1-1, and the pinout descriptions are shown in Table 1-2.

TABLE 1-1:	DEVICE PERIPHERAL	SUMMARY
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Peripheral		PIC12(L)F1501	PIC16(L)F1503	PIC16(L)F1507	PIC16(L)F1508	PIC16(L)F1509
Analog-to-Digital Converter (A	ADC)	•	•	•	•	٠
Complementary Wave Generation	ator (CWG)	•	•	•	٠	٠
Digital-to-Analog Converter (I	DAC)	•	•		•	•
Enhanced Universal Synchronous/Asynchronous Transmitter (EUSART)	Receiver/				•	•
Fixed Voltage Reference (FV	R)	•	•	•	٠	٠
Numerically Controlled Oscilla	ator (NCO)	•	•	•	•	•
Temperature Indicator		•	•	•	•	•
Comparators						
	C1	•	•		٠	•
	C2		•		•	•
Configurable Logic Cell (CLC	:)		-	-		-
	CLC1	•	•	•	•	•
	CLC2	٠	•	•	٠	•
	CLC3				٠	•
	CLC4				•	•
Master Synchronous Serial P	orts					
	MSSP1		•		٠	•
PWM Modules						
	PWM1	•	•	•	٠	•
	PWM2	•	•	•	•	•
	PWM3	٠	•	•	٠	•
	PWM4	٠	•	•	٠	•
Timers						
	Timer0	•	•	•	٠	•
	Timer1	•	•	•	•	•
	Timer2	•	•	•	٠	•

4.0 DEVICE CONFIGURATION

Device configuration consists of Configuration Words, Code Protection and Device ID.

4.1 Configuration Words

There are several Configuration Word bits that allow different oscillator and memory protection options. These are implemented as Configuration Word 1 at 8007h and Configuration Word 2 at 8008h.

Note: The DEBUG bit in Configuration Words is managed automatically by device development tools including debuggers and programmers. For normal device operation, this bit should be maintained as a '1'.

5.5 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) allows the device to continue operating should the external oscillator or external clock fail. If an oscillator mode is selected, the FSCM can detect oscillator failure any time after the Oscillator Start-up Timer (OST) has expired. When an external clock mode is selected, the FSCM can detect failure as soon as the device is released from Reset.

FSCM is enabled by setting the FCMEN bit in the Configuration Words. The FSCM is applicable to external oscillator modes (LP, XT, HS) and external clock modes (ECH, ECM, ECL, EXTRC) and the Secondary Oscillator (SOSC).





5.5.1 FAIL-SAFE DETECTION

The FSCM module detects a failed oscillator by monitoring falling clock edges and using LFINTOSC as a time base. See Figure 5-9. Detection of a failed oscillator will take 32 to 96 cycles of the LFINTOSC. Figure 5-10 shows a timing diagram of the FSCM module.

5.5.2 FAIL-SAFE OPERATION

When the external clock fails, the FSCM switches the CPU clock to an internal clock source and sets the OSFIF bit of the PIR2 register. The internal clock source is determined by the IRCF<3:0> bits in the OSCCON register.

When the OSFIF bit is set, an interrupt will be generated, if the OSFIE bit in the PIE2 register is enabled. The user's firmware in the Interrupt Service Routine (ISR) can then take steps to mitigate the problems that may arise from the failed clock.

The system clock will continue to be sourced from the internal clock source until the fail-safe condition has been cleared, see Section 5.5.3 "Fail-Safe Condition Clearing".

5.5.3 FAIL-SAFE CONDITION CLEARING

When a Fail-Safe condition exists, the user must take the following actions to clear the condition before returning to normal operation with the external source.

The next sections describe how to clear the Fail-Safe condition for specific clock selections (FOSC bits) and clock switching modes (SCS bit settings).

When a Fail-Safe condition occurs with the FOSC bits selecting external oscillator (FOSC<2:0> = HS, XT, LP) and the clock switch has been selected to run from the FOSC selection (SCS<1:0> = 00), the condition is cleared by performing the following procedure.

When SCS<1:0> = 00 (Running from FOSC selection)

SCS<1:0> = 1x:

Change the SCS bits in the OSCCON register to select the internal oscillator block. This resets the OST timer and allows it to operate again.

OSFIF = 0:

Clear the OSFIF bit in the PIR2 register.

SCS<1:0> = 00:

Change the SCS bits in the OSCCON register to select the FOSC Configuration Word clock selection. This will start the OST. The CPU will continue to operate from the internal oscillator until the OST count is reached. When OST expires, the clock module will switch to the external oscillator and the Fail-Safe condition will be cleared.

If the Fail-Safe condition still exists, the OSFIF bit will again be set by hardware.

5.5.3.2 External Clock with SCS<1:0> = 00

When a Fail-Safe condition occurs with the FOSC bits selecting external clock (FOSC<2:0> = ECH, ECM, ECL, EXTRC) and the clock switch has selected to run from the FOSC selection (SCS<1:0> = 00), the condition is cleared by performing the following procedure.

When SCS<1:0> = 00 (Running from FOSC selection)

SCS<1:0> = 1x:

Change the SCS bits in the OSCCON register to select the internal oscillator block. This resets the OST timer and allows it to operate again.

OSFIF = 0:

Clear the OSFIF bit in the PIR2 register.





6.3 Register Definitions: BOR Control

REGISTER 6-1: BORCON: BROWN-OUT RESET CONTROL REGISTER

R/W-1/u	R/W-0/u	U-0	U-0	U-0	U-0	U-0	R-q/u
SBOREN	BORFS	—	—	—	—	—	BORRDY
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Value depends on condition

bit 7	SBOREN: Software Brown-Out Reset Enable bit <u>If BOREN <1:0> in Configuration Words = 01</u> : 1 = BOR Enabled 0 = BOR Disabled <u>If BOREN <1:0> in Configuration Words ≠ 01</u> : SBOREN is read/write, but has no effect on the BOR
bit 6	BORFS: Brown-Out Reset Fast Start bit ⁽¹⁾ <u>If BOREN <1:0> = 10 (Disabled in Sleep) or BOREN<1:0> = 01 (Under software control):</u> 1 = Band gap is forced on always (covers sleep/wake-up/operating cases) 0 = Band gap operates normally, and may turn off <u>If BOREN<1:0> = 11 (Always on) or BOREN<1:0> = 00 (Always off)</u> BORFS is Read/Write, but has no effect.
bit 5-1	Unimplemented: Read as '0'
bit 0	BORRDY: Brown-Out Reset Circuit Ready Status bit 1 = The Brown-out Reset circuit is active 0 = The Brown-out Reset circuit is inactive
Note 1:	BOREN<1:0> bits are located in Configuration Words.

R/W-0/U	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	
TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	_	TMR2IE	TMR1IE	
bit 7							bit 0	
Legena:	hit	M = M/ritabla	hit	II – Unimplon	nantad hit raa	d aa 'O'		
	DIL				t DOD and DC		thar Deasta	
u = Dit is unch	angeu	x = Dit is ullki			IL FOR and BC		iner Resels	
I = BILIS SEL		0 = Bit is cie	areo					
bit 7	TMR1GIE: Ti	mer1 Gate Inte	errupt Enable I	oit				
	1 = Enables t	he Timer1 gate	e acquisition ir	nterrupt				
	0 = Disables	the Timer1 gat	e acquisition i	nterrupt				
bit 6	ADIE: Analog	g-to-Digital Con	verter (ADC)	Interrupt Enable	e bit			
	1 = Enables t	he ADC interru	ıpt					
	0 = Disables the ADC interrupt							
bit 5	RCIE: USAR	T Receive Inter	rrupt Enable b	it				
	1 = Enables t 0 = Disables	he USART receive interrupt						
hit 4		Transmit Inte	rrunt Enable h	it				
bit i	1 = Enables t	he USART transmit interrupt						
	0 = Disables	the USART tra	nsmit interrup	t				
bit 3	SSP1IE: Syn	chronous Seria	al Port (MSSP) Interrupt Enat	ole bit			
	1 = Enables t	he MSSP inter	rupt					
	0 = Disables	the MSSP inte	rrupt					
bit 2	Unimplemen	ted: Read as '	0'					
bit 1	TMR2IE: TM	R2 to PR2 Mat	ch Interrupt Ei	nable bit				
	1 = Enables t 0 = Disables	he Timer2 to P the Timer2 to F	R2 match inte R2 match inte	errupt errupt				
bit 0	TMR1IE: Tim	er1 Overflow Ir	nterrupt Enabl	e bit				
	1 = Enables t	he Timer1 ove	rflow interrupt					
	0 = Disables	the Timer1 ove	rflow interrunt	•				

REGISTER 7-2: PIE1: PERIPHERAL INTERRUPT ENABLE REGISTER 1

U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0			
—	—	—	—	CLC4IE	CLC3IE	CLC2IE	CLC1IE			
bit 7							bit 0			
Legend:										
R = Readable	e bit	W = Writable	bit	U = Unimpler	nented bit, read	as '0'				
u = Bit is uncl	hanged	x = Bit is unkr	iown	-n/n = Value a	at POR and BO	R/Value at all o	other Resets			
'1' = Bit is set		'0' = Bit is clea	ared							
bit 7-4	Unimplemen	ted: Read as '	כי							
bit 3	CLC4IE: Con	ifigurable Logic	Block 4 Inter	rrupt Enable bit						
	1 = Enables	the CLC 4 inter	the CLC 4 interrupt							
	0 = Disables	the CLC 4 inte	rrupt							
bit 2	CLC3IE: Con	figurable Logic	Block 3 Inte	rrupt Enable bit						
	1 = Enables	1 = Enables the CLC 3 interrupt								
L:1		the CLC 3 Inte	rrupt Dis els 2 lintes	www.mt Enchla hit						
DIT		Ingurable Logic		rrupt Enable bit						
	\perp = Enables 0 = Disables	the CLC 2 Inter	rupt							
bit 0	CI C1IF: Con	figurable Logic	Block 1 Inte	rrupt Enable bit						
bit o	1 = Enables	the CLC 1 inter	rupt							
	0 = Disables	the CLC 1 inte	rrupt							
			must bo							
NOLE. DI		I CON TEGISLEI	must be							

REGISTER 7-4: PIE3: PERIPHERAL INTERRUPT ENABLE REGISTER 3

set to enable any peripheral interrupt.

U-0	U-0	R/W-x/u	R/W-x/u	U-0	R/W-x/u	R/W-x/u	R/W-x/u
—	—	LATA5	LATA4	—	LATA2	LATA1	LATA0
bit 7							bit 0
Legend:							
R = Readable bit		W = Writable bit		U = Unimplemented bit, read as '0'			
u = Bit is unchanged		x = Bit is unknown		-n/n = Value a	at POR and BOF	R/Value at all o	ther Resets
'1' = Bit is set	İ.	'0' = Bit is cle	ared				
bit 7-6	Unimplemen	ted: Read as '	0'				
bit 5.4 LATA -5.4 DAZE 4 Output Lateb Value bite ⁽¹⁾							

REGISTER 11-4: LATA: PORTA DATA LATCH REGISTER

- bit 5-4 LATA<5:4>: RA<5:4> Output Latch Value bits⁽¹⁾
- bit 3 Unimplemented: Read as '0'
- bit 2-0 LATA<2:0>: RA<2:0> Output Latch Value bits⁽¹⁾
- **Note 1:** Writes to PORTA are actually written to corresponding LATA register. Reads from PORTA register is return of actual I/O pin values.

REGISTER 11-5: ANSELA: PORTA ANALOG SELECT REGISTER

U-0	U-0	U-0	R/W-1/1	U-0	R/W-1/1	R/W-1/1	R/W-1/1
—	—	—	ANSA4	—	ANSA2	ANSA1	ANSA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-5	Unimplemented: Read as '0'
bit 4	 ANSA4: Analog Select between Analog or Digital Function on pins RA4, respectively 1 = Analog input. Pin is assigned as analog input⁽¹⁾. Digital input buffer disabled. 0 = Digital I/O. Pin is assigned to port or digital special function.
bit 3	Unimplemented: Read as '0'
bit 2-0	 ANSA<2:0>: Analog Select between Analog or Digital Function on pins RA<2:0>, respectively 1 = Analog input. Pin is assigned as analog input⁽¹⁾. Digital input buffer disabled. 0 = Digital I/O. Pin is assigned to port or digital special function.
Note 1.	When setting a pin to an analog input the corresponding TRIS bit must be set to Input mode in order to

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

REGISTER 11-9:	LATB: PORTB DATA LATCH REGISTER
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R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	U-0	U-0	U-0	U-0	
LATB7	LATB6	LATB5	LATB4		—	—	—	
bit 7						•	bit 0	
Legend:								
R = Readable bit W = Writable bit				U = Unimplemented bit, read as '0'				
u = Bit is unchanged x = Bit is unknown		nown	-n/n = Value at POR and BOR/Value at all other Resets					
'1' = Bit is set '0' = Bit is cleared								

bit 7-4 LATB<7:4>: RB<7:4> Output Latch Value bits⁽¹⁾

bit 3-0 Unimplemented: Read as '0'

Note 1: Writes to PORTB are actually written to corresponding LATB register. Reads from PORTB register is return of actual I/O pin values.

REGISTER 11-10: ANSELB: PORTB ANALOG SELECT REGISTER

U-0	U-0	R/W-1/1	R/W-1/1	U-0	U-0	U-0	U-0
—	—	ANSB5	ANSB4	—	—	—	—
bit 7							bit 0
Logondi							

Legena:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 Unimplemented: Read as '0'

bit 5-4 **ANSB<5:4>**: Analog Select between Analog or Digital Function on pins RB<5:4>, respectively 1 = Analog input. Pin is assigned as analog input⁽¹⁾. Digital input buffer disabled.

0 = Digital I/O. Pin is assigned to port or digital special function.

bit 3-0 Unimplemented: Read as '0'

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

15.3 Register Definitions: ADC Control

REGISTER 15-1: ADCON0: ADC CONTROL REGISTER 0

U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0		
—			CHS<4:0>			GO/DONE	ADON		
bit 7							bit 0		
Legend:									
R = Reada	ble bit	W = Writable	bit	U = Unimpler	nented bit, rea	id as '0'			
u = Bit is u	nchanged	x = Bit is unkr	nown	-n/n = Value a	at POR and BO	OR/Value at all c	ther Resets		
'1' = Bit is s	set	'0' = Bit is cle	ared						
bit 7	Unimpleme	nted: Read as '	0'						
bit 6-2	CHS<4:0>: /	Analog Channel	Select bits						
	00000 = AN	0							
	00001 = AN	1							
	00010 = AN	2							
	00011 = AN	UUU11 = AN3							
	00100 = AN	5							
	00110 = AN	6							
	00111 = AN	7							
	01000 = AN	8							
	01001 = AN	9							
	01010 = AN	10							
	01011 - AN	served No cha	nel connecte	d					
	•			G .					
	•								
	•								
	11100 = Re	served. No cha	nnel connecte	d.					
	11101 = 100	C (Digital to An	alog Converte	r)(3)					
	11110 = DA	R (Fixed Voltage	e Reference) E	Buffer 1 Output ⁽	2)				
bit 1	GO/DONE: /		n Status bit	·					
	1 = ADC con	version cycle ir	progress. Se	tting this bit sta	rts an ADC co	nversion cycle.			
	This bit is	s automatically	cleared by har	dware when the	e ADC conver	sion has comple	ted.		
	0 = ADC con	version comple	ted/not in prog	gress					
bit 0	ADON: ADC	Enable bit							
	1 = ADC is e	nabled							
	0 = ADC is d	lisabled and cor	nsumes no ope	erating current					
Note 1:	See Section 14.0) "Temperature	Indicator Mo	odule" for more	information.				
2:	See Section 13.0) "Fixed Voltag	e Reference ((FVR)" for more	e information.				

3: See Section 16.0 "5-Bit Digital-to-Analog Converter (DAC) Module" for more information.

100KL 19-3.	TIMENT GATE SINGLE-FULSE MC	
TMR1GE		
T1GPOL		
T1GSPM		
T1GG <u>O/</u> DONE	▲ Set by software Counting enabled on	Cleared by hardware on falling edge of T1GVAL
t1g_in	rising edge of T1G	
Т1СКІ		
T1GVAL		
Timer1	N N + 1	N + 2
TMR1GIF	Cleared by software	 Set by hardware on falling edge of T1GVAL



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28.0 INSTRUCTION SET SUMMARY

Each instruction is a 14-bit word containing the operation code (opcode) and all required operands. The opcodes are broken into three broad categories.

- · Byte Oriented
- · Bit Oriented
- · Literal and Control

The literal and control category contains the most varied instruction word format.

Table 28-3 lists the instructions recognized by the MPASM $^{\rm TM}$ assembler.

All instructions are executed within a single instruction cycle, with the following exceptions, which may take two or three cycles:

- Subroutine takes two cycles (CALL, CALLW)
- Returns from interrupts or subroutines take two cycles (RETURN, RETLW, RETFIE)
- Program branching takes two cycles (GOTO, BRA, BRW, BTFSS, BTFSC, DECFSZ, INCSFZ)
- One additional instruction cycle will be used when any instruction references an indirect file register and the file select register is pointing to program memory.

One instruction cycle consists of 4 oscillator cycles; for an oscillator frequency of 4 MHz, this gives a nominal instruction execution rate of 1 MHz.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

28.1 Read-Modify-Write Operations

Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator 'd'. A read operation is performed on a register even if the instruction writes to that register.

TABLE 28-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
х	Don't care location (= 0 or 1). The assembler will generate code with x = 0 . It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.
n	FSR or INDF number. (0-1)
mm	Pre-post increment-decrement mode selection

TABLE 28-2: ABBREVIATION DESCRIPTIONS

Field	Description
PC	Program Counter
TO	Time-Out bit
С	Carry bit
DC	Digit Carry bit
Z	Zero bit
PD	Power-Down bit

NOTES:

29.2 Standard Operating Conditions

The standard operating conditions for any device are defined as:

Operating Voltage: Operating Temperature:	$\label{eq:VDDMAX} \begin{array}{l} V \text{DDMIN} \leq V \text{DD} \leq V \text{DDMAX} \\ \text{Ta}_\text{MIN} \leq \text{Ta} \leq \text{Ta}_\text{MAX} \end{array}$	
VDD — Operating Supply	v Voltage ⁽¹⁾	
PIC16LF1508/9		
Vddmin (F	osc ≤ 16 MHz)	
VDDMIN (1	6 MHz < Fosc ≤ 20 MHz)	
VDDMAX		
PIC16F1508/9		
VDDMIN (F	$osc \leq 16 MHz$)	
VDDMIN (1	6 MHz < Fosc ≤ 20 MHz)	
VDDMAX		+5.5V
TA — Operating Ambient	Temperature Range	
Industrial Temperat	ure	
TA_MIN		40°C
Та_мах		+85°C
Extended Temperat	ure	
TA_MIN		-40°C
Та_мах		+125°C

Note 1: See Parameter D001, DC Characteristics: Supply Voltage.

TABLE 29-21: I²C BUS DATA REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	Symbol	Characteristic		Min.	Max.	Units	Conditions
SP100*	Тнідн	Clock high time	100 kHz mode	4.0	_	μS	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6		μS	Device must operate at a minimum of 10 MHz
			SSP module	1.5Tcy	_		
SP101*	TLOW	Clock low time	100 kHz mode	4.7		μS	Device must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3		μS	Device must operate at a minimum of 10 MHz
			SSP module	1.5Tcy	_		
SP102*	TR	SDA and SCL rise	100 kHz mode	—	1000	ns	
	time	400 kHz mode	20 + 0.1Св	300	ns	CB is specified to be from 10-400 pF	
SP103*	TF	SDA and SCL fall	100 kHz mode	—	250	ns	
t	time	400 kHz mode	20 + 0.1Св	250	ns	CB is specified to be from 10-400 pF	
SP106*	THD:DAT	Data input hold time	100 kHz mode	0		ns	
			400 kHz mode	0	0.9	μS	
SP107*	TSU:DAT	Data input setup	100 kHz mode	250	_	ns	(Note 2)
		time	400 kHz mode	100		ns	
SP109*	ΤΑΑ	Output valid from	100 kHz mode	—	3500	ns	(Note 1)
		clock	400 kHz mode	—	_	ns	
SP110*	TBUF	Bus free time	100 kHz mode	4.7	_	μS	Time the bus must be free
			400 kHz mode	1.3	_	μS	before a new transmission can start
SP111	Св	Bus capacitive loading	ng	_	400	pF	

* These parameters are characterized but not tested.

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

2: A Fast mode (400 kHz) I²C bus device can be used in a Standard mode (100 kHz) I²C bus system, but the requirement TSU:DAT \geq 250 ns must then be met. This will automatically be the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line TR max. + TSU:DAT = 1000 + 250 = 1250 ns (according to the Standard mode I²C bus specification), before the SCL line is released.













31.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

31.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

31.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

31.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a fullspeed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming[™] (ICSP[™]).

31.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

20-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units			
Dimen	MIN	NOM	MAX	
Number of Pins	Ν		20	
Pitch	е		0.50 BSC	
Overall Height	А	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2 2.60 2.70 2		
Overall Length	D	4.00 BSC		
Exposed Pad Length	D2	2.60 2.70 2.80		
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	_	_

Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated.
- 3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-126B