Microchip Technology - PIC16LF1508-E/SO Datasheet





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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	7KB (4K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1508-e-so

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3.3.2 SPECIAL FUNCTION REGISTER

The Special Function Registers are registers used by the application to control the desired operation of peripheral functions in the device. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh). The registers associated with the operation of the peripherals are described in the appropriate peripheral chapter of this data sheet.

3.3.3 GENERAL PURPOSE RAM

There are up to 80 bytes of GPR in each data memory bank. The Special Function Registers occupy the 20 bytes after the core registers of every data memory bank (addresses x0Ch/x8Ch through x1Fh/x9Fh).

3.3.3.1 Linear Access to GPR

The general purpose RAM can be accessed in a non-banked method via the FSRs. This can simplify access to large memory structures. See **Section 3.6.2** "Linear Data Memory" for more information.

3.3.4 COMMON RAM

There are 16 bytes of common RAM accessible from all banks.

FIGURE 3-2: BANKED MEMORY PARTITIONING

7-bit Bank Offset	Memory Region
00h	Core Registers
0Bh	(12 bytes)
0Ch	Special Function Registers
1Fh	(20 bytes maximum)
6Fh	General Purpose RAM (80 bytes maximum)
70h	Common RAM
7Fh	(16 bytes)

PIC16(L)F1508/9

U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	
—	—	—	—	CLC4IE	CLC3IE	CLC2IE	CLC1IE	
bit 7							bit 0	
Legend:								
R = Readable	e bit	W = Writable	bit	U = Unimpler	nented bit, read	as '0'		
u = Bit is uncl	hanged	x = Bit is unkr	iown	-n/n = Value a	at POR and BO	R/Value at all o	other Resets	
'1' = Bit is set		'0' = Bit is clea	ared					
bit 7-4	Unimplemen	ted: Read as '	כי					
bit 3	CLC4IE: Con	ifigurable Logic	Block 4 Inter	rrupt Enable bit				
	1 = Enables	the CLC 4 inter	rupt					
	0 = Disables	the CLC 4 inte	rrupt					
bit 2	CLC3IE: Con	figurable Logic	Block 3 Inte	rrupt Enable bit				
	1 = Enables	the CLC 3 inter	rupt					
L:1		0 = Disables the CLC 3 interrupt						
DIT		CLC2IE: Configurable Logic Block 2 Interrupt Enable bit						
	\perp = Enables 0 = Disables	the CLC 2 Inter	rupt					
bit 0	CI C1IF: Con	CI CIIE: Configurable Logic Block 1 Interrupt Enable bit						
bit o	1 = Enables the CLC 1 interrupt							
	0 = Disables	the CLC 1 inte	rrupt					
			must bo					
NOLE. DI		I CON TEGISLET	must be					

REGISTER 7-4: PIE3: PERIPHERAL INTERRUPT ENABLE REGISTER 3

set to enable any peripheral interrupt.

9.1 Independent Clock Source

The WDT derives its time base from the 31 kHz LFINTOSC internal oscillator. Time intervals in this chapter are based on a nominal interval of 1 ms. See **Section 29.0 "Electrical Specifications"** for the LFINTOSC tolerances.

9.2 WDT Operating Modes

The Watchdog Timer module has four operating modes controlled by the WDTE<1:0> bits in Configuration Words. See Table 9-1.

9.2.1 WDT IS ALWAYS ON

When the WDTE bits of Configuration Words are set to '11', the WDT is always on.

WDT protection is active during Sleep.

9.2.2 WDT IS OFF IN SLEEP

When the WDTE bits of Configuration Words are set to '10', the WDT is on, except in Sleep.

WDT protection is not active during Sleep.

9.2.3 WDT CONTROLLED BY SOFTWARE

When the WDTE bits of Configuration Words are set to '01', the WDT is controlled by the SWDTEN bit of the WDTCON register.

WDT protection is unchanged by Sleep. See Table 9-1 for more details.

WDTE<1:0>	SWDTEN	Device Mode	WDT Mode
11	Х	х	Active
10		Awake	Active
10	X	Sleep	Disabled
0.1	1	х	Active
UT	0	х	Disabled
00	Х	х	Disabled

TABLE 9-1: WDT OPERATING MODES

9.3 Time-Out Period

The WDTPS bits of the WDTCON register set the time-out period from 1 ms to 256 seconds (nominal). After a Reset, the default time-out period is two seconds.

9.4 Clearing the WDT

The WDT is cleared when any of the following conditions occur:

- · Any Reset
- CLRWDT instruction is executed
- Device enters Sleep
- · Device wakes up from Sleep
- Oscillator fail
- WDT is disabled
- Oscillator Start-up Timer (OST) is running

See Table 9-2 for more information.

9.5 Operation During Sleep

When the device enters Sleep, the WDT is cleared. If the WDT is enabled during Sleep, the WDT resumes counting. When the device exits Sleep, the WDT is cleared again.

The WDT remains clear until the OST, if enabled, completes. See Section 5.0 "Oscillator Module (With Fail-Safe Clock Monitor)" for more information on the OST.

When a WDT time-out occurs while the device is in Sleep, no Reset is generated. Instead, the device wakes up and resumes operation. The \overline{TO} and \overline{PD} bits in the STATUS register are changed to indicate the event. The RWDT bit in the PCON register can also be used. See Section 3.0 "Memory Organization" for more information.

TABLE 9-2:	WDT CLEARING CONDITIONS
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Conditions	WDT	
WDTE<1:0> = 00		
WDTE<1:0> = 01 and SWDTEN = 0		
WDTE<1:0> = 10 and enter Sleep	Cleared	
CLRWDT Command	Cleared	
Oscillator Fail Detected		
Exit Sleep + System Clock = T1OSC, EXTRC, INTOSC, EXTCLK		
Exit Sleep + System Clock = XT, HS, LP	Cleared until the end of OST	
Change INTOSC divider (IRCF bits)	Unaffected	

PIC16(L)F1508/9

FIGURE 10-6: FLASH MEMORY WRITE FLOWCHART



11.5 PORTB Registers

11.5.1 DATA REGISTER

PORTB is a 4-bit wide, bidirectional port. The corresponding data direction register is TRISB (Register 11-8). Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., disable the output driver). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., enables output driver and puts the contents of the output latch on the selected pin). Example 11-1 shows how to initialize an I/O port.

Reading the PORTB register (Register 11-7) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATB).

11.5.2 DIRECTION CONTROL

The TRISB register (Register 11-8) controls the PORTB pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISB register are maintained set when using them as analog inputs. I/O pins configured as analog input always read '0'.

11.5.3 ANALOG CONTROL

The ANSELB register (Register 11-10) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELB bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELB bits has no effect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note:	The ANSELB bits default to the Analog
	mode after Reset. To use any pins as
	digital general purpose or peripheral
	inputs, the corresponding ANSEL bits
	must be initialized to '0' by user software.

11.5.4 PORTB FUNCTIONS AND OUTPUT PRIORITIES

Each PORTB pin is multiplexed with other functions. The pins, their combined functions and their output priorities are shown in Table 11-5.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the highest priority.

Analog input functions, such as ADC and comparator inputs, are not shown in the priority lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELx registers. Digital output functions may control the pin when it is in Analog mode with the priority shown below in Table 11-5.

Pin Name	Function Priority ⁽¹⁾
RB4	SDA
	RB4
RB5	RB5
RB6	SCL
	SCK
	RB6
RB7	CLC3
	ТХ
	RB7

TABLE 11-5: PORTB OUTPUT PRIORITY

Note 1: Priority listed from highest to lowest.

2: Default pin (see APFCON register).

3: Alternate pin (see APFCON register).

12.6 Register Definitions: Interrupt-on-Change Control

REGISTER 12-1: IOCAP: INTERRUPT-ON-CHANGE PORTA POSITIVE EDGE REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
_	_	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0
bit 7							bit 0
Legend:							
R = Readable bit		W = Writable bi	t	U = Unimplem	ented bit, read as	'0'	
u = Bit is unchan	ged	x = Bit is unkno	wn	-n/n = Value at	POR and BOR/Va	alue at all other f	Resets
'1' = Bit is set		'0' = Bit is clear	ed				

bit 7-6 Unimplemented: Read as '0'

bit 5-0

bit 5-0

bit 5-0

IOCAP<5:0>: Interrupt-on-Change PORTA Positive Edge Enable bits

1 = Interrupt-on-Change enabled on the pin for a positive going edge. IOCAFx bit and IOCIF flag will be set upon detecting an edge.

0 = Interrupt-on-Change disabled for the associated pin.

REGISTER 12-2: IOCAN: INTERRUPT-ON-CHANGE PORTA NEGATIVE EDGE REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
_	_	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 Unimplemented: Read as '0'

IOCAN<5:0>: Interrupt-on-Change PORTA Negative Edge Enable bits

- 1 = Interrupt-on-Change enabled on the pin for a negative going edge. IOCAFx bit and IOCIF flag will be set upon detecting an edge.
- 0 = Interrupt-on-Change disabled for the associated pin.

REGISTER 12-3: IOCAF: INTERRUPT-ON-CHANGE PORTA FLAG REGISTER

U-0	U-0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0	R/W/HS-0/0
—	—	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HS - Bit is set in hardware

bit 7-6 Unimplemented: Read as '0'

IOCAF<5:0>: Interrupt-on-Change PORTA Flag bits

1 = An enabled change was detected on the associated pin.

Set when IOCAPx = 1 and a rising edge was detected on RAx, or when IOCANx = 1 and a falling edge was detected on RAx.

0 = No change was detected, or the user cleared the detected change.

13.3 Register Definitions: FVR Control

R/W-0/0	R-q/q	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
FVREN ⁽¹⁾	FVRRDY ⁽²⁾	TSEN ⁽³⁾	TSRNG ⁽³⁾	CDAFVR<1:0> ⁽¹⁾		ADFVR<1:0> ⁽¹⁾	
bit 7	·						bit (
Legend:							
R = Readab	ole bit	W = Writable	bit	U = Unimplei	mented bit, read	as '0'	
u = Bit is un	changed	x = Bit is unki	nown	-n/n = Value	at POR and BO	R/Value at all c	ther Resets
'1' = Bit is s	et	'0' = Bit is cle	ared	q = Value de	pends on condit	ion	
bit 7	FVREN: Fixed 1 = Fixed Vol 0 = Fixed Vol	d Voltage Refe Itage Referenc Itage Referenc	rence Enable e is enabled e is disabled	bit ⁽¹⁾			
bit 6	t 6 FVRRDY: Fixed Voltage Reference Ready Flag bit ⁽²⁾ 1 = Fixed Voltage Reference output is ready for use 0 = Fixed Voltage Reference output is not ready or not enabled						
bit 5	TSEN: Temperature Indicator Enable bit ⁽³⁾ 1 = Temperature Indicator is enabled 0 = Temperature Indicator is disabled						
bit 4	TSRNG: Temperature Indicator Range Selection bit ⁽³⁾ 1 = VOUT = VDD - 4VT (High Range) 0 = VOUT = VDD - 2VT (Low Range)						
bit 3-2	-2 CDAFVR<1:0>: Comparator FVR Buffer Gain Selection bits ⁽¹⁾ 11 = Comparator FVR Buffer Gain is 4x, with output voltage = 4x VFVR (4.096V nominal) ⁽⁴⁾ 10 = Comparator FVR Buffer Gain is 2x, with output voltage = 2x VFVR (2.048V nominal) ⁽⁴⁾ 01 = Comparator FVR Buffer Gain is 1x, with output voltage = 1x VFVR (1.024V nominal) 00 = Comparator FVR Buffer is off						
bit 1-0	ADFVR<1:0> 11 = ADC FV 10 = ADC FV 01 = ADC FV 00 = ADC FV	: ADC FVR Bu R Buffer Gain R Buffer Gain R Buffer Gain R Buffer is off	iffer Gain Sele is 4x, with out is 2x, with out is 1x, with out	ection bit ⁽¹⁾ put voltage = 4 put voltage = 2 put voltage = 1	Ix Vfvr (4.096V 2x Vfvr (2.048V 1x Vfvr (1.024V	nominal) (4) nominal) (4) nominal)	
Note 1: 7	To minimize curren ng the Buffer Gain	t consumption	when the FVF	R is disabled, t	he FVR buffers	should be turne	ed off by clear

REGISTER 13-1: FVRCON: FIXED VOLTAGE REFERENCE CONTROL REGISTER

- 2: FVRRDY is always '1' for the PIC16F1508/9 devices.
- 3: See Section 14.0 "Temperature Indicator Module" for additional information.
- 4: Fixed Voltage Reference output cannot exceed VDD.

TABLE 13-2: SUMMARY OF REGISTERS ASSOCIATED WITH THE FIXED VOLTAGE REFERENCE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page	
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR>1:0>		CDAFVR>1:0> ADFVR<1:0>		R<1:0>	125

Legend: Shaded cells are unused by the Fixed Voltage Reference module.

15.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

The Analog-to-Digital Converter (ADC) allows conversion of an analog input signal to a 10-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 10-bit binary result via successive

FIGURE 15-1: ADC BLOCK DIAGRAM

approximation and stores the conversion result into the ADC result registers (ADRESH:ADRESL register pair). Figure 15-1 shows the block diagram of the ADC.

The ADC voltage reference is software selectable to be either internally generated or externally supplied.

The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake-up the device from Sleep.



17.2.5 COMPARATOR OUTPUT POLARITY

Inverting the output of the comparator is functionally equivalent to swapping the comparator inputs. The polarity of the comparator output can be inverted by setting the CxPOL bit of the CMxCON0 register. Clearing the CxPOL bit results in a non-inverted output.

Table 17-2 shows the output state versus input conditions, including polarity control.

TABLE 17-2: COMPARATOR OUTPUT STATE VS. INPUT CONDITIONS

Input Condition	CxPOL	CxOUT		
CxVN > CxVP	0	0		
CxVN < CxVP	0	1		
CxVN > CxVP	1	1		
CxVN < CxVP	1	0		

17.2.6 COMPARATOR SPEED/POWER SELECTION

The trade-off between speed or power can be optimized during program execution with the CxSP control bit. The default state for this bit is '1' which selects the Normal-Speed mode. Device power consumption can be optimized at the cost of slower comparator propagation delay by clearing the CxSP bit to '0'.



17.3 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 17-3. Since the analog input pins share their connection with a digital input, they have reverse biased ESD protection diodes to VDD and Vss. The analog input, therefore, must be between Vss and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur.

A maximum source impedance of $10 \text{ k}\Omega$ is recommended for the analog sources. Also, any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current to minimize inaccuracies introduced.

- Note 1: When reading a PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert as an analog input, according to the input specification.
 - Analog levels on any pin defined as a digital input, may cause the input buffer to consume more current than is specified.



21.4.5 START CONDITION

The I^2C specification defines a Start condition as a transition of SDAx from a high to a low state while SCLx line is high. A Start condition is always generated by the master and signifies the transition of the bus from an Idle to an Active state. Figure 21-12 shows wave forms for Start and Stop conditions.

A bus collision can occur on a Start condition if the module samples the SDAx line low before asserting it low. This does not conform to the I^2C Specification that states no bus collision can occur on a Start.

21.4.6 STOP CONDITION

A Stop condition is a transition of the SDAx line from low-to-high state while the SCLx line is high.

Note: At least one SCLx low time must appear before a Stop is valid, therefore, if the SDAx line goes low then high again while the SCLx line stays high, only the Start condition is detected.

21.4.7 RESTART CONDITION

A Restart is valid any time that a Stop would be valid. A master can issue a Restart if it wishes to hold the bus after terminating the current transfer. A Restart has the same effect on the slave that a Start would, resetting all slave logic and preparing it to clock in an address. The master may want to address the same or another slave. Figure 21-13 shows the wave form for a Restart condition.

In 10-bit Addressing Slave mode a Restart is required for the master to clock data out of the addressed slave. Once a slave has been fully addressed, matching both high and low address bytes, the master can issue a Restart and the high address byte with the R/\overline{W} bit set. The slave logic will then hold the clock and prepare to clock out data.

After a full match with R/\overline{W} clear in 10-bit mode, a prior match flag is set and maintained. Until a Stop condition, a high address with R/\overline{W} clear, or high address match fails.

21.4.8 START/STOP CONDITION INTERRUPT MASKING

The SCIE and PCIE bits of the SSPxCON3 register can enable the generation of an interrupt in Slave modes that do not typically support this function. Slave modes where interrupt on Start and Stop detect are already enabled, these bits will have no effect.

FIGURE 21-12: I²C START AND STOP CONDITIONS



FIGURE 21-13: I²C RESTART CONDITION



PIC16(L)F1508/9





21.6 I²C MASTER MODE

Master mode is enabled by setting and clearing the appropriate SSPM bits in the SSPxCON1 register and by setting the SSPEN bit. In Master mode, the SDAx and SCKx pins must be configured as inputs. The MSSP peripheral hardware will override the output driver TRIS controls when necessary to drive the pins low.

Master mode of operation is supported by interrupt generation on the detection of the Start and Stop conditions. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSPx module is disabled. Control of the I²C bus may be taken when the P bit is set, or the bus is idle.

In Firmware Controlled Master mode, user code conducts all I²C bus operations based on Start and Stop bit condition detection. Start and Stop condition detection is the only active circuitry in this mode. All other communication is done by the user software directly manipulating the SDAx and SCLx lines.

The following events will cause the SSPx Interrupt Flag bit, SSPxIF, to be set (SSPx interrupt, if enabled):

- · Start condition detected
- Stop condition detected
- · Data transfer byte transmitted/received
- Acknowledge transmitted/received
- Repeated Start generated
 - Note 1: The MSSPx module, when configured in I²C Master mode, does not allow queueing of events. For instance, the user is not allowed to initiate a Start condition and immediately write the SSPxBUF register to initiate transmission before the Start condition is complete. In this case, the SSPxBUF will not be written to and the WCOL bit will be set, indicating that a write to the SSPxBUF did not occur
 - 2: When in Master mode, Start/Stop detection is masked and an interrupt is generated when the SEN/PEN bit is cleared and the generation is complete.

21.6.1 I²C MASTER MODE OPERATION

The master device generates all of the serial clock pulses and the Start and Stop conditions. A transfer is ended with a Stop condition or with a Repeated Start condition. Since the Repeated Start condition is also the beginning of the next serial transfer, the I²C bus will not be released.

In Master Transmitter mode, serial data is output through SDAx, while SCLx outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (seven bits) and the Read/Write (R/W) bit. In this case, the R/W bit will be logic '0'. Serial data is transmitted eight bits at a time. After each byte is transmitted, an Acknowledge bit is received. Start and Stop conditions are output to indicate the beginning and the end of a serial transfer.

In Master Receive mode, the first byte transmitted contains the slave address of the transmitting device (seven bits) and the R/W bit. In this case, the R/W bit will be logic '1'. Thus, the first byte transmitted is a 7-bit slave address followed by a '1' to indicate the receive bit. Serial data is received via SDAx, while SCLx outputs the serial clock. Serial data is received eight bits at a time. After each byte is received, an Acknowledge bit is transmitted. Start and Stop conditions indicate the beginning and end of transmission.

A Baud Rate Generator is used to set the clock frequency output on SCLx. See **Section21.7 "Baud Rate Generator"** for more detail.

21.6.4 I²C MASTER MODE START CONDITION TIMING

To initiate a Start condition (Figure 21-26), the user sets the Start Enable bit, SEN bit of the SSPxCON2 register. If the SDAx and SCLx pins are sampled high, the Baud Rate Generator is reloaded with the contents of SSPxADD<7:0> and starts its count. If SCLx and SDAx are both sampled high when the Baud Rate Generator times out (TBRG), the SDAx pin is driven low. The action of the SDAx being driven low while SCLx is high is the Start condition and causes the S bit of the SSPxADD<7:0> and resumes its count. When the Baud Rate Generator times out (TBRG), the SDAx bit of the SSPxSTAT1 register to be set. Following this, the Baud Rate Generator is reloaded with the contents of SSPxADD<7:0> and resumes its count. When the Baud Rate Generator times out (TBRG), the SEN bit of the SSPxCON2 register will be automatically cleared

by hardware; the Baud Rate Generator is suspended, leaving the SDAx line held low and the Start condition is complete.

- Note 1: If at the beginning of the Start condition, the SDAx and SCLx pins are already sampled low, or if during the Start condition, the SCLx line is sampled low before the SDAx line is driven low, a bus collision occurs, the Bus Collision Interrupt Flag, BCLxIF, is set, the Start condition is aborted and the I²C module is reset into its Idle state.
 - 2: The Philips I²C Specification states that a bus collision cannot occur on a Start.



- 22.1.2.8 Asynchronous Reception Set-up:
- Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see Section22.4 "EUSART Baud Rate Generator (BRG)").
- 2. Clear the ANSEL bit for the RX pin (if applicable).
- 3. Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
- 4. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- 5. If 9-bit reception is desired, set the RX9 bit.
- 6. Enable reception by setting the CREN bit.
- 7. The RCIF interrupt flag bit will be set when a character is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE interrupt enable bit was also set.
- 8. Read the RCSTA register to get the error flags and, if 9-bit data reception is enabled, the ninth data bit.
- 9. Get the received eight Least Significant data bits from the receive buffer by reading the RCREG register.
- 10. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.

22.1.2.9 9-bit Address Detection Mode Set-up

This mode would typically be used in RS-485 systems. To set up an Asynchronous Reception with Address Detect Enable:

- Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see Section22.4 "EUSART Baud Rate Generator (BRG)").
- 2. Clear the ANSEL bit for the RX pin (if applicable).
- 3. Enable the serial port by setting the SPEN bit. The SYNC bit must be clear for asynchronous operation.
- If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- 5. Enable 9-bit reception by setting the RX9 bit.
- 6. Enable address detection by setting the ADDEN bit.
- 7. Enable reception by setting the CREN bit.
- The RCIF interrupt flag bit will be set when a character with the ninth bit set is transferred from the RSR to the receive buffer. An interrupt will be generated if the RCIE interrupt enable bit was also set.
- 9. Read the RCSTA register to get the error flags. The ninth data bit will always be set.
- 10. Get the received eight Least Significant data bits from the receive buffer by reading the RCREG register. Software determines if this is the device's address.
- 11. If an overrun occurred, clear the OERR flag by clearing the CREN receiver enable bit.
- 12. If the device has been addressed, clear the ADDEN bit to allow all received data into the receive buffer and generate interrupts.



FIGURE 22-5: ASYNCHRONOUS RECEPTION

24.0 CONFIGURABLE LOGIC CELL (CLC)

The Configurable Logic Cell (CLCx) provides programmable logic that operates outside the speed limitations of software execution. The logic cell takes up to 16 input signals, and through the use of configurable gates, reduces the 16 inputs to four logic lines that drive one of eight selectable single-output logic functions.

Input sources are a combination of the following:

- · I/O pins
- Internal clocks
- · Peripherals
- · Register bits

The output can be directed internally to peripherals and to an output pin.

Refer to Figure 24-1 for a simplified diagram showing signal flow through the CLCx.

Possible configurations include:

- Combinatorial Logic
 - AND
 - NAND
 - AND-OR
 - AND-OR-INVERT
 - OR-XOR
 - OR-XNOR
- Latches
 - S-R
 - Clocked D with Set and Reset
 - Transparent D with Set and Reset
 - Clocked J-K with Reset



FIGURE 24-1: CONFIGURABLE LOGIC CELL BLOCK DIAGRAM

29.3 DC Characteristics

TABLE 29-1: SUPPLY VOLTAGE

PIC16LF1508/9			Standard Operating Conditions (unless otherwise stated)							
PIC16F1508/9										
Param. No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions			
D001	Vdd	Supply Voltage								
			VDDMIN 1.8 2.5	_	VDDMAX 3.6 3.6	V V	Fosc ≤ 16 MHz Fosc ≤ 20 MHz			
D001			2.3 2.5	_	5.5 5.5	V V	Fosc ≤ 16 MHz Fosc ≤ 20 MHz			
D002*	Vdr	RAM Data Retention Voltage ⁽¹⁾								
			1.5		—	V	Device in Sleep mode			
D002*			1.7	_	_	V	Device in Sleep mode			
D002A*	VPOR	Power-on Reset Release Voltage ⁽²⁾								
			—	1.6	—	V				
D002A*			_	1.6	—	V				
D002B*	VPORR*	Power-on Reset Rearm Voltage ⁽²⁾								
			—	0.8	—	V				
D002B*				1.5	—	V				
D003	VFVR	Fixed Voltage Reference Voltage								
		1x gain (1.024V nominal) 2x gain (2.048V nominal) 4x gain (4.096V nominal)	-4 -3	_	+4 +7	%	$\label{eq:VDD} \begin{array}{l} VDD \geq 2.5V, \ -40^{\circ}C \leq TA \leq +85^{\circ}C \\ VDD \geq 2.5V, \ -40^{\circ}C \leq TA \leq +85^{\circ}C \\ VDD \geq 4.75V, \ -40^{\circ}C \leq TA \leq +85^{\circ}C \\ \end{array}$			
D004*	SVDD	VDD Rise Rate ⁽²⁾	0.05	—	—	V/ms	Ensures that the Power-on Reset signal is released properly.			

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

2: See Figure 29-3, POR and POR REARM with Slow Rising VDD.

























20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging









VIEW A-A

Microchip Technology Drawing C04-094C Sheet 1 of 2