Microchip Technology - PIC16LF1509-E/SO Datasheet





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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SOIC (0.295", 7.50mm Width)
Supplier Device Package	20-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1509-e-so

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U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
	<u> </u>	_		CLC4IF	CLC3IF	CLC2IF	CLC1IF
bit 7							bit 0
Legend:							
R = Readabl	e bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'	
u = Bit is und	changed	x = Bit is unkr	nown	-n/n = Value a	at POR and BO	R/Value at all o	ther Resets
'1' = Bit is se	t	'0' = Bit is clea	ared				
bit 7-4	Unimplement	ted: Read as '	0'				
bit 3	CLC4IF: Cont	figurable Logic	Block 4 Inter	rupt Flag bit			
	1 = Interrupt is	s pending					
	0 = Interrupt is	s not pending					
bit 2	CLC3IF: Cont	figurable Logic	Block 3 Inter	rupt Flag bit			
	1 = Interrupt is	s pending					
bit 1		s not penuing	Plook 2 Inter	rupt Elog bit			
	1 = Interrunt in			i upi riag bil			
	0 = Interrupt is	s not pendina					
bit 0	CLC1IF: Conf	figurable Logic	Block 1 Inter	rupt Flag bit			
	1 = Interrupt is	s pending	-	,			
	0 = Interrupt is	s not pending					
Note: In	terrupt flag bits a	re set when an	interrupt				
CC	ondition occurs, re	egardless of the	e state of				
its	s corresponding e	enable bit or th	e Global				
E	nable bit, GIE of	t the INTCON	register.				
0 a	sei soitware	of flag bits are c	lear prior				

REGISTER 7-7: PIR3: PERIPHERAL INTERRUPT REQUEST REGISTER 3

to enabling an interrupt.

8.3 Register Definitions: Voltage Regulator Control

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-1/1
—	—	—	—	—	—	VREGPM	Reserved
bit 7							bit 0
Legend:							

REGISTER 8-1: VREGCON: VOLTAGE REGULATOR CONTROL REGISTER⁽¹⁾

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-2	Unimplemented: Read as '0'
bit 1	VREGPM: Voltage Regulator Powe

VREGPM: Voltage Regulator Power Mode Selection bit

- 1 = Low-Power Sleep mode enabled in Sleep⁽²⁾
 Draws lowest current in Sleep, slower wake-up
- 0 = Normal Power mode enabled in Sleep⁽²⁾
 Draws higher current in Sleep, faster wake-up
- bit 0 **Reserved:** Read as '1'. Maintain this bit set.

Note 1: PIC16F1508/9 only.

2: See Section 29.0 "Electrical Specifications".

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	75
IOCAF	—	—	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0	121
IOCAN	—	—	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0	121
IOCAP	—	—	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0	121
IOCBF	IOCBF7	IOCBF6	IOCBF5	IOCBF4	_	_	—	—	122
IOCBN	IOCBN7	IOCBN6	IOCBN5	IOCBN4	_	_	—	—	122
IOCBP	IOCBP7	IOCBP6	IOCBP5	IOCBP4	_	_	—	—	122
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	_	TMR2IE	TMR1IE	76
PIE2	OSFIE	C2IE	C1IE	—	BCL1IE	NCO1IE	—	—	77
PIE3	—	—	—	—	CLC4IE	CLC3IE	CLC2IE	CLC1IE	78
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	—	TMR2IF	TMR1IF	78
PIR2	OSFIF	C2IF	C1IF	—	BCL1IF	NCO1IF	—	—	78
PIR3	—	—	—	—	CLC4IF	CLC3IF	CLC2IF	CLC1IF	81
STATUS	—	—	—	TO	PD	Z	DC	С	19
WDTCON	_	_		V	VDTPS<4:0	>		SWDTEN	88

TABLE 8-1: SUMMARY OF REGISTERS ASSOCIATED WITH POWER-DOWN MODE

Legend: — = unimplemented, read as '0'. Shaded cells are not used in Power-Down mode.

10.6 Register Definitions: Flash Program Memory Control

REGISTER 10-1: PMDATL: PROGRAM MEMORY DATA LOW BYTE REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
			PMDA	T<7:0>			
bit 7							bit 0
Legend:							
R = Readable bit		W = Writable bit		U = Unimpleme	nted bit, read as '0	,	
u = Bit is unchanged		x = Bit is unknown		-n/n = Value at f	POR and BOR/Valu	ue at all other Res	sets
'1' = Bit is set		'0' = Bit is cleared					

bit 7-0

PMDAT<7:0>: Read/write value for Least Significant bits of program memory

REGISTER 10-2: PMDATH: PROGRAM MEMORY DATA HIGH BYTE REGISTER

U-0	U-0	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u		
—	—		PMDAT<13:8>						
bit 7							bit 0		

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 Unimplemented: Read as '0'

bit 5-0 PMDAT<13:8>: Read/write value for Most Significant bits of program memory

REGISTER 10-3: PMADRL: PROGRAM MEMORY ADDRESS LOW BYTE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0				
	PMADR<7:0>										
bit 7							bit 0				

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **PMADR<7:0>**: Specifies the Least Significant bits for program memory address

REGISTER 10-4: PMADRH: PROGRAM MEMORY ADDRESS HIGH BYTE REGISTER

U-1	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
(1)				PMADR<14:8>	>		
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 Unimplemented: Read as '1'

bit 6-0 PMADR<14:8>: Specifies the Most Significant bits for program memory address

Note 1: Unimplemented, read as '1'.

11.4 Register Definitions: PORTA

U-0	U-0	R/W-x/x	R/W-x/x	R-x/x	R/W-x/x	R/W-x/x	R/W-x/x
—	—	RA5	RA4	RA3	RA2	RA1	RA0
bit 7							bit 0
Legend:							
R = Readable bit W = Writable bit		U = Unimplemented bit, read as '0'					
u = Bit is unchanged x = Bit is unknown		-n/n = Value at POR and BOR/Value at all other Resets					
'1' = Bit is set		'0' = Bit is clea	ared				

REGISTER 11-2: PORTA: PORTA REGISTER

bit 7-6	Unimplemented: Read as '0'
bit 5-0	RA<5:0>: PORTA I/O Value bits ⁽¹⁾
	1 = Port pin is <u>></u> Vін
	0 = Port pin is <u><</u> Vı∟

Note 1: Writes to PORTA are actually written to corresponding LATA register. Reads from PORTA register is return of actual I/O pin values.

REGISTER 11-3: TRISA: PORTA TRI-STATE REGISTER

U-0	U-0	R/W-1/1	R/W-1/1	U-1	R/W-1/1	R/W-1/1	R/W-1/1
—	—	TRISA5	TRISA4	(1)	TRISA2	TRISA1	TRISA0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6	Unimplemented: Read as '0'
bit 5-4	TRISA<5:4>: PORTA Tri-State Control bit 1 = PORTA pin configured as an input (tri-stated) 0 = PORTA pin configured as an output
bit 3	Unimplemented: Read as '1'

Note 1: Unimplemented, read as '1'.

REGISTER 11-15: ANSELC: PORTC ANALOG SELECT REGISTER

R/W-1/1	R/W-1/1	U-0	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
ANSC7	ANSC6	—	—	ANSC3	ANSC2	ANSC1	ANSC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6	 ANSC<7:6>: Analog Select between Analog or Digital Function on pins RC<7:6>, respectively 1 = Analog input. Pin is assigned as analog input⁽¹⁾. Digital input buffer disabled. 0 = Digital I/O. Pin is assigned to port or digital special function.
bit 5-4	Unimplemented: Read as '0'
bit 3-0	 ANSC<3:0>: Analog Select between Analog or Digital Function on pins RC<3:0>, respectively 1 = Analog input. Pin is assigned as analog input⁽¹⁾. Digital input buffer disabled. 0 = Digital I/O. Pin is assigned to port or digital special function.

Note 1: When setting a pin to an analog input, the corresponding TRIS bit must be set to Input mode in order to allow external control of the voltage on the pin.

TABLE 11-9: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELC	ANSC7	ANSC6	—	—	ANSC3	ANSC2	ANSC1	ANSC0	118
LATC	LATC7	LATC6	LATC5	LATC4	LATC3	LATC2	LATC1	LATC0	117
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	117
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	117

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTC.









19.6.2.1 T1G Pin Gate Operation

The T1G pin is one source for Timer1 gate control. It can be used to supply an external source to the Timer1 gate circuitry.

19.6.2.2 Timer0 Overflow Gate Operation

When Timer0 increments from FFh to 00h, a low-tohigh pulse will automatically be generated and internally supplied to the Timer1 gate circuitry.

19.6.3 TIMER1 GATE TOGGLE MODE

When Timer1 Gate Toggle mode is enabled, it is possible to measure the full-cycle length of a Timer1 gate signal, as opposed to the duration of a single level pulse.

The Timer1 gate source is routed through a flip-flop that changes state on every incrementing edge of the signal. See Figure 19-4 for timing details.

Timer1 Gate Toggle mode is enabled by setting the T1GTM bit of the T1GCON register. When the T1GTM bit is cleared, the flip-flop is cleared and held clear. This is necessary in order to control which edge is measured.

Note: Enabling Toggle mode at the same time as changing the gate polarity may result in indeterminate operation.

19.6.4 TIMER1 GATE SINGLE-PULSE MODE

When Timer1 Gate Single-Pulse mode is enabled, it is possible to capture a single pulse gate event. Timer1 Gate Single-Pulse mode is first enabled by setting the T1GSPM bit in the T1GCON register. Next, the T1GGO/ DONE bit in the T1GCON register must be set. The Timer1 will be fully enabled on the next incrementing edge. On the next trailing edge of the pulse, the T1GGO/ DONE bit will automatically be cleared. No other gate events will be allowed to increment Timer1 until the T1GGO/DONE bit is once again set in software. See Figure 19-5 for timing details.

If the Single Pulse Gate mode is disabled by clearing the T1GSPM bit in the T1GCON register, the T1GGO/DONE bit should also be cleared.

Enabling the Toggle mode and the Single-Pulse mode simultaneously will permit both sections to work together. This allows the cycle times on the Timer1 gate source to be measured. See Figure 19-6 for timing details.

19.6.5 TIMER1 GATE VALUE STATUS

When Timer1 Gate Value Status is utilized, it is possible to read the most current level of the gate control value. The value is stored in the T1GVAL bit in the T1GCON register. The T1GVAL bit is valid even when the Timer1 gate is not enabled (TMR1GE bit is cleared).

19.6.6 TIMER1 GATE EVENT INTERRUPT

When Timer1 Gate Event Interrupt is enabled, it is possible to generate an interrupt upon the completion of a gate event. When the falling edge of T1GVAL occurs, the TMR1GIF flag bit in the PIR1 register will be set. If the TMR1GIE bit in the PIE1 register is set, then an interrupt will be recognized.

The TMR1GIF flag bit operates even when the Timer1 gate is not enabled (TMR1GE bit is cleared).

22.4 **EUSART Baud Rate Generator** (BRG)

The Baud Rate Generator (BRG) is an 8-bit or 16-bit timer that is dedicated to the support of both the asynchronous and synchronous EUSART operation. By default, the BRG operates in 8-bit mode. Setting the BRG16 bit of the BAUDCON register selects 16-bit mode.

The SPBRGH, SPBRGL register pair determines the period of the free running baud rate timer. In Asynchronous mode the multiplier of the baud rate period is determined by both the BRGH bit of the TXSTA register and the BRG16 bit of the BAUDCON register. In Synchronous mode, the BRGH bit is ignored.

Table 22-3 contains the formulas for determining the baud rate. Example 22-1 provides a sample calculation for determining the baud rate and baud rate error.

Typical baud rates and error values for various asynchronous modes have been computed for your convenience and are shown in Table 22-3. It may be advantageous to use the high baud rate (BRGH = 1), or the 16-bit BRG (BRG16 = 1) to reduce the baud rate error. The 16-bit BRG mode is used to achieve slow baud rates for fast oscillator frequencies.

Writing a new value to the SPBRGH, SPBRGL register pair causes the BRG timer to be reset (or cleared). This ensures that the BRG does not wait for a timer overflow before outputting the new baud rate.

If the system clock is changed during an active receive operation, a receive error or data loss may result. To avoid this problem, check the status of the RCIDL bit to make sure that the receive operation is idle before changing the system clock.

EXAMPLE 22-1: CALCULATING BAUD **RATE ERROR**

For a device with Fosc of 16 MHz, desired baud rate 0

of 9600, Asynchronous mode, 8-bit BRG:

$$Desired Baud Rate = \frac{Fosc}{64([SPBRGH:SPBRGL] + 1)}$$
Solving for SPBRGH:SPBRGL:

$$X = \frac{Fosc}{0} = \frac{Fosc}{64} - 1$$

$$= \frac{16000000}{9600} - 1$$

$$= [25.042] = 25$$
Calculated Baud Rate = $\frac{16000000}{64(25 + 1)}$

$$= 9615$$

$$Error = \frac{Calc. Baud Rate - Desired Baud Rate}{Desired Baud Rate}$$

$$= \frac{(9615 - 9600)}{9600} = 0.16\%$$

C

REGISTER 24-9: CLCDATA: CLC DATA OUTPUT

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0	
—	—	—	—	MLC4OUT	MLC3OUT	MLC2OUT	MLC1OUT	
bit 7					bit 0			
Legend:								
R = Readable bit		W = Writable bit		U = Unimplemented bit, read as '0'				
u = Bit is unchanged x = Bit is unknow		nown	-n/n = Value a	at POR and BO	R/Value at all o	ther Resets		
'1' = Bit is set '0' = Bit is cleared		ared						
bit 7-4	7-4 Unimplemented: Read as '0'							
bit 3	MLC4OUT: Mirror copy of LC4OUT bit		C4OUT bit					
bit 2	MLC3OUT: Mirror copy of LC3OUT bit							
bit 1	MLC2OUT: Mirror copy of LC2OUT bit							
bit 0	MLC1OUT: Mirror copy of LC1OUT bit							

TABLE 24-3:	SUMMARY OF REGISTERS ASSOCIATED WITH CLCx
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Name	Bit7	Bit6	Bit5	Bit4	Blt3	Bit2	Bit1	Bit0	Register on Page
ANSELA	_		—	ANSA4	—	ANSA2	ANSA1	ANSA0	110
ANSELB	_	_	ANSB5 ANSE		—	—	—	—	114
ANSELC	ANSC7	ANSC6	—	—	ANSC3	ANSC2	ANSC1	ANSC0	118
CLC1CON	LC1EN	LC10E LC10UT LC1INTP		LC1INTN	LC1MODE<2:0>			263	
CLCDATA	_	_	_	_	_	MLC3OUT	MLC2OUT	MLC1OUT	271
CLC1GLS0	LC1G1D4T	LC1G1D4N	LC1G1D3T	LC1G1D3N	LC1G1D2T	LC1G1D2N	LC1G1D1T	LC1G1D1N	267
CLC1GLS1	LC1G2D4T	LC1G2D4N	LC1G2D3T	LC1G2D3N	LC1G2D2T	LC1G2D2N	LC1G2D1T	LC1G2D1N	268
CLC1GLS2	LC1G3D4T	LC1G3D4N	LC1G3D3T	LC1G3D3N	LC1G3D2T	LC1G3D2N	LC1G3D1T	LC1G3D1N	269
CLC1GLS3	LC1G4D4T	LC1G4D4N	LC1G4D3T	LC1G4D3N	LC1G4D2T	LC1G4D2N	LC1G4D1T	LC1G4D1N	270
CLC1POL	LC1POL	_	_	_	LC1G4POL	LC1G3POL	LC1G2POL	LC1G1POL	264
CLC1SEL0	_		LC1D2S<2:0>		—		LC1D1S<2:0>		265
CLC1SEL1	_		LC1D4S<2:0>		—		LC1D3S<2:0>		266
CLC2CON	LC2EN	LC2OE	LC2OUT	LC2INTP	LC2INTN	L	C2MODE<2:0	>	263
CLC2GLS0	LC2G1D4T	LC2G1D4N	LC2G1D3T	LC2G1D3N	LC2G1D2T	LC2G1D2N	LC2G1D1T	LC2G1D1N	267
CLC2GLS1	LC2G2D4T	LC2G2D4N	LC2G2D3T	LC2G2D3N	LC2G2D2T	LC2G2D2N	LC2G2D1T	LC2G2D1N	268
CLC2GLS2	LC2G3D4T	LC2G3D4N	LC2G3D3T	LC2G3D3N	LC2G3D2T	LC2G3D2N	LC2G3D1T	LC2G3D1N	269
CLC2GLS3	LC2G4D4T	LC2G4D4N	LC2G4D3T	LC2G4D3N	LC2G4D2T	LC2G4D2N	LC2G4D1T	LC2G4D1N	270
CLC2POL	LC2POL	_	—	—	LC2G4POL	LC2G3POL	LC2G2POL	LC2G1POL	264
CLC2SEL0	_		LC2D2S<2:0>		—		LC2D1S<2:0>		265
CLC2SEL1	_		LC2D4S<2:0>		—		LC2D3S<2:0>		266
CLC3CON	LC3EN	LC3OE	LC3OUT	LC3INTP	LC3INTN	L	263		
CLC3GLS0	LC3G1D4T	LC3G1D4N	LC3G1D3T	LC3G1D3N	LC3G1D2T	LC3G1D2N	LC3G1D1T	LC3G1D1N	267
CLC3GLS1	LC3G2D4T	LC3G2D4N	LC3G2D3T	LC3G2D3N	LC3G2D2T	LC3G2D2N	LC3G2D1T	LC3G2D1N	268
CLC3GLS2	LC3G3D4T	LC3G3D4N	LC3G3D3T	LC3G3D3N	LC3G3D2T	LC3G3D2N	LC3G3D1T	LC3G3D1N	269
CLC3GLS3	LC3G4D4T	LC3G4D4N	LC3G4D3T	LC3G4D3N	LC3G4D2T	LC3G4D2N	LC3G4D1T	LC3G4D1N	270
CLC3POL	LC3POL	_	_	_	LC3G4POL	LC3G3POL	LC3G2POL	LC3G1POL	264
CLC3SEL0	_		LC3D2S<2:0>		—	LC3D1S<2:0>			265
CLC3SEL1	_		LC3D4S<2:0>		—		LC3D3S<2:0>		266
CLC4CON	LC4EN	LC4OE	LC4OUT	LC4INTP	LC4INTN	L	C4MODE<2:0	>	263
CLC4GLS0	LC4G1D4T	LC4G1D4N	LC4G1D3T	LC4G1D3N	LC4G1D2T	LC4G1D2N	LC4G1D1T	LC4G1D1N	267
CLC4GLS1	LC4G2D4T	LC4G2D4N	LC4G2D3T	LC4G2D3N	LC4G2D2T	LC4G2D2N	LC4G2D1T	LC4G2D1N	268
CLC4GLS2	LC4G3D4T	LC4G3D4N	LC4G3D3T	LC4G3D3N	LC4G3D2T	LC4G3D2N	LC4G3D1T	LC4G3D1N	269
CLC4GLS3	LC4G4D4T	LC4G4D4N	LC4G4D3T	LC4G4D3N	LC4G4D2T	LC4G4D2N	LC4G4D1T	LC4G4D1N	270
CLC4POL	LC4POL	_	_	_	LC4G4POL	LC4G3POL	LC4G2POL	LC4G1POL	264
CLC4SEL0	_		LC4D2S<2:0>		—		LC4D1S<2:0>		265
CLC4SEL1	_	LC4D4S<2:0>			_	LC4D3S<2:0>			266
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	75
PIE3	_		—	—	CLC4IE	CLC3IE	CLC2IE	CLC1IE	78
PIR3	-	_	—	—	CLC4IF	CLC3IF	CLC2IF	CLC1IF	81
TRISA	-	_	TRISA5	TRISA4	(1)	TRISA2	TRISA1	TRISA0	109
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	—	—	—	—	113
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	117

 Legend:
 — = unimplemented read as '0',. Shaded cells are not used for CLC module.

 Note
 1:
 Unimplemented, read as '1'.



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Status

26.12 Register Definitions: CWG Control

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0			
GxEN	GxOEB	GxOEA	GxPOLB	GxPOLA	—	—	GxCS0			
bit 7							bit 0			
Legend:										
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'				
u = Bit is unch	anged	x = Bit is unki	nown	-n/n = Value a	at POR and BOP	R/Value at all	other Resets			
'1' = Bit is set		'0' = Bit is cle	ared	q = Value dep	pends on conditi	on				
bit 7	GxEN: CWG	x Enable bit								
	1 = Module is	s enabled								
	0 = Module is	s disabled								
bit 6	GxOEB: CW	CEB: CWGxB Output Enable bit								
	1 = CWGxB is available on appropriate I/O pin									
6.4. F				te i/O pin						
DIL 5		EXUEA: UVIGXA OUTPUT ENABLE DIT								
	0 = CWGXA	is not available	on appropriate i/	te I/O pin						
bit 4	GxPOLB: CV	VGxB Output F	olarity bit							
	1 = Output is	inverted polar	ity							
	0 = Output is	normal polarit	y							
bit 3	GxPOLA: CV	VGxA Output F	olarity bit							
	1 = Output is	s inverted polar	ity							
	0 = Output is	s normal polarit	у							
bit 2-1	Unimplemen	ted: Read as '	0'							
bit 0	GxCS0: CWC	Gx Clock Sourc	e Select bit							
	1 = HFINTOS	SC								
	0 = FUSC									

REGISTER 26-1: CWGxCON0: CWG CONTROL REGISTER 0

28.0 INSTRUCTION SET SUMMARY

Each instruction is a 14-bit word containing the operation code (opcode) and all required operands. The opcodes are broken into three broad categories.

- · Byte Oriented
- · Bit Oriented
- · Literal and Control

The literal and control category contains the most varied instruction word format.

Table 28-3 lists the instructions recognized by the MPASM $^{\rm TM}$ assembler.

All instructions are executed within a single instruction cycle, with the following exceptions, which may take two or three cycles:

- Subroutine takes two cycles (CALL, CALLW)
- Returns from interrupts or subroutines take two cycles (RETURN, RETLW, RETFIE)
- Program branching takes two cycles (GOTO, BRA, BRW, BTFSS, BTFSC, DECFSZ, INCSFZ)
- One additional instruction cycle will be used when any instruction references an indirect file register and the file select register is pointing to program memory.

One instruction cycle consists of 4 oscillator cycles; for an oscillator frequency of 4 MHz, this gives a nominal instruction execution rate of 1 MHz.

All instruction examples use the format '0xhh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

28.1 Read-Modify-Write Operations

Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator 'd'. A read operation is performed on a register even if the instruction writes to that register.

TABLE 28-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
х	Don't care location (= 0 or 1). The assembler will generate code with x = 0 . It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.
n	FSR or INDF number. (0-1)
mm	Pre-post increment-decrement mode selection

TABLE 28-2: ABBREVIATION DESCRIPTIONS

Field	Description					
PC	Program Counter					
TO	Time-Out bit					
С	Carry bit					
DC	Digit Carry bit					
Z	Zero bit					
PD	Power-Down bit					

PIC16LF1508/9		Operating Conditions: (unless otherwise stated) Low-Power Sleep Mode								
PIC16F1508/9		Low-Power Sleep Mode, VREGPM = 1								
Param.	aram.		T 1	Max.	Max.	11-14-	Conditions			
No.	Device Characteristics	wiin.	турт	+85°C	+125°C	Units	Vdd	Note		
D022	Base IPD		0.020	1.0	8.0	μA	1.8	WDT, BOR, FVR and SOSC		
		—	0.025	2.0	9.0	μA	3.0	disabled, all Peripherals inactive		
D022	Base IPD	_	0.25	3.0	10	μA	2.3	WDT, BOR, FVR and SOSC		
		—	0.30	4.0	12	μA	3.0	disabled, all Peripherals inactive,		
		—	0.40	6.0	15	μA	5.0	Low-Power Sleep mode		
D022A	Base IPD		9.8	16	18	μΑ	2.3	WDT, BOR, FVR and SOSC		
			10.3	18	20	μA	3.0	disabled, all Peripherals inactive,		
		—	11.5	21	26	μA	5.0	VREGPM = 0		
D023		—	0.26	2.0	9.0	μA	1.8	WDT Current		
		_	0.44	3.0	10	μA	3.0			
D023		_	0.43	6.0	15	μA	2.3	WDT Current		
		_	0.53	7.0	20	μA	3.0			
		—	0.64	8.0	22	μA	5.0			
D023A		_	15	28	30	μA	1.8	FVR Current		
		—	18	30	33	μA	3.0			
D023A			18	33	35	μA	2.3	FVR Current		
			19	35	37	μA	3.0			
		—	20	37	39	μA	5.0			
D024		—	6.0	17	20	μA	3.0	BOR Current		
D024			7.0	17	30	μA	3.0	BOR Current		
		—	8.0	20	40	μA	5.0			
D24A		—	0.1	4.0	10	μΑ	3.0	LPBOR Current		
D24A		_	0.35	5.0	14	μA	3.0	LPBOR Current		
		—	0.45	8.0	17	μA	5.0			

TABLE 29-3: POWER-DOWN CURRENTS (IPD)^(1,2)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral ∆ current can be determined by subtracting the base IPD current from this limit. Max. values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to Vss.

3: ADC clock source is FRC.

FIGURE 29-5: CLOCK TIMING



TABLE 29-7: CLOCK OSCILLATOR TIMING REQUIREMENTS

Param. No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions
OS01	Fosc	External CLKIN Frequency ⁽¹⁾	DC		0.5	MHz	External Clock (ECL)
			DC	—	4	MHz	External Clock (ECM)
			DC	—	20	MHz	External Clock (ECH)
		Oscillator Frequency ⁽¹⁾	_	32.768	_	kHz	LP Oscillator
			0.1	—	4	MHz	XT Oscillator
			1	—	4	MHz	HS Oscillator
			1	—	20	MHz	HS Oscillator, VDD > 2.7V
			DC	—	4	MHz	EXTRC, VDD > 2.0V
OS02	Tosc	External CLKIN Period ⁽¹⁾	27		×	μs	LP Oscillator
			250	—	∞	ns	XT Oscillator
			50	—	∞	ns	HS Oscillator
			50	—	∞	ns	External Clock (EC)
		Oscillator Period ⁽¹⁾	_	30.5	_	μs	LP Oscillator
			250	—	10,000	ns	XT Oscillator
			50	—	1,000	ns	HS Oscillator
			250	—	—	ns	EXTRC
OS03	TCY	Instruction Cycle Time ⁽¹⁾	200	Тсү	DC	ns	Tcy = 4/Fosc
OS04*	TosH,	External CLKIN High	2	_	_	μs	LP Oscillator
	TosL	External CLKIN Low	100	—	—	ns	XT Oscillator
			20	—	—	ns	HS Oscillator
OS05*	TosR,	External CLKIN Rise	0	—	—	ns	LP Oscillator
	TosF	External CLKIN Fall	0	—	—	ns	XT Oscillator
			0	—	—	ns	HS Oscillator

Standard Operating Conditions (unless otherwise stated)

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (TcY) equals four times the input oscillator time base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min" values with an external clock applied to CLKIN pin. When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

FIGURE 29-8: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING











31.0 DEVELOPMENT SUPPORT

The PIC[®] microcontrollers (MCU) and dsPIC[®] digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
 - MPLAB[®] X IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB XC Compiler
 - MPASM[™] Assembler
 - MPLINK[™] Object Linker/ MPLIB[™] Object Librarian
 - MPLAB Assembler/Linker/Librarian for Various Device Families
- Simulators
 - MPLAB X SIM Software Simulator
- Emulators
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
 - MPLAB ICD 3
 - PICkit™ 3
- Device Programmers
- MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

31.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows[®], Linux and Mac $OS^{®}$ X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- · Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- · Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- · Call graph window

Project-Based Workspaces:

- Multiple projects
- · Multiple tools
- Multiple configurations
- Simultaneous debugging sessions

File History and Bug Tracking:

- Local file history feature
- · Built-in support for Bugzilla issue tracker

20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	С		7.20	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2072A