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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	17
Program Memory Size	14KB (8K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x10b; D/A 1x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	20-SSOP (0.209", 5.30mm Width)
Supplier Device Package	20-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1509-e-ss

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# 3.2.1 READING PROGRAM MEMORY AS DATA

There are two methods of accessing constants in program memory. The first method is to use tables of RETLW instructions. The second method is to set an FSR to point to the program memory.

## 3.2.1.1 RETLW Instruction

The RETLW instruction can be used to provide access to tables of constants. The recommended way to create such a table is shown in Example 3-1.

EXAMPLE 3-1: RETLW INSTRUCTION

constants	
BRW	;Add Index in W to
	;program counter to
	;select data
RETLW DATA0	;Index0 data
RETLW DATA1	;Index1 data
RETLW DATA2	
RETLW DATA3	
my_function	
; LOTS OF CODE	
MOVLW DATA_INI	DEX
call constants	
; THE CONSTANT IS	IN W

The BRW instruction makes this type of table very simple to implement. If your code must remain portable with previous generations of microcontrollers, then the BRW instruction is not available so the older table read method must be used.

## 3.2.1.2 Indirect Read with FSR

The program memory can be accessed as data by setting bit 7 of the FSRxH register and reading the matching INDFx register. The MOVIW instruction will place the lower eight bits of the addressed word in the W register. Writes to the program memory cannot be performed via the INDF registers. Instructions that access the program memory via the FSR require one extra instruction cycle to complete. Example 3-2 demonstrates accessing the program memory via an FSR.

The HIGH operator will set bit<7> if a label points to a location in program memory.

## EXAMPLE 3-2: ACCESSING PROGRAM MEMORY VIA FSR

constants
DW DATAO ;First constant
DW DATAI Second constant
DW DATA2
DW DATA3
my_function
; LOTS OF CODE
MOVLW DATA_INDEX
ADDLW LOW constants
MOVWF FSR1L
MOVLW HIGH constants;MSb sets
automatically
MOVWF FSR1H
BTFSC STATUS, C ;carry from ADDLW?
INCF FSR1h, f ;yes
MOVIW 0[FSR1]
;THE PROGRAM MEMORY IS IN W

## 3.3.1.1 STATUS Register

The STATUS register, shown in Register 3-1, contains:

- the arithmetic status of the ALU
- · the Reset status

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

## REGISTER 3-1: STATUS: STATUS REGISTER

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS register as '000u uluu' (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect any Status bits. For other instructions not affecting any Status bits (Refer to **Section 28.0 "Instruction Set Summary"**).

Note 1: The <u>C</u> and <u>DC</u> bits operate as Borrow and <u>Digit</u> Borrow out bits, respectively, in subtraction.

U-0	U-0	U-0	R-1/q	R-1/q R/W-0/u		R/W-0/u	R/W-0/u	
		_	TO	PD	PD Z		C <sup>(1)</sup>	
bit 7					•		bit 0	
Legend:								
R = Readable bit W = Writable bit			bit	U = Unimplemented bit, read as '0'				
u = Bit is unchanged x = Bit is unknown			-n/n = Value at POR and BOR/Value at all other Resets					
'1' = Bit is set '0' = Bit is cleared			q = Value depends on condition					

bit 7-5	Unimplemented: Read as '0'
bit 4	TO: Time-Out bit
	<ul> <li>1 = After power-up, CLRWDT instruction or SLEEP instruction</li> <li>0 = A WDT time-out occurred</li> </ul>
bit 3	PD: Power-Down bit
	<ul> <li>1 = After power-up or by the CLRWDT instruction</li> <li>0 = By execution of the SLEEP instruction</li> </ul>
bit 2	Z: Zero bit
	<ul> <li>1 = The result of an arithmetic or logic operation is zero</li> <li>0 = The result of an arithmetic or logic operation is not zero</li> </ul>
bit 1	DC: Digit Carry/Digit Borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions) <sup>(1)</sup>
	<ul> <li>1 = A carry-out from the 4th low-order bit of the result occurred</li> <li>0 = No carry-out from the 4th low-order bit of the result</li> </ul>
bit 0	C: Carry/Borrow bit <sup>(1)</sup> (ADDWF, ADDLW, SUBLW, SUBWF instructions) <sup>(1)</sup>
	<ul> <li>1 = A carry-out from the Most Significant bit of the result occurred</li> <li>0 = No carry-out from the Most Significant bit of the result occurred</li> </ul>

**Note 1:** For Borrow, the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high-order or low-order bit of the source register.

# 7.3 Interrupts During Sleep

Some interrupts can be used to wake from Sleep. To wake from Sleep, the peripheral must be able to operate without the system clock. The interrupt source must have the appropriate Interrupt Enable bit(s) set prior to entering Sleep.

On waking from Sleep, if the GIE bit is also set, the processor will branch to the interrupt vector. Otherwise, the processor will continue executing instructions after the SLEEP instruction. The instruction directly after the SLEEP instruction will always be executed before branching to the ISR. Refer to **Section 8.0 "Power-Down Mode (Sleep)"** for more details.

# 7.4 INT Pin

The INT pin can be used to generate an asynchronous edge-triggered interrupt. This interrupt is enabled by setting the INTE bit of the INTCON register. The INTEDG bit of the OPTION\_REG register determines on which edge the interrupt will occur. When the INTEDG bit is set, the rising edge will cause the interrupt. When the INTEDG bit is clear, the falling edge will cause the interrupt. The INTF bit of the INTCON register will be set when a valid edge appears on the INT pin. If the GIE and INTE bits are also set, the processor will redirect program execution to the interrupt vector.

# 7.5 Automatic Context Saving

Upon entering an interrupt, the return PC address is saved on the stack. Additionally, the following registers are automatically saved in the shadow registers:

- W register
- STATUS register (except for TO and PD)
- BSR register
- FSR registers
- PCLATH register

Upon exiting the Interrupt Service Routine, these registers are automatically restored. Any modifications to these registers during the ISR will be lost. If modifications to any of these registers are desired, the corresponding shadow register should be modified and the value will be restored when exiting the ISR. The shadow registers are available in Bank 31 and are readable and writable. Depending on the user's application, other registers may also need to be saved.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	—	ANSA4	—	ANSA2	ANSA1	ANSA0	110
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	75
IOCAF	—	_	IOCAF5	IOCAF4	IOCAF3	IOCAF2	IOCAF1	IOCAF0	121
IOCAN	—	—	IOCAN5	IOCAN4	IOCAN3	IOCAN2	IOCAN1	IOCAN0	121
IOCAP	—	—	IOCAP5	IOCAP4	IOCAP3	IOCAP2	IOCAP1	IOCAP0	121
IOCBF	IOCBF7	IOCBF6	IOCBF5	IOCBF4	_	_	_	_	122
IOCBN	IOCBN7	IOCBN6	IOCBN5	IOCBN4	_	_	_	_	122
IOCBP	IOCBP7	IOCBP6	IOCBP5	IOCBP4	_	_	_	_	122
TRISA	_	_	TRISA5	TRISA4	—(1)	TRISA2	TRISA1	TRISA0	109
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	_	_	_	_	113

## TABLE 12-1: SUMMARY OF REGISTERS ASSOCIATED WITH INTERRUPT-ON-CHANGE

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by interrupt-on-change.

**Note 1:** Unimplemented, read as '1'.

# 17.0 COMPARATOR MODULE

Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. Comparators are very useful mixed signal building blocks because they provide analog functionality independent of program execution. The analog comparator module includes the following features:

- · Independent comparator control
- · Programmable input selection
- · Comparator output is available internally/externally
- · Programmable output polarity
- Interrupt-on-change
- Wake-up from Sleep
- Programmable Speed/Power optimization
- PWM shutdown
- Programmable and fixed voltage reference

# 17.1 Comparator Overview

A single comparator is shown in Figure 17-2 along with the relationship between the analog input levels and the digital output. When the analog voltage at VIN+ is less than the analog voltage at VIN-, the output of the comparator is a digital low level. When the analog voltage at VIN+ is greater than the analog voltage at VIN-, the output of the comparator is a digital high level.

The comparators available for this device are listed in Table 17-1.

## TABLE 17-1: AVAILABLE COMPARATORS

Device	C1	C2
PIC16(L)F1508	•	•
PIC16(L)F1509	•	•

## FIGURE 17-1: COMPARATOR MODULE SIMPLIFIED BLOCK DIAGRAM



R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W/HC-0/u	R-x/x	R/W-0/u	R/W-0/u
TMR1GE	T1GPOL	POL T1GTM T1GSPM		T1GGO/ DONE	T1GVAL	T1GSS<1:0>	
bit 7	•	•					bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplem	nented bit, read	d as '0'	
u = Bit is uncha	anged	x = Bit is unkr	nown	-n/n = Value a	t POR and BO	R/Value at all o	ther Resets
'1' = Bit is set		'0' = Bit is clea	ared	HC = Bit is cle	eared by hardw	are	
bit 7 <b>TMR1GE:</b> Timer1 Gate Enable bit <u>If TMR1ON = 0</u> : This bit is ignored <u>If TMR1ON = 1</u> : 1 = Timer1 counting is controlled by the Timer1 gate function							
bit 6	T1GPOL: Tim	ner1 Gate Pola	rity bit				
	1 = Timer1 g 0 = Timer1 g	ate is active-hi ate is active-lo	gh (Timer1 cou w (Timer1 cou	unts when gate nts when gate is	is high) s low)		
bit 5	T1GTM: Time	er1 Gate Toggle	e Mode bit				
	1 = Timer1 G 0 = Timer1 G Timer1 gate fl	ate Toggle mo ate Toggle mo lip-flop toggles	de is enabled de is disabled on every risin	and toggle flip- g edge.	flop is cleared		
bit 4	T1GSPM: Tin	ner1 Gate Sing	le-Pulse Mode	e bit			
	1 = Timer1 ga 0 = Timer1 ga	ate Single-Puls ate Single-Puls	se mode is ena se mode is dis	abled and is cor abled	ntrolling Timer1	gate	
bit 3	T1GGO/DON	E: Timer1 Gate	e Single-Pulse	Acquisition Sta	itus bit		
	<ul> <li>1 = Timer1 gate single-pulse acquisition is ready, waiting for an edge</li> <li>0 = Timer1 gate single-pulse acquisition has completed or has not been started</li> </ul>						
bit 2	<b>T1GVAL:</b> Timer1 Gate Value Status bit Indicates the current state of the Timer1 gate that could be provided to TMR1H:TMR1L.						
bit 1-0	Unaffected by Timer1 Gate Enable (TMR1GE). <b>T1GSS&lt;1:0&gt;:</b> Timer1 Gate Source Select bits 11 = Comparator 2 optionally synchronized output (C2OUT_sync) 10 = Comparator 1 optionally synchronized output (C1OUT_sync) 01 = Timer0 overflow output (T0_overflow) 00 = Timer1 gate pin (T1G)						

# REGISTER 19-2: T1GCON: TIMER1 GATE CONTROL REGISTER

## 21.6.4 I<sup>2</sup>C MASTER MODE START CONDITION TIMING

To initiate a Start condition (Figure 21-26), the user sets the Start Enable bit, SEN bit of the SSPxCON2 register. If the SDAx and SCLx pins are sampled high, the Baud Rate Generator is reloaded with the contents of SSPxADD<7:0> and starts its count. If SCLx and SDAx are both sampled high when the Baud Rate Generator times out (TBRG), the SDAx pin is driven low. The action of the SDAx being driven low while SCLx is high is the Start condition and causes the S bit of the SSPxADD<7:0> and resumes its count. When the Baud Rate Generator times out (TBRG), the SDAx bit of the SSPxSTAT1 register to be set. Following this, the Baud Rate Generator is reloaded with the contents of SSPxADD<7:0> and resumes its count. When the Baud Rate Generator times out (TBRG), the SEN bit of the SSPxCON2 register will be automatically cleared

by hardware; the Baud Rate Generator is suspended, leaving the SDAx line held low and the Start condition is complete.

- Note 1: If at the beginning of the Start condition, the SDAx and SCLx pins are already sampled low, or if during the Start condition, the SCLx line is sampled low before the SDAx line is driven low, a bus collision occurs, the Bus Collision Interrupt Flag, BCLxIF, is set, the Start condition is aborted and the I<sup>2</sup>C module is reset into its Idle state.
  - 2: The Philips I<sup>2</sup>C Specification states that a bus collision cannot occur on a Start.



# 22.0 ENHANCED UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (EUSART)

The Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART) module is a serial I/O communications peripheral. It contains all the clock generators, shift registers and data buffers necessary to perform an input or output serial data transfer independent of device program execution. The EUSART, also known as a Serial Communications Interface (SCI), can be configured as a full-duplex asynchronous system or half-duplex synchronous Full-Duplex is useful system. mode for communications with peripheral systems, such as CRT terminals and personal computers. Half-Duplex Synchronous mode is intended for communications with peripheral devices, such as A/D or D/A integrated circuits, serial EEPROMs or other microcontrollers. These devices typically do not have internal clocks for baud rate generation and require the external clock signal provided by a master synchronous device.

The EUSART module includes the following capabilities:

- · Full-duplex asynchronous transmit and receive
- · Two-character input buffer
- · One-character output buffer
- · Programmable 8-bit or 9-bit character length
- · Address detection in 9-bit mode
- Input buffer overrun error detection
- · Received character framing error detection
- · Half-duplex synchronous master
- Half-duplex synchronous slave
- Programmable clock polarity in synchronous modes
- · Sleep operation

The EUSART module implements the following additional features, making it ideally suited for use in Local Interconnect Network (LIN) bus systems:

- · Automatic detection and calibration of the baud rate
- · Wake-up on Break reception
- · 13-bit Break character transmit

Block diagrams of the EUSART transmitter and receiver are shown in Figure 22-1 and Figure 22-2.

The EUSART transmit output (TX\_out) is available to the TX/CK pin and internally to the following peripherals:

Configurable Logic Cell (CLC)

## FIGURE 22-1: EUSART TRANSMIT BLOCK DIAGRAM



R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LCxG4D4T	LCxG4D4N	LCxG4D3T	LCxG4D3N	LCxG4D2T	LCxG4D2N	LCxG4D1T	LCxG4D1N
bit 7			•			•	bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimpler	mented bit, read	as '0'	
u = Bit is uncha	anged	x = Bit is unkr	nown	-n/n = Value a	at POR and BO	R/Value at all c	other Resets
'1' = Bit is set		'0' = Bit is clea	ared				
bit 7	LCxG4D4T: (	Gate 4 Data 4 1	rue (non-inve	rted) bit			
	1 = lcxd4T is	gated into loxo	<u>1</u> 4				
	0 = 1cxd41 is	not gated into	lcxg4				
bit 6	LCxG4D4N:	Gate 4 Data 4	Negated (invei	rted) bit			
	1 = 1CX04N is 0 = 1CX04N is	s gated into icx	J4 Jexa4				
bit 5		Sate 4 Data 3 1	True (non-inve	rted) hit			
bit 0	1 = lcxd3T is	aated into loxo	14	ned) bit			
	0 = lcxd3T is	not gated into	lcxg4				
bit 4	LCxG4D3N:	Gate 4 Data 3 I	Negated (inve	rted) bit			
	1 = Icxd3N is	gated into lcx	g4				
	0 = Icxd3N is	not gated into	lcxg4				
bit 3	LCxG4D2T: (	Gate 4 Data 2 1	rue (non-inve	rted) bit			
	1 = lcxd2T is	gated into loxo	<u>1</u>				
1.11.0	0 = 100021 is	not gated into	ICXg4				
DIT 2	LCXG4D2N:	Gate 4 Data 2	Negated (Invel	rted) bit			
	$\perp = 10002 \text{N is}$ 0 = 10002 N is	s galed into icx	J4 Jexa4				
hit 1		Gate 4 Data 1 1	rue (non-inve	rted) hit			
Sit	1 = lcxd1T is	aated into Icxo	14				
	0 = lcxd1T is	not gated into	lcxg4				
bit 0	LCxG4D1N:	Gate 4 Data 1	Negated (inver	rted) bit			
	1 = Icxd1N is	gated into lcxg	g4				
	0 = Icxd1N is	not gated into	lcxg4				

# REGISTER 24-8: CLCxGLS3: GATE 4 LOGIC SELECT REGISTER

# PIC16(L)F1508/9

## FIGURE 27-2: PICkit<sup>™</sup> PROGRAMMER STYLE CONNECTOR INTERFACE



For additional interface recommendations, refer to your specific device programmer manual prior to PCB design.

It is recommended that isolation devices be used to separate the programming pins from other circuitry. The type of isolation is highly dependent on the specific application and may include devices such as resistors, diodes, or even jumpers. See Figure 27-3 for more information.

## FIGURE 27-3: TYPICAL CONNECTION FOR ICSP™ PROGRAMMING



## 29.4 AC Characteristics

Timing Parameter Symbology has been created with one of the following formats:

1. TppS2ppS

2. TppS

Т			
F	Frequency	Т	Time
Lowerc	case letters (pp) and their meanings:		
рр			
сс	CCP1	osc	CLKIN
ck	CLKOUT	rd	RD
CS	CS	rw	RD or WR
di	SDIx	SC	SCKx
do	SDO	SS	SS
dt	Data in	tO	ТОСКІ
io	I/O PORT	t1	T1CKI
mc	MCLR	wr	WR
Upperc	case letters and their meanings:		
S			
F	Fall	Р	Period
Н	High	R	Rise
I	Invalid (High-impedance)	V	Valid
L	Low	Z	High-impedance

## FIGURE 29-4: LOAD CONDITIONS



# TABLE 29-13: ANALOG-TO-DIGITAL CONVERTER (ADC) CHARACTERISTICS<sup>(1,2,3)</sup>

VDD = 3	VDD = 3.0V, TA = 25°C									
Param. No.	Sym.	Characteristic	Min.	Тур†	Max.	Units	Conditions			
AD01	NR	Resolution	—	—	10	bit				
AD02	EIL	Integral Error	_	±1	±1.7	LSb	VREF = 3.0V			
AD03	Edl	Differential Error	—	±1	±1	LSb	No missing codes VREF = 3.0V			
AD04	EOFF	Offset Error	_	±1	±2.5	LSb	Vref = 3.0V			
AD05	Egn	Gain Error	_	±1	±2.0	LSb	VREF = 3.0V			
AD06	VREF	Reference Voltage	1.8	—	Vdd	V	VREF = (VRPOS - VRNEG) (Note 4)			
AD07	VAIN	Full-Scale Range	Vss	_	VREF	V				
AD08	Zain	Recommended Impedance of Analog Voltage Source	_	_	10	kΩ	Can go higher if external 0.01µF capacitor is present on input pin.			
*										

These parameters are characterized but not tested.

Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not t tested.

Note 1:Total Absolute Error includes integral, differential, offset and gain errors.

2: The ADC conversion result never decreases with an increase in the input voltage and has no missing codes.

3: See Section 30.0 "DC and AC Characteristics Graphs and Charts" for operating characterization.

4: ADC VREF is selected by ADPREF<0> bit.

# PIC16(L)F1508/9









# PIC16(L)F1508/9









# 32.2 Package Details

The following sections give the technical details of the packages.

# 20-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		INCHES		
Dimension	n Limits	MIN	NOM	MAX	
Number of Pins	N		20		
Pitch	е	.100 BSC			
Top to Seating Plane	А	-	-	.210	
Molded Package Thickness	A2	.115	.130	.195	
Base to Seating Plane	A1	.015	-	-	
Shoulder to Shoulder Width	E	.300	.310	.325	
Molded Package Width	E1	.240	.250	.280	
Overall Length	D	.980	1.030	1.060	
Tip to Seating Plane	L	.115	.130	.150	
Lead Thickness	С	.008	.010	.015	
Upper Lead Width	b1	.045	.060	.070	
Lower Lead Width	b	.014	.018	.022	
Overall Row Spacing §	eB	-	-	.430	

### Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. § Significant Characteristic.
- 3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- 4. Dimensioning and tolerancing per ASME Y14.5M.
  - BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-019B

# 20-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging









VIEW A-A

Microchip Technology Drawing C04-094C Sheet 1 of 2

20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units	MILLIMETERS		
Dimension	Dimension Limits		NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	С		7.20	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2072A

# 20-Lead Plastic Quad Flat, No Lead Package (ML) – 4x4x0.9 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	Units		MILLIMETERS		
Dimen	sion Limits	MIN	NOM	MAX	
Number of Pins	Ν		20		
Pitch	е	0.50 BSC			
Overall Height	А	0.80	0.90	1.00	
Standoff	A1	0.00	0.02	0.05	
Contact Thickness	A3	0.20 REF			
Overall Width	E	4.00 BSC			
Exposed Pad Width	E2	2.60	2.70	2.80	
Overall Length	D	4.00 BSC			
Exposed Pad Length	D2	2.60	2.70	2.80	
Contact Width	b	0.18	0.25	0.30	
Contact Length	L	0.30	0.40	0.50	
Contact-to-Exposed Pad	K	0.20	_	_	

### Notes:

- 1. Pin 1 visual index feature may vary, but must be located within the hatched area.
- 2. Package is saw singulated.
- 3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-126B

# 20-Lead Ultra Thin Plastic Quad Flat, No Lead Package (GZ) - 4x4x0.5 mm Body [UQFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



# RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			2.80
Optional Center Pad Length	Y2			2.80
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X20)	X1			0.30
Contact Pad Length (X20)	Y1			0.80
Contact Pad to Center Pad (X20)	G1	0.20		

## Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2255A