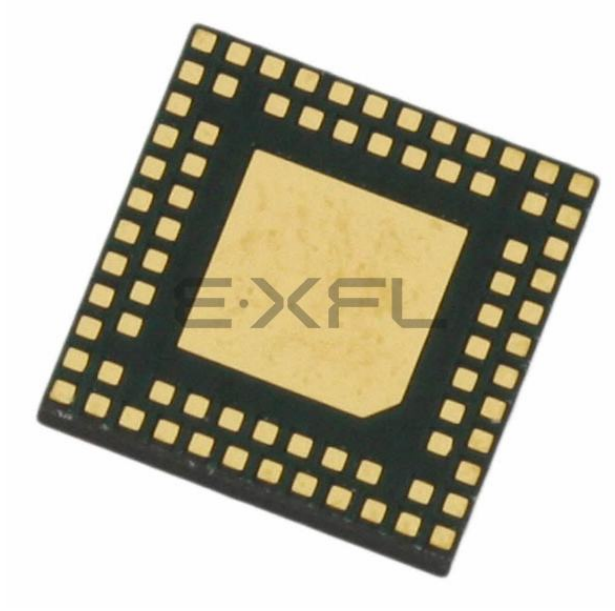

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, LCD, POR, PWM, WDT
Number of I/O	57
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	76-VFQFN Dual Rows, Exposed Pad
Supplier Device Package	76-DQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f960-b-gm

Table 4.6. Reset Electrical Characteristics

V_{BAT} = 1.8 to 3.8 V, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
$\overline{RST}$ Output Low Voltage	I_{OL} = 1.4 mA,	—	—	0.6	V
$\overline{RST}$ Input High Voltage	V_{BAT} = 2.0 to 3.8 V	V_{BAT} – 0.6	—	—	V
	V_{BAT} = 1.8 to 2.0 V	0.7 x V_{BAT}	—	—	V
$\overline{RST}$ Input Low Voltage	V_{BAT} = 2.0 to 3.8 V	—	—	0.6	V
	V_{BAT} = 1.8 to 2.0 V	—	—	0.3 x V_{BAT}	V
$\overline{RST}$ Input Pullup Current	$\overline{RST}$ = 0.0 V, V_{BAT} = 1.8 V	—	4	—	µA
	$\overline{RST}$ = 0.0 V, V_{BAT} = 3.8 V	—	20	35	
VBAT Monitor Threshold (V_{RST})*	Early Warning	1.8	1.85	1.9	V
	Reset Trigger (all power modes except Sleep)	1.7	1.75	1.8	
VBAT Ramp Time for Power On*	VBAT Ramp from 0–1.8 V	—	—	3	ms
POR Monitor Threshold (V_{POR})	Brownout Condition (V_{BAT} Falling)	0.45	0.7	1.0	V
	Recovery from Brownout (V_{BAT} Rising)	—	1.75	—	
Missing Clock Detector Timeout	Time from last system clock rising edge to reset initiation	100	650	1000	µs
Minimum System Clock w/ Missing Clock Detector Enabled	System clock frequency which triggers a missing clock detector timeout	—	7	10	kHz
Reset Time Delay	Delay between release of any reset source and code execution at location 0x0000	—	10	—	µs
Minimum $\overline{RST}$ Low Time to Generate a System Reset		15	—	—	µs
Digital/Analog Monitor Turn-on Time		—	300	—	ns
Digital Monitor Supply Current		—	14	—	µA
Analog Monitor Supply Current		—	14	—	µA

***Note:** The VBAT monitor electical specifications apply to both the analog and digital VBAT monitors (“SFR Definition 22.1. VDM0CN: VDD Supply Monitor Control” on page 282).

5.2.4. Settling Time Requirements

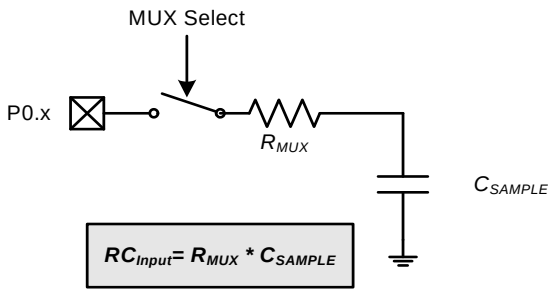
A minimum amount of tracking time is required before each conversion can be performed, to allow the sampling capacitor voltage to settle. This tracking time is determined by the AMUX0 resistance, the ADC0 sampling capacitance, any external source resistance, and the accuracy required for the conversion. Note that in low-power tracking mode, three SAR clocks are used for tracking at the start of every conversion. For many applications, these three SAR clocks will meet the minimum tracking time requirements, and higher values for the external source impedance will increase the required tracking time.

Figure 5.4 shows the equivalent ADC0 input circuit. The required ADC0 settling time for a given settling accuracy (SA) may be approximated by Equation . When measuring the Temperature Sensor output or V_{DD} with respect to GND, R_{TOTAL} reduces to R_{MUX}. See Table 4.12 for ADC0 minimum settling time requirements as well as the mux impedance and sampling capacitor values.

$$t = \ln\left(\frac{2^n}{SA}\right) \times R_{TOTAL} C_{SAMPLE}$$

ADC0 Settling Time Requirements

Where:
SA is the settling accuracy, given as a fraction of an LSB (for example, 0.25 to settle within 1/4 LSB)
t is the required settling time in seconds
R_{TOTAL} is the sum of the AMUX0 resistance and any external source resistance.
n is the ADC resolution in bits (10).



Note: The value of CSAMPLE depends on the PGA Gain. See Table 4.12 for details.

Figure 5.4. ADC0 Equivalent Input Circuits

5.2.5. Gain Setting

The ADC has gain settings of 1x and 0.5x. In 1x mode, the full scale reading of the ADC is determined directly by V_{REF}. In 0.5x mode, the full-scale reading of the ADC occurs when the input voltage is V_{REF} x 2. The 0.5x gain setting can be useful to obtain a higher input Voltage range when using a small V_{REF} voltage, or to measure input voltages that are between V_{REF} and V_{DD}. Gain settings for the ADC are controlled by the AMP0GN bit in register ADC0CF.

8.2. CIP-51 Register Descriptions

Following are descriptions of SFRs related to the operation of the CIP-51 System Controller. Reserved bits should not be set to logic l. Future product versions may use these bits to implement new features in which case the reset value of the bit will be logic 0, selecting the feature's default state. Detailed descriptions of the remaining SFRs are included in the sections of the data sheet associated with their corresponding system function.

SFR Definition 8.1. DPL: Data Pointer Low Byte

Bit	7	6	5	4	3	2	1	0
Name	DPL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = All Pages; SFR Address = 0x82

Bit	Name	Function
7:0	DPL[7:0]	**Data Pointer Low.** The DPL register is the low byte of the 16-bit DPTR. DPTR is used to access indirectly addressed flash memory or XRAM.

SFR Definition 8.2. DPH: Data Pointer High Byte

Bit	7	6	5	4	3	2	1	0
Name	DPH[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = All Pages; SFR Address = 0x83

Bit	Name	Function
7:0	DPH[7:0]	**Data Pointer High.** The DPH register is the high byte of the 16-bit DPTR. DPTR is used to access indirectly addressed flash memory or XRAM.

Table 10.1. EMIF Pinout (C8051F960/2/4/6/8)

Multiplexed Mode		
Signal Name	**Port Pin**	
	8-Bit Mode[1]	**16-Bit Mode[2]**
$\overline{RD}$	P3.6	P3.6
$\overline{WR}$	P3.7	P3.7
ALE	P3.5	P3.5
AD0	P6.0	P6.0
AD1	P6.1	P6.1
AD2	P6.2	P6.2
AD3	P6.3	P6.3
AD4	P6.4	P6.4
AD5	P6.5	P6.5
AD6	P6.6	P6.6
AD7	P6.7	P6.7
A8	—	P5.0
A9	—	P5.1
A10	—	P5.2
A11	—	P5.3
A12	—	P5.4
A13	—	P5.5
A14	—	P5.6
A15	—	P5.7
—	—	—
—	—	—
—	—	—
—	—	—
—	—	—
—	—	—
—	—	—
Required I/O:	**11**	**19**

Non Multiplexed Mode		
Signal Name	**Port Pin**	
	8-Bit Mode [1]	**16-Bit Mode[2]**
$\overline{RD}$	P3.6	P3.6
$\overline{WR}$	P3.7	P3.7
D0	P6.0	P6.0
D1	P6.1	P6.1
D2	P6.2	P6.2
D3	P6.3	P6.3
D4	P6.4	P6.4
D5	P6.5	P6.5
D6	P6.6	P6.6
D7	P6.7	P6.7
A0	P5.0	P5.0
A1	P5.1	P5.1
A2	P5.2	P5.2
A3	P5.3	P5.3
A4	P5.4	P5.4
A5	P5.5	P5.5
A6	P5.6	P5.6
A7	P5.7	P5.7
A8	—	P4.0
A9	—	P4.1
A10	—	P4.2
A11	—	P4.3
A12	—	P4.4
A13	—	P4.5
A14	—	P4.6
A15	—	P4.7
Required I/O:	**18**	**26**

Notes:
1. Using 8-bit movx instruction without bank select.
2. Using 16-bit movx instruction.

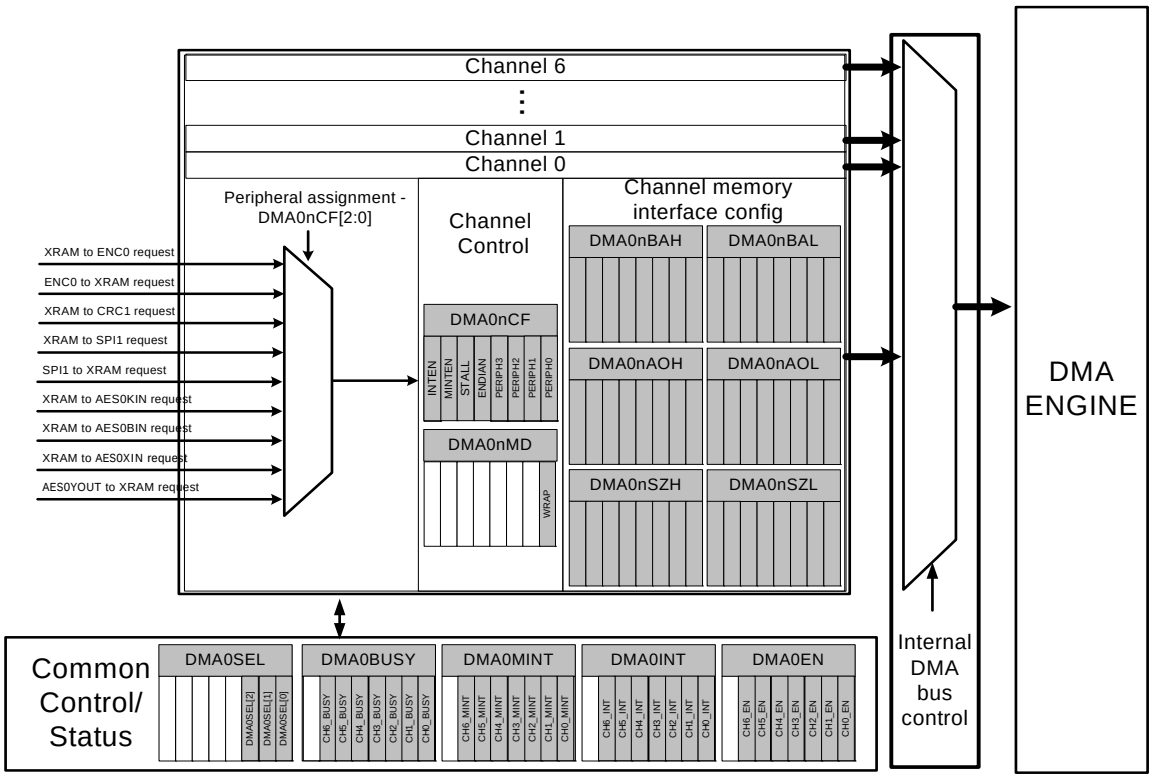


Figure 11.1. DMA0 Block Diagram

11.1. DMA0 Architecture

The first step in configuring a DMA0 channel is to select the desired channel for data transfer using DMA0-SEL[2:0] bits (DMA0SEL). After setting the DMA0 channel, firmware can address channel-specific registers such as DMA0NCF, DMA0NBAH/L, DMA0NAOH/L, and DMA0NSZH/L. Once firmware selects a channel, the subsequent SFR configuration applies to the DMA0 transfer of that selected channel.

Each DMA0 channel consists of an SFR assigning the channel to a peripheral, a channel control register and a set of SFRs that describe XRAM and SFR addresses to be used during data transfer (See Figure 11.1). The peripheral assignment bits of DMA0nCF select one of the eight data transfer functions. The selected channel can choose the desired function by writing to the PERIPH[2:0] bits (DMA0NCF[2:0]).

The control register DMA0NCF of each channel configures the endian-ness of the data in XRAM, stall enable, full-length interrupt enable and mid-point interrupt enable. When a channel is stalled by setting the STALL bit (DMA0NCF.5), DMA0 transfers in progress will not be aborted, but new DMA0 transfers will be blocked until the stall status of the channel is reset. After the stall bit is set, software should poll the corresponding DMA0BUSY to verify that there are no more DMA transfers for that channel.

The memory interface configuration SFRs of a channel define the linear region of XRAM involved in the transfer through a 12-bit base address register DMA0NBAH:L, a 10-bit address offset register DMA0NAOH:L and a 10-bit data transfer size DMA0NSZH:L. The effective memory address is the address involved in the current DMA0 transaction.

Effective Memory Address = Base Address + Address Offset

The address offset serves as byte counter. The address offset should be always less than data transfer length. The address offset increments by one after each byte transferred. For DMA0 configuration of any channel, address offsets of active channels should be reset to 0 before DMA0 transfers occur.

14.6.5.1. CTR Data Flow

The AES0 module data flow for CTR encryption and decryption shown in Figure 14.5. The data flow is the same for encryption and decryption. The AES0DCF sfr is always configured to XOR AES0XIN with the AES Core output.The XOR on the input is not used. The AES core is configured for an encryption operation. The encryption key is written to AES0KIN. The key size is set to the desired key size.

For an encryption operation, the plaintext is written to the AES0BIN sfr and the ciphertext is read from AES0YOUT. For decryption, the ciphertext is written to AES0BIN and the plaintext is read from AES0YOUT.

Note the counter must be incremented after each block using software.

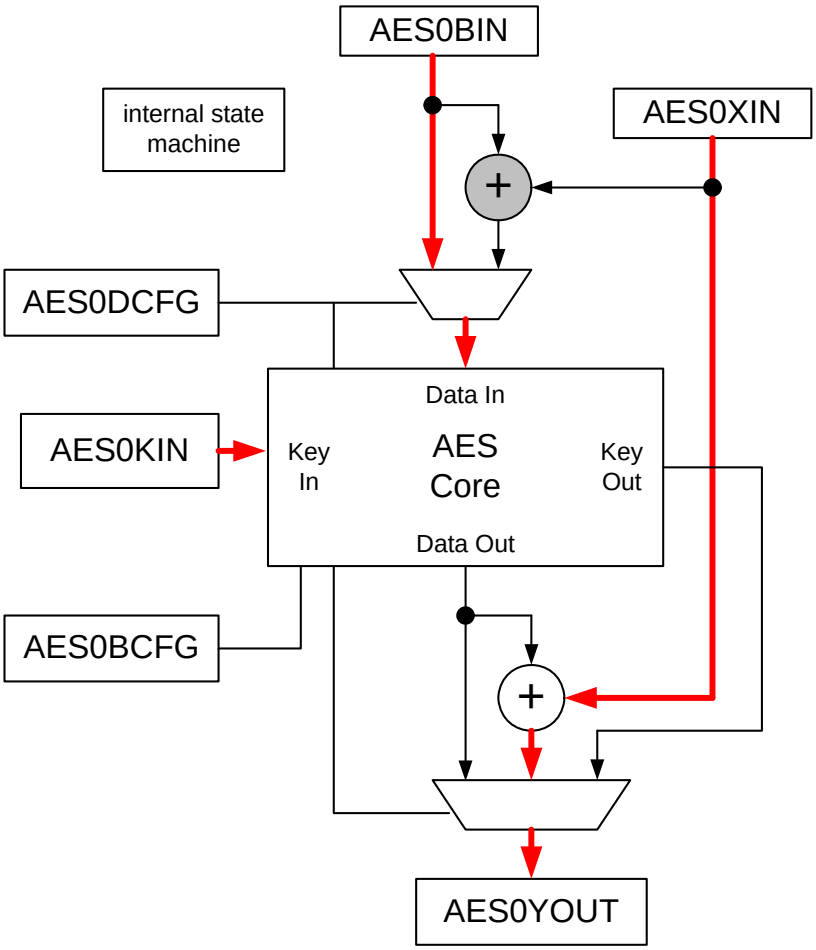


Figure 14.8. Counter Mode Data Flow

- Disable the DMA by writing 0x00 to DMA0EN
- Increment counter and repeat all steps for additional blocks

14.6.6.1. CTR Encryption using SFRs

- First Configure AES Module for CTR Block Cipher Mode Encryption
  - Reset AES module by writing 0x00 to AES0BCFG.
  - Configure the AES Module data flow for XOR on output data by writing 0x02 to the AES0DCFG sfr.
  - Write key size to bits 1 and 0 of the AES0BCFG.
  - Configure the AES core for encryption by setting bit 2 of AES0BCFG.
  - Enable the AES core by setting bit 3 of AES0BCFG.
- Repeat alternating write sequence 16 times
  - Write plaintext byte to AES0BIN.
  - Write counter byte to AES0XIN
  - Write encryption key byte to AES0KIN.
- Write remaining encryption key bytes to AES0KIN for 192-bit and 256-bit decryption only.
- Wait on AES done interrupt or poll bit 5 of AES0BCFG.
- Read 16 encrypted bytes from the AES0YOUT sfr.

If encrypting multiple blocks, increment the counter and repeat this process. It is not necessary reconfigure the AES module for each block.

15.7. Using the ENC0 module with the DMA

The steps for Encoding/Decoding using the DMA are as follows.

1. Clear the ENC module by writing 0x00 to the ENC0CN SFR.
2. Configure the first DMA channel for the XRAM-to-ENC0 input transfer:
   a. Disable the first DMA channel by clearing the corresponding bit in DMA0EN.
   b. Select the first DMA channel by writing to DMA0SEL.
   c. Configure the selected DMA channel to use the XRAM-to-ENC0 input peripheral request by writing 0x00 to DMA0NCF.
   d. Set the ENDIAN bit in DMA0NCF to enable big-endian multi-byte DMA transfers.
   e. Write 0 to DMA0NMD to disable wrapping.
   f. Write the address of the first byte of input data DMA0NBAH:L.
   g. Write the size of the input data transfer in bytes to DMA0NSZH:L.
   h. Clear the address offset SFRs DMA0A0H:L.
3. Configure the second DMA channel for the ENC0-to-XRAM output transfer:
   a. Disable the second DMA channel by clearing the corresponding bit in DMA0EN.
   b. Select the second DMA channel by writing to DMA0SEL.
   c. Configure the selected DMA channel to use the SPI1DAT-to-XRAM output peripheral request by writing 0x01 to DMA0NCF.
   d. Set the ENDIAN bit in DMA0NCF to enable big-endian multi-byte DMA transfers.
   e. Enable DMA interrupts for the second channel by setting bit 7 of DMA0NCF.
   f. Write 0 to DMA0NMD to disable wrapping.
   g. Write the address for the first byte of the output data to DMA0NBAH:L.
   h. Write the size of the output data transfer in bytes to DMA0NSZH:L.
   i. Clear the address offset SFRs DMA0A0H:L.
   j. Enable the interrupt on the second channel by setting the corresponding bit in DMA0INT.
4. Clear the interrupt bits in DMA0INT for both channels.
5. Enable DMA interrupts by setting bit 5 of EIE2.
6. If desired for a decode operation, enable the ERROR interrupt bit by setting bit 6 of EIE2.
7. Write the operation value to ENC0CN setting ENC, DEC, and MODE bits for the desired operation. The DMA bit and ENDIAN bits must be set. The READY bits and ERROR bits must be cleared.
   a. Write 0x16 for Manchester Decode operation.
   b. Write 0x17 for Three-out-of-Six Decode operation.
   c. Write 0x26 for Manchester Encode operation.
   d. Write 0x27 for Three-out-of-Six Encode operation.
8. Wait on the DMA interrupt.
9. Clear the DMA enables in the DMA0EN SFR.
10. Clear the DMA interrupts in the DMA0INT SFR.
11. For a decode operation only, check the ERROR bit in ENC0CN for a decode error.

Note that the encoder and all DMA channels should be configured for Big-Endian mode.

SFR Definition 15.1. ENC0CN: Encoder Decoder 0 Control

Bit	7	6	5	4	3	2	1	0
Name	READY	ERROR	ENC	DEC		DMA	ENDIAN	MODE
Type	R	R	R/W	R/W	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC5; SFR page = 0x2; Not bit-Addressable

Bit	Name	Function
7	READY	**Ready Flag.**
6	ERROR	**Error Flag.**
5	ENC	**Encode.** Setting this bit will initiate an Encode operation.
4	DEC	**Decode.** Setting this bit will initiate a Decode operation.
2	DMA	**DMA Mode Enable.** This bit should be set when using the encoder/decoder with the DMA.
1	ENDIAN	**Big-Endian DMA Mode Select.** This bit should be set when using the DMA with big-endian multiple byte DMA transfers. The DMA must also be configured for the same endian mode.
0	MODE	**Mode.** 0: Select Manchester encoding or decoding. 1:Select Three-out-of-Six encoding or decoding.

SFR Definition 18.7. FRBCN: Flash Read Buffer Control

Bit	7	6	5	4	3	2	1	0
Name							FRBD	CHBLKW
Type	R	R	R	R	R	R	R/W	R/W
Reset	0	0	1	0	0	0	0	0

SFR Page = 0xF; SFR Address = 0xB5

Bit	Name	Function
7:2	Unused	Read = 000000b. Write = don't care.
1	FRBD	**Flash Read Buffer Disable Bit.** 0: Flash read buffer is enabled and being used. 1: Flash read buffer is disabled and bypassed.
0	CHBLKW	**Block Write Enable Bit.** This bit allows block writes to flash memory from firmware. 0: Each byte of a software flash write is written individually. 1: Flash bytes are written in groups of four.

SFR Definition 19.6. PMU0MD: Power Management Unit Mode

Bit	7	6	5	4	3	2	1	0
Name	RTCOE	WAKEOE	MONDIS					
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xB3

Bit	Name	Function
7	RTCOE	**Buffered SmaRTClock Output Enable.** Enables the buffered SmaRTClock oscillator output on P0.2. 0: Buffered SmaRTClock output not enabled. 1: Buffered SmaRTClock output not enabled.
6	WAKEOE	**Wakeup Request Output Enable.** Enables the Sleep Mode wake-up request signal on P0.3. 0: Wake-up request signal is not enabled. 1: Wake-up request signal is enabled.
5	MONDIS	**POR Supply Monitor Disable.** Writing a 1 to this bit disables the POR supply monitor.
4:0	Unused	Read = 00000b. Write = Don't Care.

26.3. LCD Contrast Adjustment

The LCD Bias voltages which determine the LCD contrast are generated using the VBAT supply voltage or the on-chip charge pump. There are four contrast control modes to accomodate a wide variety of applications and supply voltages. The target contrast voltage is programmable in 60 mV steps from 1.9 to 3.72 V. The LCD contrast voltage is controlled by the LCD0CNTRST register and the contrast control mode is selected by setting the appropriate bits in the LCD0MSCN, LCD0MSCF, LCD0PWR, and LCD0VBMCN registers.

Note: An external 10 µF decoupling capacitor is required on the VLCD pin to create a charge reservoir at the output of the charge pump.

Table 26.1. Bit Configurations to select Contrast Control Modes

Mode	LCD0MSCN.2	LCD0MSCF.0	LCD0PWR.3	LCD0VBMCN.7
1	0	1	0	0
2	0	1	1	1
3	1*	0	1	1
4	1*	0	0	1
*** May be set to 0 to support increased load currents.**				

26.3.1. Contrast Control Mode 1 (Bypass Mode)

In Contrast Control Mode 1, the contrast control circuitry is disabled and the VLCD voltage follows the VBAT supply voltage, as shown in Figure 26.3. This mode is useful in systems where the VBAT voltage always remains constant and will provide the lowest LCD power consumption. Bypass Mode is selected using the following procedure:

1. Clear Bit 2 of the LCD0MSCN register to 0b (LCD0MSCN &= ~0x04)
2. Set Bit 0 of the LCD0MSCF register to 1b (LCD0MSCF |= 0x01)
3. Clear Bit 3 of the LCD0PWR register to 0b (LCD0PWR &= ~0x08)
4. Clear Bit 7 of the LCD0VBMCN register to 0b (LCD0VBMCN &= ~0x80)

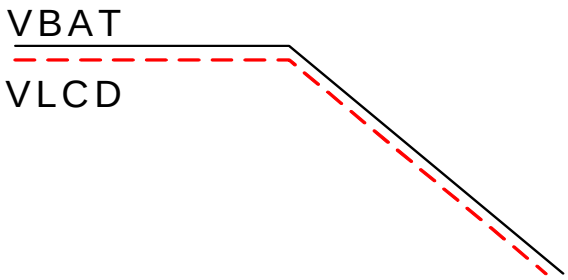


Figure 26.3. Contrast Control Mode 1

27.4. Port Match

Port match functionality allows system events to be triggered by a logic value change on P0 or P1. A software controlled value stored in the PnMAT registers specifies the expected or normal logic values of P0 and P1. A Port mismatch event occurs if the logic levels of the Port's input pins no longer match the software controlled value. This allows Software to be notified if a certain change or pattern occurs on P0 or P1 input pins regardless of the XBRn settings.

The PnMASK registers can be used to individually select which P0 and P1 pins should be compared against the PnMAT registers. A Port mismatch event is generated if (P0 & P0MASK) does not equal (PnMAT & P0MASK) or if (P1 & P1MASK) does not equal (PnMAT & P1MASK).

A Port mismatch event may be used to generate an interrupt or wake the device from a low power mode. See Section "17. Interrupt Handler" on page 232 and Section "19. Power Management" on page 257 for more details on interrupt and wake-up sources.

SFR Definition 27.4. P0MASK: Port0 Mask Register

Bit	7	6	5	4	3	2	1	0
Name	P0MASK[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page= 0x0; SFR Address = 0xC7

Bit	Name	Function
7:0	P0MASK[7:0]	**Port0 Mask Value.** Selects the P0 pins to be compared with the corresponding bits in P0MAT. 0: P0.n pin pad logic value is ignored and cannot cause a Port Mismatch event. 1: P0.n pin pad logic value is compared to P0MAT.n.

SFR Definition 27.5. P0MAT: Port0 Match Register

Bit	7	6	5	4	3	2	1	0
Name	P0MAT[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Page= 0x0; SFR Address = 0xD7

Bit	Name	Function
7:0	P0MAT[7:0]	**Port 0 Match Value.** Match comparison value used on Port 0 for bits in P0MASK which are set to 1. 0: P0.n pin logic value is compared with logic LOW. 1: P0.n pin logic value is compared with logic HIGH.

SFR Definition 27.14. P1SKIP: Port1 Skip

Bit	7	6	5	4	3	2	1	0
Name	P1SKIP[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xD5

Bit	Name	Function
7:0	P1SKIP[7:0]	**Port 1 Crossbar Skip Enable Bits.** These bits select Port 1 pins to be skipped by the Crossbar Decoder. Port pins used for analog, special functions or GPIO should be skipped by the Crossbar. 0: Corresponding P1.n pin is not skipped by the Crossbar. 1: Corresponding P1.n pin is skipped by the Crossbar.

SFR Definition 27.15. P1MDIN: Port1 Input Mode

Bit	7	6	5	4	3	2	1	0
Name	P1MDIN[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Page = 0x0; SFR Address = 0xF2

Bit	Name	Function
7:0	P1MDIN[7:0]	**Analog Configuration Bits for P1.7–P1.0 (respectively).** Port pins configured for analog mode have their weak pullup and digital receiver disabled. The digital driver is not explicitly disabled. 0: Corresponding P1.n pin is configured for analog mode. 1: Corresponding P1.n pin is not configured for analog mode.

Table 28.5. SMBus Status Decoding With Hardware ACK Generation Disabled (EHACK = 0)

Mode	Values Read				Current SMbus State	Typical Response Options	Values to Write			Next Status Vector Expected
	Status Vector	ACKRQ	ARBLOST	ACK			STA	STO	ACK	
Slave Transmitter	0100	0	0	0	A slave byte was transmitted; NACK received.	No action required (expecting STOP condition).	0	0	X	0001
		0	0	1	A slave byte was transmitted; ACK received.	Load SMB0DAT with next data byte to transmit.	0	0	X	0100
		0	1	X	A Slave byte was transmitted; error detected.	No action required (expecting Master to end transfer).	0	0	X	0001
	0101	0	X	X	An illegal STOP or bus error was detected while a Slave Transmission was in progress.	Clear STO.	0	0	X	-
Slave Receiver	0010	1	0	X	A slave address + R/W was received; ACK requested.	If Write, Acknowledge received address	0	0	1	0000
						If Read, Load SMB0DAT with data byte; ACK received address	0	0	1	0100
						NACK received address.	0	0	0	-
		1	1	X	Lost arbitration as master; slave address + R/W received; ACK requested.	If Write, Acknowledge received address	0	0	1	0000
						If Read, Load SMB0DAT with data byte; ACK received address	0	0	1	0100
						NACK received address.	0	0	0	-
						Reschedule failed transfer; NACK received address.	1	0	0	1110
	0001	0	0	X	A STOP was detected while addressed as a Slave Transmitter or Slave Receiver.	Clear STO.	0	0	X	-
		1	1	X	Lost arbitration while attempting a STOP.	No action required (transfer complete/aborted).	0	0	0	-
	0000	1	0	X	A slave byte was received; ACK requested.	Acknowledge received byte; Read SMB0DAT.	0	0	1	0000
						NACK received byte.	0	0	0	-
Bus Error Condition	0010	0	1	X	Lost arbitration while attempting a repeated START.	Abort failed transfer.	0	0	X	-
						Reschedule failed transfer.	1	0	X	1110
	0001	0	1	X	Lost arbitration due to a detected STOP.	Abort failed transfer.	0	0	X	-
						Reschedule failed transfer.	1	0	X	1110
	0000	1	1	X	Lost arbitration while transmitting a data byte as master.	Abort failed transfer.	0	0	0	-
						Reschedule failed transfer.	1	0	0	1110

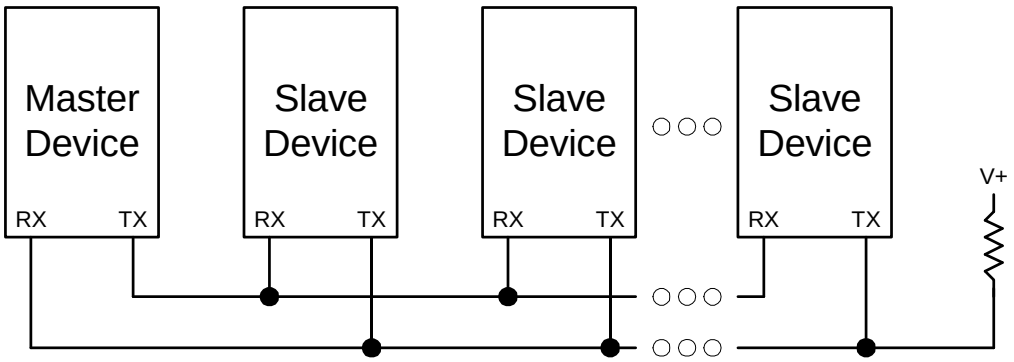


Figure 29.6. UART Multi-Processor Mode Interconnect Diagram

Table 30.1. SPI Slave Timing Parameters

Parameter	Description	Min	Max	Units
Master Mode Timing (See Figure 30.8 and Figure 30.9)				
T_{MCKH}	SCK High Time	1 x T_{SYSCLK}	—	ns
T_{MCKL}	SCK Low Time	1 x T_{SYSCLK}	—	ns
T_{MIS}	MISO Valid to SCK Shift Edge	1 x T_{SYSCLK} + 20	—	ns
T_{MIH}	SCK Shift Edge to MISO Change	0	—	ns
Slave Mode Timing (See Figure 30.10 and Figure 30.11)				
T_{SE}	NSS Falling to First SCK Edge	2 x T_{SYSCLK}	—	ns
T_{SD}	Last SCK Edge to NSS Rising	2 x T_{SYSCLK}	—	ns
T_{SEZ}	NSS Falling to MISO Valid	—	4 x T_{SYSCLK}	ns
T_{SDZ}	NSS Rising to MISO High-Z	—	4 x T_{SYSCLK}	ns
T_{CKH}	SCK High Time	5 x T_{SYSCLK}	—	ns
T_{CKL}	SCK Low Time	5 x T_{SYSCLK}	—	ns
T_{SIS}	MOSI Valid to SCK Sample Edge	2 x T_{SYSCLK}	—	ns
T_{SIH}	SCK Sample Edge to MOSI Change	2 x T_{SYSCLK}	—	ns
T_{SOH}	SCK Shift Edge to MISO Change	—	4 x T_{SYSCLK}	ns
T_{SLH}	Last SCK Edge to MISO Change (CKPHA = 1 ONLY)	6 x T_{SYSCLK}	8 x T_{SYSCLK}	ns
Note: T_{SYSCLK} is equal to one period of the device system clock (SYSCLK).				

31.1. Signal Descriptions

The four signals used by SPI1 (MOSI, MISO, SCK, NSS) are described below.

31.1.1. Master Out, Slave In (MOSI)

The master-out, slave-in (MOSI) signal is an output from a master device and an input to slave devices. It is used to serially transfer data from the master to the slave. This signal is an output when SPI1 is operating as a master and an input when SPI1 is operating as a slave. Data is transferred most-significant bit first. When configured as a master, MOSI is driven by the MSB of the shift register in both 3- and 4-wire mode.

31.1.2. Master In, Slave Out (MISO)

The master-in, slave-out (MISO) signal is an output from a slave device and an input to the master device. It is used to serially transfer data from the slave to the master. This signal is an input when SPI1 is operating as a master and an output when SPI1 is operating as a slave. Data is transferred most-significant bit first. The MISO pin is placed in a high-impedance state when the SPI module is disabled and when the SPI operates in 4-wire mode as a slave that is not selected. When acting as a slave in 3-wire mode, MISO is always driven by the MSB of the shift register.

31.1.3. Serial Clock (SCK)

The serial clock (SCK) signal is an output from the master device and an input to slave devices. It is used to synchronize the transfer of data between the master and slave on the MOSI and MISO lines. SPI1 generates this signal when operating as a master. The SCK signal is ignored by a SPI slave when the slave is not selected (NSS = 1) in 4-wire slave mode.

31.1.4. Slave Select (NSS)

The function of the slave-select (NSS) signal is dependent on the setting of the NSSMD1 and NSSMD0 bits in the SPI1CN register. There are three possible modes that can be selected with these bits:

1. NSSMD[1:0] = 00: 3-Wire Master or 3-Wire Slave Mode: SPI1 operates in 3-wire mode, and NSS is disabled. When operating as a slave device, SPI1 is always selected in 3-wire mode. Since no select signal is present, SPI1 must be the only slave on the bus in 3-wire mode. This is intended for point-to-point communication between a master and one slave.
2. NSSMD[1:0] = 01: 4-Wire Slave or Multi-Master Mode: SPI1 operates in 4-wire mode, and NSS is enabled as an input. When operating as a slave, NSS selects the SPI1 device. When operating as a master, a 1-to-0 transition of the NSS signal disables the master function of SPI1 so that multiple master devices can be used on the same SPI bus.
3. NSSMD[1:0] = 1x: 4-Wire Master Mode: SPI1 operates in 4-wire mode, and NSS is enabled as an output. The setting of NSSMD0 determines what logic level the NSS pin will output. This configuration should only be used when operating SPI1 as a master device.

See Figure 31.2, Figure 31.3, and Figure 31.4 for typical connection diagrams of the various operational modes. **Note that the setting of NSSMD bits affects the pinout of the device.** When in 3-wire master or 3-wire slave mode, the NSS pin will not be mapped by the crossbar. In all other modes, the NSS signal will be mapped to a pin on the device. See Section “27. Port Input/Output” on page 351 for general purpose port I/O and crossbar information.

Document Change List

Revision 0.1 to Revision 0.2

- Added new content to DC0 chapter.
- Reordered chapters.
- Corrections to SFR tables.
- Updated Electrical Specifications.

Revision 0.2 to Revision 0.3

- Added new content to DMA0, CRC1, ENC0, SPI1, and Pulse Counter chapters.
- Added TQFP-80 package variant.
- Added package drawings and landing diagram for TQFP-80 package.
- Added via placement recommendations for DQFN-76 package.
- Updated electrical specifications.
- Corrections to SFR tables.
- Fixed inconsistencies in SFR names.
- Fixed inconsistencies in acronyms and terminology.

Revision 0.3 to Revision 0.5

- Updated maximum IBAT current using precision oscillator in Table 4.4.
- Updated sleep currents in Table 4.4.
- Added Note 1 to Table 4.6.
- Deleted SFR Page Stack Example in Special Function Registers chapter.
- Change description of SFRPGEN bit in SFRPGCN SFR definition.
- Added paragraph to Flash chapter to explain lock byte behavior on 128 kB devices.
- Corrected SFRPAGE in SPI1 SFR definitions 32.1/2/3.

Revision 0.5 to Revision 1.0

- Changed revision in ordering information from A to B.
- Fixed inconsistencies in VIORF pin definitions.
- Added note about IFBANK usage.
- Updated Table 4.4 Digital Supply Current—Sleep Mode (LCD disabled, RTC disabled) 3.6 V, 25 °C maximum to 0.23 µA.
- Fixed inconsistencies in description of reset behavior.
- Added encryption/decryption times to SFR Definition 14.1.
- Fixed inconsistencies in SFR Definition 14.2.
- Fixed inconsistencies in Port P2 through P7 SFR Definitions.
- All TBD specifications have been determined.