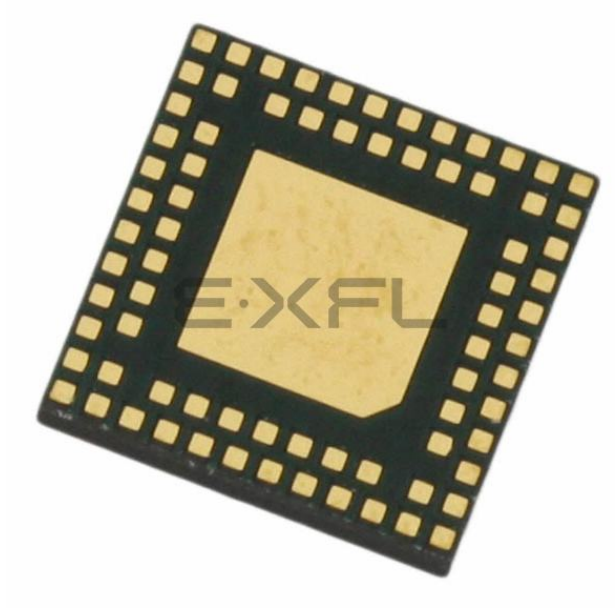
Silicon Labs - C8051F960-B-GMR Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, LCD, POR, PWM, WDT
Number of I/O	57
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	76-VFQFN Dual Rows, Exposed Pad
Supplier Device Package	76-DQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f960-b-gmr

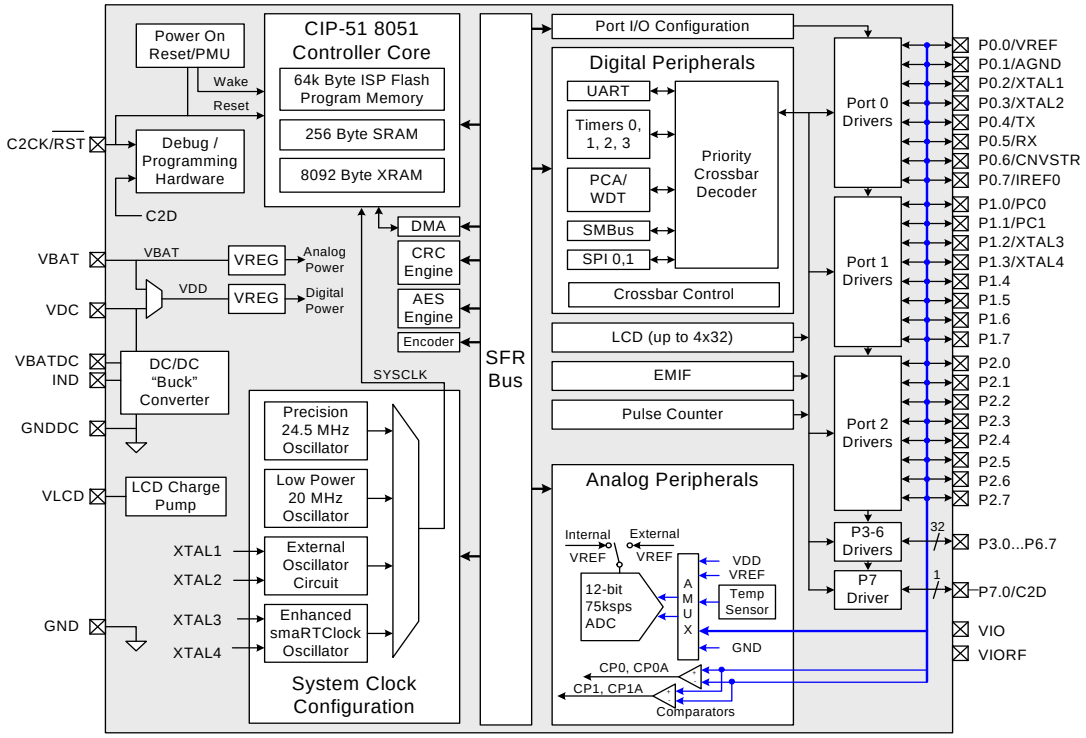


Figure 1.5. C8051F964 Block Diagram

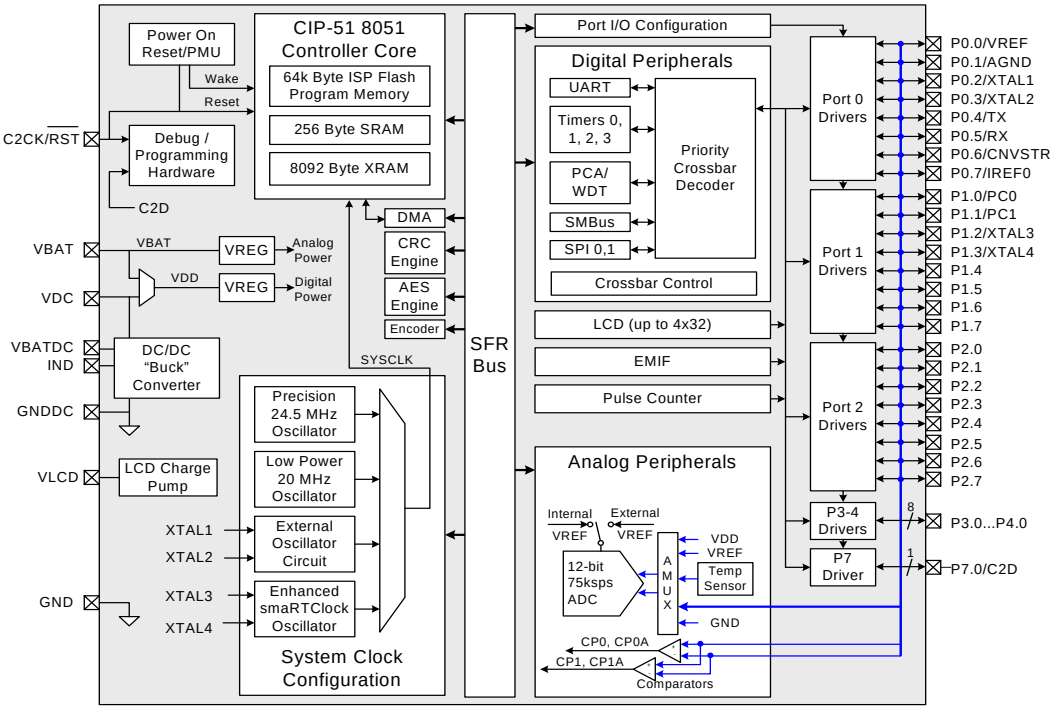


Figure 1.6. C8051F965 Block Diagram

SFR Definition 10.1. EMI0CN: External Memory Interface Control

Bit	7	6	5	4	3	2	1	0
Name	PGSEL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xAA

Bit	Name	Function
7:0	PGSEL[7:0]	**XRAM Page Select Bits.** The XRAM Page Select Bits provide the high byte of the 16-bit external data memory address when using an 8-bit MOVX command, effectively selecting a 256-byte page of RAM. 0x00: 0x0000 to 0x00FF 0x01: 0x0100 to 0x01FF ... 0xFE: 0xFE00 to 0xFEFF 0xFF: 0xFF00 to 0xFFFF

SFR Definition 10.3. EMI0TC: External Memory Timing Control

Bit	7	6	5	4	3	2	1	0
Name	EAS[1:0]		EWR[3:0]				EAH[1:0]	
Type	R/W		R/W				R/W	
Reset	1	1	1	1	1	1	1	1

SFR Page = 0x0; SFR Address = 0xAF

Bit	Name	Function
7:6	EAS[1:0]	**EMIF Address Setup Time Bits.** 00: Address setup time = 0 SYSCLK cycles. 01: Address setup time = 1 SYSCLK cycle. 10: Address setup time = 2 SYSCLK cycles. 11: Address setup time = 3 SYSCLK cycles.
5:2	EWR[3:0]	**EMIF $\overline{WR}$ and $\overline{RD}$ Pulse-Width Control Bits.** 0000: $\overline{WR}$ and $\overline{RD}$ pulse width = 1 SYSCLK cycle. 0001: $\overline{WR}$ and $\overline{RD}$ pulse width = 2 SYSCLK cycles. 0010: $\overline{WR}$ and $\overline{RD}$ pulse width = 3 SYSCLK cycles. 0011: $\overline{WR}$ and $\overline{RD}$ pulse width = 4 SYSCLK cycles. 0100: $\overline{WR}$ and $\overline{RD}$ pulse width = 5 SYSCLK cycles. 0101: $\overline{WR}$ and $\overline{RD}$ pulse width = 6 SYSCLK cycles. 0110: $\overline{WR}$ and $\overline{RD}$ pulse width = 7 SYSCLK cycles. 0111: $\overline{WR}$ and $\overline{RD}$ pulse width = 8 SYSCLK cycles. 1000: $\overline{WR}$ and $\overline{RD}$ pulse width = 9 SYSCLK cycles. 1001: $\overline{WR}$ and $\overline{RD}$ pulse width = 10 SYSCLK cycles. 1010: $\overline{WR}$ and $\overline{RD}$ pulse width = 11 SYSCLK cycles. 1011: $\overline{WR}$ and $\overline{RD}$ pulse width = 12 SYSCLK cycles. 1100: $\overline{WR}$ and $\overline{RD}$ pulse width = 13 SYSCLK cycles. 1101: $\overline{WR}$ and $\overline{RD}$ pulse width = 14 SYSCLK cycles. 1110: $\overline{WR}$ and $\overline{RD}$ pulse width = 15 SYSCLK cycles. 1111: $\overline{WR}$ and $\overline{RD}$ pulse width = 16 SYSCLK cycles.
1:0	EAH[1:0]	**EMIF Address Hold Time Bits.** 00: Address hold time = 0 SYSCLK cycles. 01: Address hold time = 1 SYSCLK cycle. 10: Address hold time = 2 SYSCLK cycles. 11: Address hold time = 3 SYSCLK cycles.

of an inadvertent write to the PCON register. If this behavior is not desired, the WDT may be disabled by software prior to entering the idle mode if the WDT was initially configured to allow this operation. This provides the opportunity for additional power savings, allowing the system to remain in the Idle mode indefinitely, waiting for an external stimulus to wake up the system. Refer to Section “22.6. PCA Watchdog Timer Reset” on page 283 for more information on the use and configuration of the WDT.

19.3. Stop Mode

Setting the Stop Mode Select bit (PCON.1) causes the CIP-51 to enter Stop mode as soon as the instruction that sets the bit completes execution. In Stop mode the precision internal oscillator and CPU are stopped; the state of the low power oscillator and the external oscillator circuit is not affected. Each analog peripheral (including the external oscillator circuit) may be shut down individually prior to entering Stop Mode. Stop mode can only be terminated by an internal or external reset. On reset, the CIP-51 performs the normal reset sequence and begins program execution at address 0x0000.

If enabled, the Missing Clock Detector will cause an internal reset and thereby terminate the Stop mode. The Missing Clock Detector should be disabled if the CPU is to be put to in STOP mode for longer than the MCD timeout.

Stop Mode is a legacy 8051 power mode; it will not result in optimal power savings. Sleep, Suspend, or Low Power Idle mode will provide more power savings if the MCU needs to be inactive for a long period of time.

19.4. Low Power Idle Mode

Low Power Idle Mode uses clock gating to reduce the supply current when the device is placed in Idle mode. This mode is enabled by configuring the clock tree gates using the PCLKEN register, setting the LPMEN bit in the CLKMODE register, and placing the device in Idle mode. The clock is automatically gated from the CPU upon entry into Idle mode when the LPMEN bit is set. This mode provides substantial power savings over the standard Idle Mode especially at high system clock frequencies.

The clock gating logic may also be used to reduce power when executing code. Low Power Active Mode is enabled by configuring the PCLKACT and PCLKEN registers, then setting the LPMEN bit. The PCLKACT register provides the ability to override the PCLKEN setting to force a clock to certain peripherals in Low Power Active mode. If the PCLKACT register is left at its default value, then PCLKEN determines which perpherals will be clocked in this mode. The CPU is always clocked in Low Power Active Mode.

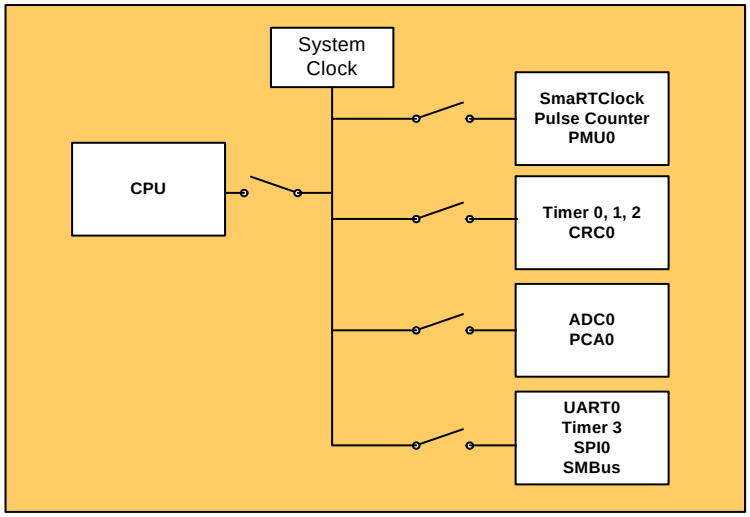


Figure 19.2. Clock Tree Distribution

23.1. Programmable Precision Internal Oscillator

All C8051F96x devices include a programmable precision internal oscillator that may be selected as the system clock. OSCICL is factory calibrated to obtain a 24.5 MHz frequency. See Section “4. Electrical Characteristics” on page 56 for complete oscillator specifications.

The precision oscillator supports a spread spectrum mode which modulates the output frequency in order to reduce the EMI generated by the system. When enabled (SSE = 1), the oscillator output frequency is modulated by a stepped triangle wave whose frequency is equal to the oscillator frequency divided by 384 (63.8 kHz using the factory calibration). The deviation from the nominal oscillator frequency is +0%, –1.6%, and the step size is typically 0.26% of the nominal frequency. When using this mode, the typical average oscillator frequency is lowered from 24.5 MHz to 24.3 MHz.

23.2. Low Power Internal Oscillator

All C8051F96x devices include a low power internal oscillator that defaults as the system clock after a system reset. The low power internal oscillator frequency is 20 MHz ± 10% and is automatically enabled when selected as the system clock and disabled when not in use. See Section “4. Electrical Characteristics” on page 56 for complete oscillator specifications.

23.3. External Oscillator Drive Circuit

All C8051F96x devices include an external oscillator circuit that may drive an external crystal, ceramic resonator, capacitor, or RC network. A CMOS clock may also provide a clock input. Figure 23.1 shows a block diagram of the four external oscillator options. The external oscillator is enabled and configured using the OSCXCN register.

The external oscillator output may be selected as the system clock or used to clock some of the digital peripherals (e.g., Timers, PCA, etc.). See the data sheet chapters for each digital peripheral for details. See Section “4. Electrical Characteristics” on page 56 for complete oscillator specifications.

23.3.1. External Crystal Mode

If a crystal or ceramic resonator is used as the external oscillator, the crystal/resonator and a 10 MΩ resistor must be wired across the XTAL1 and XTAL2 pins as shown in Figure 23.1, Option 1. Appropriate loading capacitors should be added to XTAL1 and XTAL2, and both pins should be configured for analog I/O with the digital output drivers disabled.

Figure 23.2 shows the external oscillator circuit for a 20 MHz quartz crystal with a manufacturer recommended load capacitance of 12.5 pF. Loading capacitors are "in series" as seen by the crystal and "in parallel" with the stray capacitance of the XTAL1 and XTAL2 pins. The total value of the each loading capacitor and the stray capacitance of each XTAL pin should equal 12.5 pF x 2 = 25 pF. With a stray capacitance of 10 pF per pin, the 15 pF capacitors yield an equivalent series capacitance of 12.5 pF across the crystal.

Note: The recommended load capacitance depends upon the crystal and the manufacturer. Please refer to the crystal data sheet when completing these calculations.

24.2.6. Missing SmaRTClock Detector

The missing SmaRTClock detector is a one-shot circuit enabled by setting MCLKEN (RTC0CN.6) to 1. When the SmaRTClock Missing Clock Detector is enabled, OSCFAIL (RTC0CN.5) is set by hardware if SmaRTClock oscillator remains high or low for more than 100 µs.

A SmaRTClock Missing Clock detector timeout can trigger an interrupt, wake the device from a low power mode, or reset the device. See Section “17. Interrupt Handler” on page 232, Section “19. Power Management” on page 257, and Section “22. Reset Sources” on page 278 for more information.

Note: The SmaRTClock Missing Clock Detector should be disabled when making changes to the oscillator settings in RTC0XCN.

24.2.7. SmaRTClock Oscillator Crystal Valid Detector

The SmaRTClock oscillator crystal valid detector is an oscillation amplitude detector circuit used during crystal startup to determine when oscillation has started and is nearly stable. The output of this detector can be read from the CLKVLD bit (RTX0XCN.4).

Notes:

1. The CLKVLD bit has a blanking interval of 2 ms. During the first 2 ms after turning on the crystal oscillator, the output of CLKVLD is not valid.
2. This SmaRTClock crystal valid detector (CLKVLD) is not intended for detecting an oscillator failure. The missing SmaRTClock detector (CLKFAIL) should be used for this purpose.
3. The CLKVLD bit output is driven low when BIASX2 is disabled.

24.3. SmaRTClock Timer and Alarm Function

The SmaRTClock timer is a 32-bit counter that, when running (RTC0TR = 1), is incremented every SmaRTClock oscillator cycle. The timer has an alarm function that can be set to generate an interrupt, wake the device from a low power mode, or reset the device at a specific time. See Section “17. Interrupt Handler” on page 232, Section “19. Power Management” on page 257, and Section “22. Reset Sources” on page 278 for more information.

The SmaRTClock timer includes an Auto Reset feature, which automatically resets the timer to zero one SmaRTClock cycle after the alarm 0 signal is deasserted. When using Auto Reset, the Alarm match value should always be set to 2 counts less than the desired match value. When using the LFO in combination with Auto Reset, the right-justified Alarm match value should be set to 4 counts less than the desired match value. Auto Reset can be enabled by writing a 1 to ALRM (RTC0CN.2).

24.3.1. Setting and Reading the SmaRTClock Timer Value

The 32-bit SmaRTClock timer can be set or read using the six CAPTUREn internal registers. Note that the timer does not need to be stopped before reading or setting its value. The following steps can be used to set the timer value:

1. Write the desired 32-bit set value to the CAPTUREn registers.
2. Write 1 to RTC0SET. This will transfer the contents of the CAPTUREn registers to the SmaRTClock timer.
3. Operation is complete when RTC0SET is cleared to 0 by hardware.

The following steps can be used to read the current timer value:

1. Write 1 to RTC0CAP. This will transfer the contents of the timer to the CAPTUREn registers.
2. Poll RTC0CAP until it is cleared to 0 by hardware.
3. A snapshot of the timer value can be read from the CAPTUREn registers

Notes:

1. If the system clock is faster than 4x the SmaRTClock, then the HSMODE bit should be set to allow the set and capture operations to be concluded quickly (system clock used for transfers).
2. If the system clock is slower than 4x the SmaRTClock, then HSMODE should be set to zero, and RTC must be

SFR Definition 25.6. PC0DCL: PC0 Debounce Configuration Low

Bit	7	6	5	4	3	2	1	0
Name	PC0DCL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	1	0	0

SFR Address = 0xF9; SFR Page = 0x2

Bit	Name	Function
7:0	PC0DCL[7:0]	**Pulse Counter Debounce Low** Number of cumulative good samples seen by the integrator before recognizing the input as low. Setting PC0DCL to 0x00 will disable integrators on both PC0 and PC1. The actual value used is PC0DCL plus one. Sampling a low decrements while sampling a high increments the count. Switch bounce produces a random looking signal. The worst case would be to bounce high at each sample point and not start decrementing the integrator until the switch bounce settled. Therefore, minimum pulse width should account for twice the debounce time. For example, using a sample rate of 1 ms and a PC0DCL value of 0x09 will look for 10 cumulative lows before recognizing the input as low (1 ms x 10 = 10 ms). The minimum pulse width should be 20 ms or greater for this example. If PC0DCL has a value of 0x03 and the sample rate is 500 µs, the integrator would need to see 4 cumulative lows before recognizing the low (500 µs x 4 = 2 ms). The minimum pulse width should be 4 ms for this example.

SFR Definition 25.20. PC0INT0: PC0 Interrupt 0

Bit	7	6	5	4	3	2	1	0
Name	CMP1F	CMP1EN	CMP0F	CMP0EN	OVRF	OVREN	DIRCHGF	DIRCHGEN
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xFB; SFR Page = 0x2

Bit	Name	Function
7	CMP1F	**Comparator 1 Flag** 0: Counter 1 did not match comparator 1 value. 1: Counter 1 matched comparator 1 value.
6	CMP1EN	**Comparator 1 Interrupt/Wake-up Source Enable** 0:CMP1F not enabled as interrupt or wake-up source. 1:CMP1F enabled as interrupt or wake-up source.
5	CMP0F	**Comparator 0 Flag** 0: Counter 0 did not match comparator 0 value. 1: Counter 0 matched comparator 0 value.
4	CMP0EN	**Comparator 0 Interrupt/Wake-up Source Enable** 0:CMP0F not enabled as interrupt or wake-up source. 1:CMP0F enabled as interrupt or wake-up source.
3	OVRF	**Counter Overflow Flag** 1:Neither of the counters has overflowed. 1:One of the counters has overflowed.
2	OVREN	**Counter Overflow Interrupt/Wake-up Source Enable** 0:OVRF not enabled as interrupt or wake-up source. 1:OVRF enabled as interrupt or wake-up source.
1	DIRCHGF	**Direction Change Flag** Direction changed for quadrature mode only. 0:No change in direction detected. 1:Direction Change detected.
0	DIRCHGEN	**Direction Change Interrupt/Wake-up Source Enable** 0:DIRCHGF not enabled as interrupt or wake-up source. 1:DIRCHGF enabled as interrupt or wake-up source.

LCD0CF Register.

8. Set the LCD contrast using the LCD0CNTRST register.
9. Set the desired threshold for the VBAT Supply Monitor.
10. Set the LCD refresh rate using the LCD0DIVH:LCD0DIVL registers.
11. Write a pattern to the LCD0Dn registers.
12. Enable the LCD by setting bit 0 of LCD0MSCN to logic 1 (LCD0MSCN |= 0x01).

26.2. Mapping Data Registers to LCD Pins

The LCD0 data registers are organized as 16 byte-wide special function registers (LCD0Dn), each half-byte or nibble in these registers controls 1 LCD output pin. There are 32 nibbbles used to control the 32 segment pins.

Each LCD0 segment pin can control 1, 2, 3, or 4 LCD segments depending on the selected mux mode. The least significant bit of each nibble controls the segment connected to the backplane signal COM0. The next to least significant bit controls the segment associated with COM1, the next bit controls the segment associated with COM2, and the most significant bit in the 4-bit nibble controls the segment associated with COM3.

In static mode, only the least significant bit in each nibble is used and the three remaining bits in each nibble are ignored. In 2-mux mode, only the two least significant bits are used; in 3-mux mode, only the three least significant bits are used, and in 4-mux mode, each of the 4 bits in the nibble controls one LCD segment. Bits with a value of 1 turn on the associated segment and bits with a value of 0 turn off the associated segment.

SFR Definition 26.1. LCD0Dn: LCD0 Data

Bit	7	6	5	4	3	2	1	0
Name	LCD0Dn							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page: 0x2

Addresses: LCD0D0 = 0x89, LCD0D1 = 0x8A, LCD0D2 = 0x8B, LCD0D3 = 0x8C,
LCD0D4 = 0x8D, LCD0D5 = 0x8E, LCD0D6 = 0x91, LCD0D7 = 0x92,
LCD0D8 = 0x93, LCD0D9 = 0x94, LCD0DA = 0x95, LCD0DB = 0x96,
LCD0DC = 0x97, LCD0DD = 0x99, LCD0DE = 0x9A, LCD0DF = 0x9B.

Bit	Name	Function
7:0	LCD0Dn	**LCD Data.** Each nibble controls one LCD pin. See “Mapping Data Registers to LCD Pins” on page 335 for additional information.

SFR Definition 26.4. LCD0MSCN: LCD0 Master Control

Bit	7	6	5	4	3	2	1	0
Name		BIASEN	DCBIASOE	CLKOE		LOWDRV	LCDRST	LCDEN
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	0	0	0	0	0

SFR Page = 0x2; SFR Address = 0xAB

Bit	Name	Function
7	Reserved	Read = 0b. Must write 0b.
6	BIASEN	**LCD0 Bias Enable.** LCD0 bias may be disabled when using a static LCD (single backplane), contrast control mode 1 (Bypass Mode) is selected, and the VLCD/VIO Supply Comparator is disabled (LCD0CF.5 = 1). It is required for all other modes. 0: LCD0 Bias is disabled. 1: LCD0 Bias is enabled
5	DCBIASOE	**DCDC Converter Bias Output Enable. (Note 1)** 0: The bias for the DCDC converter is gated off. 1: LCD0 provides the bias for the DCDC converter.
4	CLKOE	**LCD Clock Output Enable.** 0: The clock signal to the LCD0 module is gated off. 1: The SmaRTClock provides the undivided clock to the LCD0 Module.
3	Reserved	Read = 0b. Must write 0b.
2	LOWDRV	**Charge Pump Reduced Drive Mode.** This bit should be set to 1 in Contrast Control Mode 3 and Mode 4 for minimum power consumption. This bit may be set to 0 in these modes to support higher load current requirements. 0: The charge pump operates at full power. 1: The charge pump operates at reduced power.
1	LCDRST	**LCD0 Reset.** Writing a 1 to this bit will clear all the LCD0Dn registers to 0x00. This bit must be cleared by software.
0	LCDEN	**LCD0 Enable.** 0: LCD0 is disabled. 1: LCD0 is enabled.
Note 1: To same bias generator is shared by the DCDC Converter and LCD0.		

27. Port Input/Output

Digital and analog resources are available through 57 I/O pins (C8051F960/2/4/6/8) or 34 I/O pins (C8051F961/3/5/7/9). Port pins are organized as eight byte-wide ports. Port pins can be defined as digital or analog I/O. Digital I/O pins can be assigned to one of the internal digital resources or used as general purpose I/O (GPIO). Analog I/O pins are used by the internal analog resources. P7.0 can be used as GPIO and is shared with the C2 Interface Data signal (C2D). See Section “34. C2 Interface” on page 486 for more details.

The designer has complete control over which digital and analog functions are assigned to individual port pins. This resource assignment flexibility is achieved through the use of a Priority Crossbar Decoder. See Section 27.3 for more information on the Crossbar.

For Port I/Os configured as push-pull outputs, current is sourced from the VIO or VIORF supply pin. On 40-pin devices, the VIO and VIORF supply pins are internally tied to VBAT. See Section 27.1 for more information on Port I/O operating modes and the electrical specifications chapter for detailed electrical specifications.

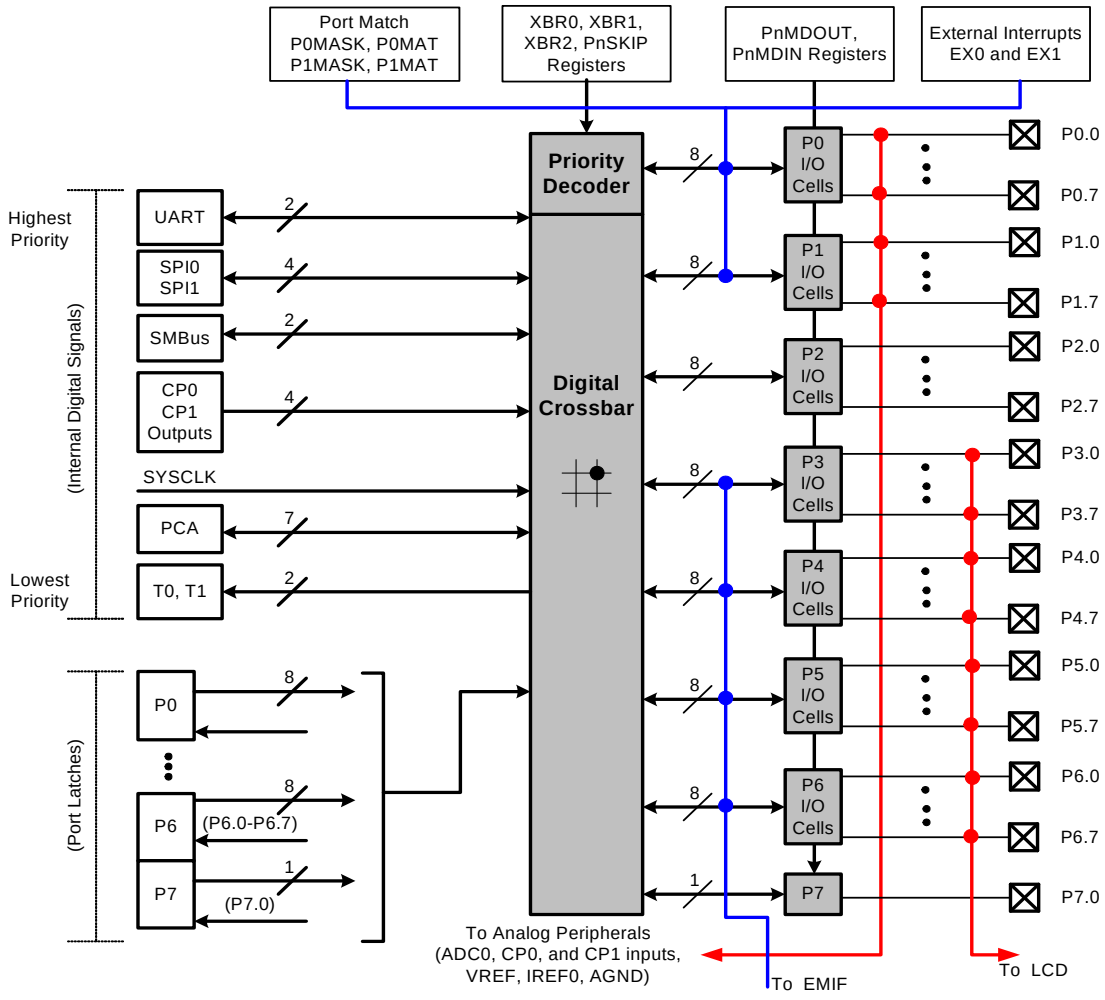


Figure 27.1. Port I/O Functional Block Diagram

SFR Definition 27.28. P4MDIN: Port4 Input Mode

Bit	7	6	5	4	3	2	1	0
Name	P4MDIN[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Page = 0xF; SFR Address = 0xF2

Bit	Name	Function
7:0	P4MDIN[3:0]	**Analog Configuration Bits for P4.7–P4.0 (respectively).** Port pins configured for analog mode have their weak pullup and digital receiver disabled. The digital driver is not explicitly disabled. 0: Corresponding P4.n pin is configured for analog mode. 1: Corresponding P4.n pin is not configured for analog mode.

SFR Definition 27.29. P4MDOUT: Port4 Output Mode

Bit	7	6	5	4	3	2	1	0
Name	P4MDOUT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0xF; SFR Address = 0xF9

Bit	Name	Function
7:0	P4MDOUT[7:0]	**Output Configuration Bits for P4.7–P4.0 (respectively).** These bits control the digital driver even when the corresponding bit in register P4MDIN is logic 0. 0: Corresponding P4.n Output is open-drain. 1: Corresponding P4.n Output is push-pull.

Table 28.1. SMBus Clock Source Selection

SMBCS1	SMBCS0	SMBus Clock Source
0	0	Timer 0 Overflow
0	1	Timer 1 Overflow
1	0	Timer 2 High Byte Overflow
1	1	Timer 2 Low Byte Overflow

The SMBCS1–0 bits select the SMBus clock source, which is used only when operating as a master or when the Free Timeout detection is enabled. When operating as a master, overflows from the selected source determine the absolute minimum SCL low and high times as defined in Equation 28.1. The selected clock source may be shared by other peripherals so long as the timer is left running at all times. For example, Timer 1 overflows may generate the SMBus and UART baud rates simultaneously. Timer configuration is covered in Section “32. Timers” on page 444.

$$T_{HighMin} = T_{LowMin} = \frac{1}{f_{ClockSourceOverflow}}$$

Equation 28.1. Minimum SCL High and Low Times

The selected clock source should be configured to establish the minimum SCL High and Low times as per Equation 28.1. When the interface is operating as a master (and SCL is not driven or extended by any other devices on the bus), the typical SMBus bit rate is approximated by Equation 28.1.

$$BitRate = \frac{f_{ClockSourceOverflow}}{3}$$

Equation 28.2. Typical SMBus Bit Rate

Figure 28.4 shows the typical SCL generation described by Equation 28.2. Notice that T_{HIGH} is typically twice as large as T_{LOW}. The actual SCL output may vary due to other devices on the bus (SCL may be extended low by slower slave devices, or driven low by contending master devices). The bit rate when operating as a master will never exceed the limits defined by Equation 28.2.

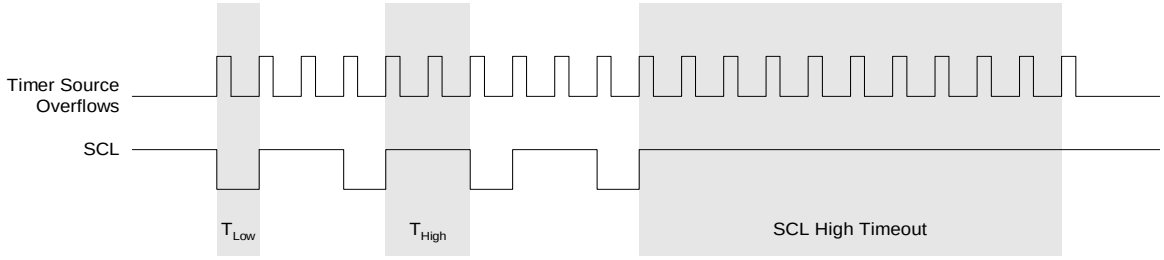


Figure 28.4. Typical SMBus SCL Generation

Setting the EXTHOLD bit extends the minimum setup and hold times for the SDA line. The minimum SDA setup time defines the absolute minimum time that SDA is stable before SCL transitions from low-to-high. The minimum SDA hold time defines the absolute minimum time that the current SDA value remains stable after SCL transitions from high-to-low. EXTHOLD should be set so that the minimum setup and hold times meet the SMBus Specification requirements of 250 ns and 300 ns, respectively. Table 28.2 shows the minimum setup and hold times for the two EXTHOLD settings. Setup and hold time extensions are typically necessary when SYSCLK is above 10 MHz.

SFR Definition 31.1. SPI1CFG: SPI1 Configuration

Bit	7	6	5	4	3	2	1	0
Name	SPIBSY	MSTEN	CKPHA	CKPOL	SLVSEL	NSSIN	SRMT	RXBMT
Type	R	R/W	R/W	R/W	R	R	R	R
Reset	0	0	0	0	0	1	1	1

SFR Page = 0x0; SFR Address = 0x84

Bit	Name	Function
7	SPIBSY	**SPI Busy.** This bit is set to logic 1 when a SPI transfer is in progress (master or slave mode).
6	MSTEN	**Master Mode Enable.** 0: Disable master mode. Operate in slave mode. 1: Enable master mode. Operate as a master.
5	CKPHA	**SPI1 Clock Phase.** 0: Data centered on first edge of SCK period.* 1: Data centered on second edge of SCK period.*
4	CKPOL	**SPI1 Clock Polarity.** 0: SCK line low in idle state. 1: SCK line high in idle state.
3	SLVSEL	**Slave Selected Flag.** This bit is set to logic 1 whenever the NSS pin is low indicating SPI1 is the selected slave. It is cleared to logic 0 when NSS is high (slave not selected). This bit does not indicate the instantaneous value at the NSS pin, but rather a de-glitched version of the pin input.
2	NSSIN	**NSS Instantaneous Pin Input.** This bit mimics the instantaneous value that is present on the NSS port pin at the time that the register is read. This input is not de-glitched.
1	SRMT	**Shift Register Empty (valid in slave mode only).** This bit will be set to logic 1 when all data has been transferred in/out of the shift register, and there is no new information available to read from the transmit buffer or write to the receive buffer. It returns to logic 0 when a data byte is transferred to the shift register from the transmit buffer or by a transition on SCK. SRMT = 1 when in Master Mode.
0	RXBMT	**Receive Buffer Empty (valid in slave mode only).** This bit will be set to logic 1 when the receive buffer has been read and contains no new information. If there is new information available in the receive buffer that has not been read, this bit will return to logic 0. RXBMT = 1 when in Master Mode.

Note: In slave mode, data on MOSI is sampled in the center of each data bit. In master mode, data on MISO is sampled one SYSCLK before the end of each data bit, to provide maximum settling time for the slave device. See Table 31.1 for timing parameters.

SFR Definition 32.8. TMR2CN: Timer 2 Control

Bit	7	6	5	4	3	2	1	0
Name	TF2H	TF2L	TF2LEN	TF2CEN	T2SPLIT	TR2	T2XCLK[1:0]	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xC8; Bit-Addressable

Bit	Name	Function
7	TF2H	**Timer 2 High Byte Overflow Flag.** Set by hardware when the Timer 2 high byte overflows from 0xFF to 0x00. In 16 bit mode, this will occur when Timer 2 overflows from 0xFFFF to 0x0000. When the Timer 2 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 2 interrupt service routine. This bit is not automatically cleared by hardware.
6	TF2L	**Timer 2 Low Byte Overflow Flag.** Set by hardware when the Timer 2 low byte overflows from 0xFF to 0x00. TF2L will be set when the low byte overflows regardless of the Timer 2 mode. This bit is not automatically cleared by hardware.
5	TF2LEN	**Timer 2 Low Byte Interrupt Enable.** When set to 1, this bit enables Timer 2 Low Byte interrupts. If Timer 2 interrupts are also enabled, an interrupt will be generated when the low byte of Timer 2 overflows.
4	TF2CEN	**Timer 2 Capture Enable.** When set to 1, this bit enables Timer 2 Capture Mode.
3	T2SPLIT	**Timer 2 Split Mode Enable.** When set to 1, Timer 2 operates as two 8-bit timers with auto-reload. Otherwise, Timer 2 operates in 16-bit auto-reload mode.
2	TR2	**Timer 2 Run Control.** Timer 2 is enabled by setting this bit to 1. In 8-bit mode, this bit enables/disables TMR2H only; TMR2L is always enabled in split mode.
1:0	T2XCLK[1:0]	**Timer 2 External Clock Select.** This bit selects the “external” and “capture trigger” clock sources for Timer 2. If Timer 2 is in 8-bit mode, this bit selects the “external” clock source for both timer bytes. Timer 2 Clock Select bits (T2MH and T2ML in register CKCON) may still be used to select between the “external” clock and the system clock for either timer. Note: External clock sources are synchronized with the system clock. 00: External Clock is SYSCLK/12. Capture trigger is SmaRTClock/8. 01: External Clock is Comparator 0. Capture trigger is SmaRTClock/8. 10: External Clock is SYSCLK/12. Capture trigger is Comparator 0. 11: External Clock is SmaRTClock/8. Capture trigger is Comparator 0.

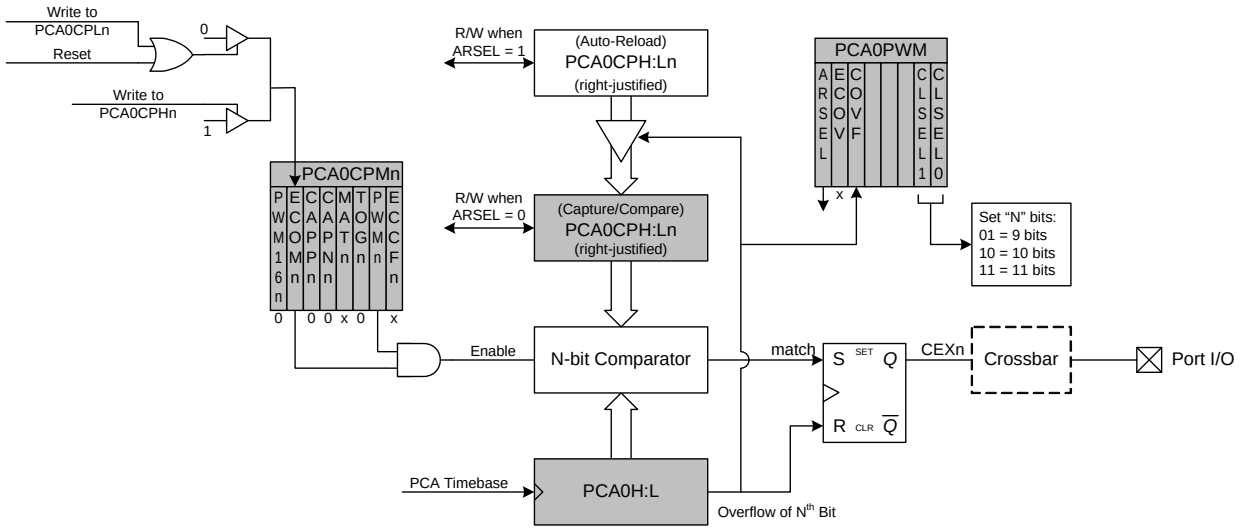


Figure 33.9. PCA 9, 10 and 11-Bit PWM Mode Diagram

33.3.6. 16-Bit Pulse Width Modulator Mode

A PCA module may also be operated in 16-Bit PWM mode. 16-bit PWM mode is independent of the other (8/9/10/11-bit) PWM modes. In this mode, the 16-bit capture/compare module defines the number of PCA clocks for the low time of the PWM signal. When the PCA counter matches the module contents, the output on CEXn is asserted high; when the 16-bit counter overflows, CEXn is asserted low. To output a varying duty cycle, new value writes should be synchronized with PCA CCFn match interrupts. 16-Bit PWM Mode is enabled by setting the ECOMn, PWMn, and PWM16n bits in the PCA0CPMn register. For a varying duty cycle, match interrupts should be enabled (ECCFn = 1 AND MATn = 1) to help synchronize the capture/compare register writes. If the MATn bit is set to 1, the CCFn flag for the module will be set each time a 16-bit comparator match (rising edge) occurs. The CF flag in PCA0CN can be used to detect the overflow (falling edge). The duty cycle for 16-Bit PWM Mode is given by Equation 33.4.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

$$\text{Duty Cycle} = \frac{(65536 - PCA0CPn)}{65536}$$

Equation 33.4. 16-Bit PWM Duty Cycle

Using Equation 33.4, the largest duty cycle is 100% (PCA0CPn = 0), and the smallest duty cycle is 0.0015% (PCA0CPn = 0xFFFF). A 0% duty cycle may be generated by clearing the ECOMn bit to 0.

SFR Definition 33.5. PCA0L: PCA Counter/Timer Low Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xF9

Bit	Name	Function
7:0	PCA0[7:0]	**PCA Counter/Timer Low Byte.** The PCA0L register holds the low byte (LSB) of the 16-bit PCA Counter/Timer.
Note: When the WDTE bit is set to 1, the PCA0L register cannot be modified by software. To change the contents of the PCA0L register, the Watchdog Timer must first be disabled.		

SFR Definition 33.6. PCA0H: PCA Counter/Timer High Byte

Bit	7	6	5	4	3	2	1	0
Name	PCA0[15:8]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xFA

Bit	Name	Function
7:0	PCA0[15:8]	**PCA Counter/Timer High Byte.** The PCA0H register holds the high byte (MSB) of the 16-bit PCA Counter/Timer. Reads of this register will read the contents of a “snapshot” register, whose contents are updated only when the contents of PCA0L are read (see Section 33.1).
Note: When the WDTE bit is set to 1, the PCA0H register cannot be modified by software. To change the contents of the PCA0H register, the Watchdog Timer must first be disabled.		