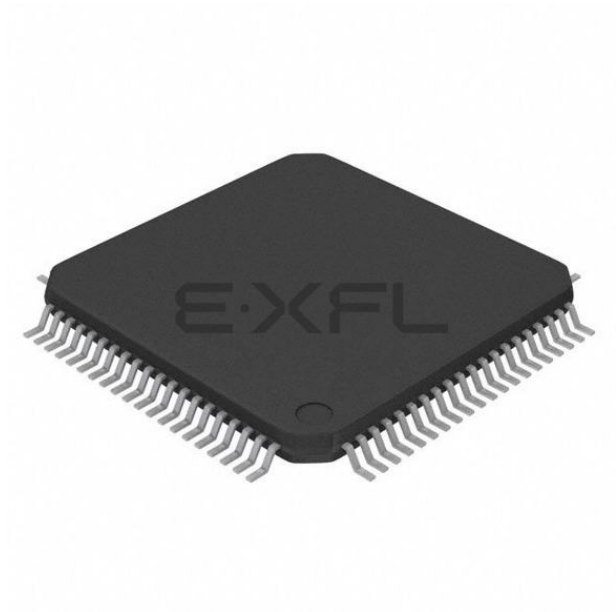

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, LCD, POR, PWM, WDT
Number of I/O	57
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f964-a-gqr

1.2. Port Input/Output

Digital and analog resources are available through 57 I/O pins (C8051F960/2/4/6/8) or 34 I/O pins (C8051F961/3/5/7/9). Port pins are organized as eight byte-wide ports. Port pins can be defined as digital or analog I/O. Digital I/O pins can be assigned to one of the internal digital resources or used as general purpose I/O (GPIO). Analog I/O pins are used by the internal analog resources. P7.0 can be used as GPIO and is shared with the C2 Interface Data signal (C2D). See Section “34. C2 Interface” on page 486 for more details.

The designer has complete control over which digital and analog functions are assigned to individual port pins. This resource assignment flexibility is achieved through the use of a Priority Crossbar Decoder. See Section “27. Port Input/Output” on page 351 for more information on the Crossbar.

For Port I/Os configured as push-pull outputs, current is sourced from the VIO, VIORF, or VBAT supply pin. Port I/Os used for analog functions can operate up to the supply voltage. See Section “27. Port Input/Output” on page 351 for more information on Port I/O operating modes and the electrical specifications chapter for detailed electrical specifications.

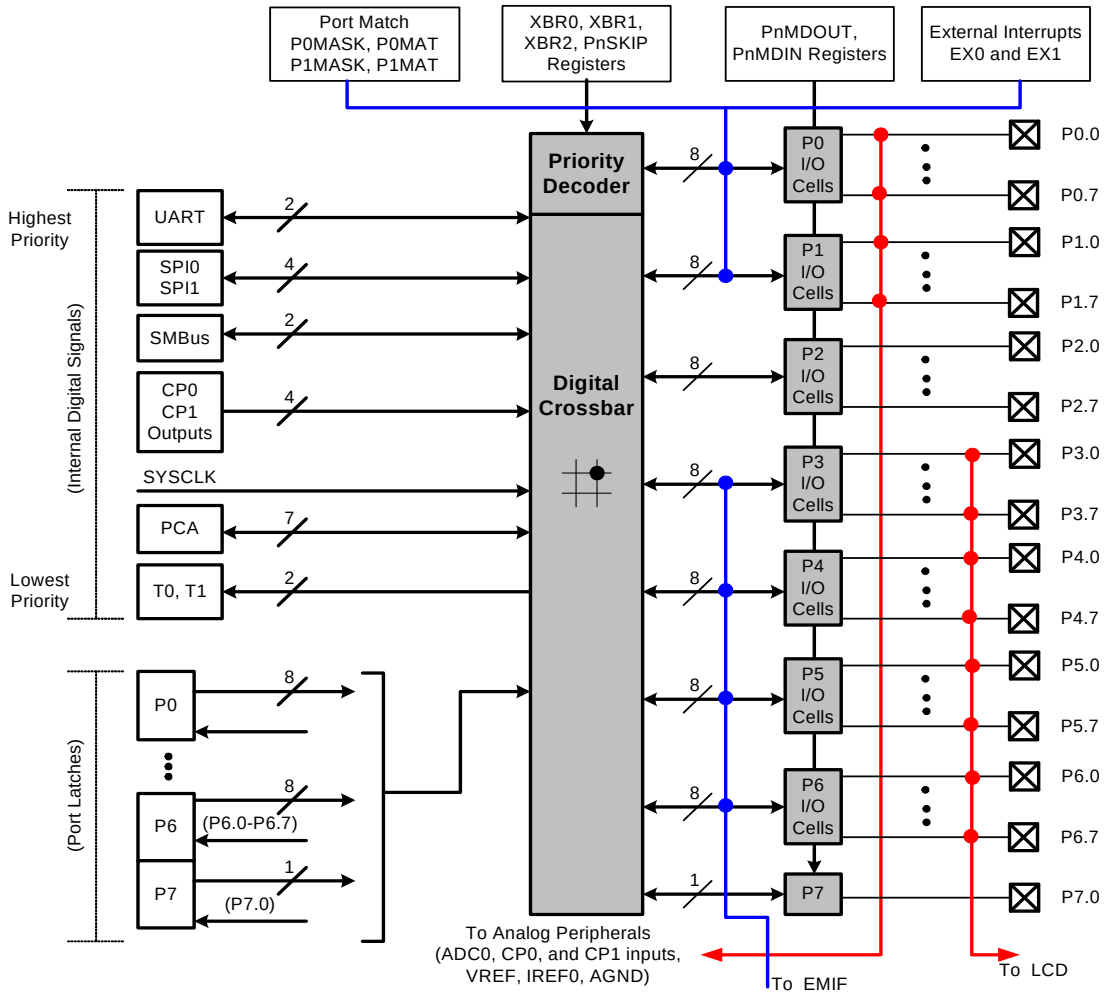

Figure 1.11. Port I/O Functional Block Diagram

2. Ordering Information

Table 2.1. Product Selection Guide

Ordering Part Number	MIPS (Peak)	Flash Memory (kB)	RAM (bytes)	Digital Port I/Os	AES 128, 192, 256 Encryption	LCD Segments (4-MUX)	SmaRTClock Real Time Clock	SMBus/I^2C	UART	Enhanced SPI	Timers (16-bit)	PCA Channels	10/12-bit 300/75 ksps ADC channels with internal VREF and temp sensor	Analog Comparators	Package
C8051F960-B-GM	25	128	8448	57	✓	128	✓	1	1	2	4	6	16	2	DQFN-76 (6x6)
C8051F960-B-GQ	25	128	8448	57	✓	128	✓	1	1	2	4	6	16	2	TQFP80 (12x12)
C8051F961-B-GM	25	128	8448	34	✓	36	✓	1	1	2	4	6	16	2	QFN-40 (6x6)
C8051F962-B-GM	25	128	8448	57	✓	—	✓	1	1	2	4	6	16	2	DQFN-76 (6x6)
C8051F962-B-GQ	25	128	8448	57	✓	—	✓	1	1	2	4	6	16	2	TQFP80 (12x12)
C8051F963-B-GM	25	128	8448	34	✓	—	✓	1	1	2	4	6	16	2	QFN-40 (6x6)
C8051F964-B-GM	25	64	8448	57	✓	128	✓	1	1	2	4	6	16	2	DQFN-76 (6x6)
C8051F964-B-GQ	25	64	8448	57	✓	128	✓	1	1	2	4	6	16	2	TQFP80 (12x12)
C8051F965-B-GM	25	64	8448	34	✓	36	✓	1	1	2	4	6	16	2	QFN-40 (6x6)
C8051F966-B-GM	25	32	8448	57	✓	128	✓	1	1	2	4	6	16	2	DQFN-76 (6x6)
C8051F966-B-GQ	25	32	8448	57	✓	128	✓	1	1	2	4	6	16	2	TQFP80 (12x12)
C8051F967-B-GM	25	32	8448	34	✓	36	✓	1	1	2	4	6	16	2	QFN-40 (6x6)
C8051F968-B-GM	25	16	4352	57	✓	128	✓	1	1	2	4	6	16	2	DQFN-76 (6x6)
C8051F968-B-GQ	25	16	4352	57	✓	128	✓	1	1	2	4	6	16	2	TQFP80 (12x12)
C8051F969-B-GM	25	16	4352	34	✓	36	✓	1	1	2	4	6	16	2	QFN-40 (6x6)

All packages are Lead-free (RoHS Compliant).

Rev A not recommended for new designs.

Table 3.1. Pin Definitions for the C8051F96x (Continued)

Name	Pin Numbers			Type	Description
	DQFN76	TQFP80	QFN40		
P5.2 LCD18	B23	63		D I/O or A In A O	Port 5.2. See Port I/O Section for a complete description. LCD Segment Pin 18
P5.3 LCD19	B22	62		D I/O or A In A O	Port 5.3. See Port I/O Section for a complete description. LCD Segment Pin 19
P5.4 LCD20	D4	59		D I/O or A In A O	Port 5.4. See Port I/O Section for a complete description. LCD Segment Pin 20
P5.5 LCD21	B21	55		D I/O or A In A O	Port 5.5. See Port I/O Section for a complete description. LCD Segment Pin 21
P5.6 LCD22	B15	44		D I/O or A In A O	Port 5.6. See Port I/O Section for a complete description. LCD Segment Pin 22
P5.7 LCD23	D3	42		D I/O or A In A O	Port 5.7. See Port I/O Section for a complete description. LCD Segment Pin 23
P6.0 LCD24	B14	40		D I/O or A In A O	Port 6.0. See Port I/O Section for a complete description. LCD Segment Pin 24
P6.1 LCD25	B13	37		D I/O or A In A O	Port 6.1. See Port I/O Section for a complete description. LCD Segment Pin 25

Table 4.14. Voltage Reference Electrical Characteristics

V_{BAT} = 1.8 to 3.8 V, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Internal High-Speed Reference (REFSL[1:0] = 11)					
Output Voltage	–40 to +85 °C, V_{BAT} = 1.8–3.8 V	1.62	1.65	1.68	V
VREF Turn-on Time		—	—	1.5	µs
Supply Current	Normal Power Mode Low Power Mode	— —	260 140	— —	µA
External Reference (REFSL[1:0] = 00, REFOE = 0)					
Input Voltage Range		0	—	V_{BAT}	V
Input Current	Sample Rate = 300 ksps; VREF = 3.0 V	—	5.25	—	µA

SFR Definition 5.3. ADC0AC: ADC0 Accumulator Configuration

Bit	7	6	5	4	3	2	1	0
Name	AD012BE	AD0AE	AD0SJST[2:0]			AD0RPT[2:0]		
Type	R/W	W	R/W			R/W		
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xBA

Bit	Name	Function
7	AD012BE	**ADC0 12-Bit Mode Enable.** Enables 12-bit Mode. 0: 12-bit Mode Disabled. 1: 12-bit Mode Enabled.
6	AD0AE	**ADC0 Accumulate Enable.** Enables multiple conversions to be accumulated when burst mode is disabled. 0: ADC0H:ADC0L contain the result of the latest conversion when Burst Mode is disabled. 1: ADC0H:ADC0L contain the accumulated conversion results when Burst Mode is disabled. Software must write 0x0000 to ADC0H:ADC0L to clear the accumulated result. This bit is write-only. Always reads 0b.
5:3	AD0SJST[2:0]	**ADC0 Accumulator Shift and Justify.** Specifies the format of data read from ADC0H:ADC0L. 000: Right justified. No shifting applied. 001: Right justified. Shifted right by 1 bit. 010: Right justified. Shifted right by 2 bits. 011: Right justified. Shifted right by 3 bits. 100: Left justified. No shifting applied. All remaining bit combinations are reserved.
2:0	AD0RPT[2:0]	**ADC0 Repeat Count.** Selects the number of conversions to perform and accumulate in Burst Mode. This bit field must be set to 000 if Burst Mode is disabled. 000: Perform and Accumulate 1 conversion. 001: Perform and Accumulate 4 conversions. 010: Perform and Accumulate 8 conversions. 011: Perform and Accumulate 16 conversions. 100: Perform and Accumulate 32 conversions. 101: Perform and Accumulate 64 conversions. All remaining bit combinations are reserved.

Table 16.3. Special Function Registers

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	SFR Page	Description	Page
ADC0AC	0xBA	0x0	ADC0 Accumulator Configuration	88
ADC0CF	0xBC	0x0	ADC0 Configuration	87
ADC0CN	0xE8	All pages	ADC0 Control	86
ADC0GTH	0xC4	0x0	ADC0 Greater-Than Compare High	92
ADC0GTL	0xC3	0x0	ADC0 Greater-Than Compare Low	92
ADC0H	0xBE	0x0	ADC0 High	91
ADC0L	0xBD	0x0	ADC0 Low	91
ADC0LTH	0xC6	0x0	ADC0 Less-Than Compare Word High	93
ADC0LTL	0xC5	0x0	ADC0 Less-Than Compare Word Low	93
ADC0MX	0xBB	0x0	ADC0 MUX	96
ADC0PWR	0xBA	0xF	ADC0 Burst Mode Power-Up Time	89
ADC0TK	0xBB	0xF	ADC0 Tracking Control	90
AES0BCFG	0xE9	0x2	AES0 Block Configuration	202
AES0BIN	0xEB	0x2	AES0 Block Input	204
AES0DCFG	0xEA	0x2	AES0 Data Configuration	203
AES0KIN	0xED	0x2	AES0 Key Input	205
AES0XIN	0xEC	0x2	AES0 XOR Input	205
AES0YOUT	0xF5	0x2	AES Y Out	206
CKCON	0x8E	0x0	Clock Control	445
CLKMODE	0xFD	0xF	Clock Mode	262
CLKSEL	0xA9	0x0 and 0xF	Clock Select	291
CPT0CN	0x9B	0x0	Comparator0 Control	108
CPT0MD	0x9D	0x0	Comparator0 Mode Selection	109
CPT0MX	0x9F	0x0	Comparator0 Mux Selection	113
CPT1CN	0x9A	0x0	Comparator1 Control	110
CPT1MD	0x9C	0x0	Comparator1 Mode Selection	111
CPT1MX	0x9E	0x0	Comparator1 Mux Selection	114
CRC0AUTO	0x96	0xF	CRC0 Automatic Control	166
CRC0CNT	0x97	0xF	CRC0 Automatic Flash Sector Count	166
CRC0CN	0x92	0xF	CRC0 Control	164
CRC0DAT	0x91	0xF	CRC0 Data	165
CRC0FLIP	0x94	0xF	CRC0 Flip	167
CRC0IN	0x93	0xF	CRC0 Input	165

Table 16.3. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	SFR Page	Description	Page
P2	0xA0	All Pages	Port 2 Latch	369
P3DRV	0xA1	0xF	Port 3 Drive Strength	373
P3MDIN	0xF1	0xF	Port 3 Input Mode Configuration	372
P3MDOUT	0xB1	0xF	P3 Mode Out	372
P3	0xB0	All Pages	Port 3	371
P4DRV	0xA2	0xF	Port 4 Drive Strength	375
P4MDIN	0xF2	0xF	Port 4 Input Mode Configuration	374
P4MDOUT	0xF9	0xF	P4 Mode Out	374
P4	0xD9	0xF	Port 4 Latch	373
P5DRV	0xA3	0xF	Port 5 Drive Strength	377
P5MDIN	0xF3	0xF	Port 5 Input Mode Configuration	376
P5MDOUT	0xFA	0xF	P5 Mode Out	376
P5	0xDA	0xF	Port 5 Latch	375
P6DRV	0xAA	0xF	Port 6 Drive Strength	379
P6MDIN	0xF4	0xF	Port 6 Input Mode Configuration	378
P6MDOUT	0xFB	0xF	P6 Mode Out	378
P6	0xDB	0xF	Port 6 Latch	377
P7DRV	0xAB	0xF	Port 7 Drive Strength	380
P7MDOUT	0xFC	0xF	P7 Mode Out	380
P7	0xDC	0xF	Port 7 Latch	379
PC0CMP0H	0xE3	0x2	PC0 Comparator 0 High	329
PC0CMP0L	0xE1	0x2	PC0 Comparator 0 Low	329
PC0CMP0M	0xE2	0x2	PC0 Comparator 0 Middle	329
PC0CMP1H	0xF3	0x2	PC0 Comparator 1 High	330
PC0CMP1L	0xF1	0x2	PC0 Comparator 1 Low	330
PC0CMP1M	0xF2	0x2	PC0 Comparator 1 Middle	330
PC0CTR0H	0xDC	0x2	PC0 Counter 0 High	327
PC0CTR0L	0xDA	0x2	PC0 Counter 0 Low	327
PC0CTR0M	0xD8	0x2	PC0 Counter 0 Middle	327
PC0CTR1H	0xDF	0x2	PC0 Counter 1 High	328
PC0CTR1L	0xDD	0x2	PC0 Counter 1 Low	328
PC0DCH	0xFA	0x2	PC0 Debounce Configuration High	325
PC0DCL	0xF9	0x2	PC0 Debounce Configuration Low	326
PC0HIST	0xF4	0x2	PC0 History	331

SFR Definition 17.7. IT01CF: $\overline{\text{INT0}}$/$\overline{\text{INT1}}$ Configuration

Bit	7	6	5	4	3	2	1	0
Name	IN1PL	IN1SL[2:0]			IN0PL	IN0SL[2:0]		
Type	R/W	R/W			R/W	R/W		
Reset	0	0	0	0	0	0	0	1

SFR Page = 0x0; SFR Address = 0xE4

Bit	Name	Function
7	IN1PL	**$\overline{\text{INT1}}$ Polarity.** 0: $\overline{\text{INT1}}$ input is active low. 1: $\overline{\text{INT1}}$ input is active high.
6:4	IN1SL[2:0]	**$\overline{\text{INT1}}$ Port Pin Selection Bits.** These bits select which Port pin is assigned to $\overline{\text{INT1}}$. Note that this pin assignment is independent of the Crossbar; $\overline{\text{INT1}}$ will monitor the assigned Port pin without disturbing the peripheral that has been assigned the Port pin via the Crossbar. The Crossbar will not assign the Port pin to a peripheral if it is configured to skip the selected pin. 000: Select P0.0 001: Select P0.1 010: Select P0.2 011: Select P0.3 100: Select P0.4 101: Select P0.5 110: Select P1.6 111: Select P1.7
3	IN0PL	**$\overline{\text{INT0}}$ Polarity.** 0: $\overline{\text{INT0}}$ input is active low. 1: $\overline{\text{INT0}}$ input is active high.
2:0	IN0SL[2:0]	**$\overline{\text{INT0}}$ Port Pin Selection Bits.** These bits select which Port pin is assigned to $\overline{\text{INT0}}$. Note that this pin assignment is independent of the Crossbar; $\overline{\text{INT0}}$ will monitor the assigned Port pin without disturbing the peripheral that has been assigned the Port pin via the Crossbar. The Crossbar will not assign the Port pin to a peripheral if it is configured to skip the selected pin. 000: Select P0.0 001: Select P0.1 010: Select P0.2 011: Select P0.3 100: Select P0.4 101: Select P0.5 110: Select P1.6 111: Select P1.7

18.1.4. Flash Write Optimization

The flash write procedure includes a block write option to optimize the time to perform consecutive byte writes. When block write is enabled by setting the CHBLKW bit (FLRBCN.0), writes to flash will occur in blocks of 4 bytes and require the same amount of time as a single byte write. This is performed by caching the bytes whose address end in 00b, 01b, and 10b that is written to flash and then committing all four bytes to flash when the byte with address 11b is written. When block writes are enabled, if the write to the byte with address 11b does not occur, the other three data bytes written is not committed to flash.

A write to flash memory can clear bits to logic 0 but cannot set them; only an erase operation can set bits to logic 1 in flash. **The Flash Block to be programmed should be erased before a new value is written.**

The recommended procedure for writing a 4-byte flash block is as follows:

1. Save current interrupt state and disable interrupts.
2. Set the CHBLKW bit (register FLRBCN).
3. Set the PSWE bit (register PSCTL).
4. Clear the PSEE bit (register PSCTL).
5. If writing to an address in Banks 1, 2, or 3, set the COBANK[1:0] bits (register PSBANK) for the appropriate bank
6. Write the first key code to FLKEY: 0xA5.
7. Write the second key code to FLKEY: 0xF1.
8. Using the MOVX instruction, write the first data byte to the desired location within the 1024-byte sector whose address ends in 00b.
9. Write the first key code to FLKEY: 0xA5.
10. Write the second key code to FLKEY: 0xF1.
11. Using the MOVX instruction, write the second data byte to the next higher flash address ending in 01b.
12. Write the first key code to FLKEY: 0xA5.
13. Write the second key code to FLKEY: 0xF1.
14. Using the MOVX instruction, write the third data byte to the next higher flash address ending in 10b.
15. Write the first key code to FLKEY: 0xA5.
16. Write the second key code to FLKEY: 0xF1.
17. Using the MOVX instruction, write the final data byte to the next higher flash address ending in 11b.
18. Clear the PSWE bit.
19. Clear the CHBLKW bit.
20. Restore previous interrupt state.

Steps 5–17 must be repeated for each flash block to be written.

Notes:

1. Flash security settings may prevent writes to some areas of flash, such as the reserved area. For a summary of flash security settings and restrictions affecting flash write operations, please see Section “18.3. Security Options” on page 247.
2. 8-bit MOVX instructions cannot be used to erase or write to flash memory at addresses higher than 0x00FF.

SFR Definition 19.2. PCLKEN: Peripheral Clock Enable

Bit	7	6	5	4	3	2	1	0
Name					PCLKEN[3:0]			
Type	R/W	R/W	R/W	R/W	R/W			
Reset								

SFR Page = 0xF; SFR Address = 0xFE

Bit	Name	Function
7:4	Unused	Read = 0b; Write = don't care.
3	PCLKEN3	**Clock Enable Controls for Peripherals in Low Power Idle Mode.** 0: Disable clocks to the SmaRTClock, Pulse Counter, and PMU0 in Low Power Idle Mode. 1: Enable clocks to the SmaRTClock, Pulse Counter, and PMU0 in Low Power Idle Mode.
2	PCLKEN2	**Clock Enable Controls for Peripherals in Low Power Idle Mode.** 0: Disable clocks to Timer 0, Timer 1, Timer 2, and CRC0 in Low Power Idle Mode. 1: Enable clocks to Timer 0, Timer 1, Timer 2, and CRC0 in Low Power Idle Mode.
1	PCLKEN1	**Clock Enable Controls for Peripherals in Low Power Idle Mode.** 0: Disableclocks to ADC0 and PCA0 in Low Power Idle Mode. 1: Enable clocks to ADC0 and PCA0 in Low Power Idle Mode.
0	PCLKEN0	**Clock Enable Controls for Peripherals in Low Power Idle Mode.** 0: Disable clocks to UART0, Timer 3, SPI0, and the SMBus in Low Power Idle Mode. 1: Enable clocks to UART0, Timer 3, SPI0, and the SMBus in Low Power Idle Mode.

20. On-Chip DC-DC Buck Converter (DC0)

C8051F96x devices include an on-chip step down dc-dc converter to efficiently utilize the energy stored in the battery, thus extending the operational life time. The dc-dc converter is a switching buck converter with an input supply of 1.8 to 3.8 V and an output that is programmable from 1.8 to 3.5 V in steps of 0.1 V. The battery voltage should be at least 0.4 V higher than the programmed output voltage. The programmed output voltage has a default value of 1.9 V. The dc-dc converter can supply up to 250 mW. The dc-dc converter can be used to power the MCU and/or external devices in the system (e.g., an RF transceiver).

The dc-dc converter has a built in voltage reference and oscillator, and will automatically limit or turn off the switching activity in case the peak inductor current rises beyond a safe limit or the output voltage rises above the programmed target value. This allows the dc-dc converter output to be safely overdriven by a secondary power source (when available) in order to preserve battery life. When enabled, the dc-dc converter can source current into the output capacitor, but cannot sink current. The dc-dc converter's settings can be modified using SFR registers described in Section 20.8.

Figure 20.1 shows a block diagram of the buck converter.

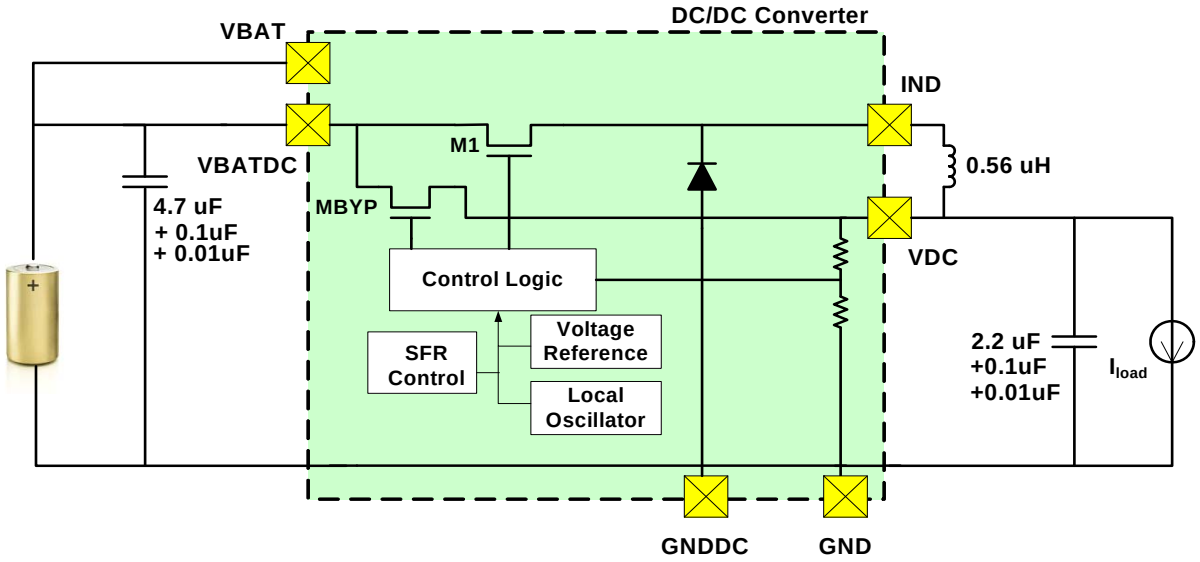

Figure 20.1. Step Down DC-DC Buck Converter Block Diagram

SFR Definition 25.19. PC0HIST: PC0 History

Bit	7	6	5	4	3	2	1	0
Name	PC0HIST[7:0]							
Type	R							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xF4; SFR Page = 0x2

Bit	Name	Function
7:0	PC0HIST[7:0]	**PC0 History.** Contains the last 8 recorded directions (1: clock-wise, 0: counter clock-wise) on the previous 8 counts. Values of 0x55 or 0xAA may indicate flutter during quadrature mode.

LCD0CF Register.

8. Set the LCD contrast using the LCD0CNTRST register.
9. Set the desired threshold for the VBAT Supply Monitor.
10. Set the LCD refresh rate using the LCD0DIVH:LCD0DIVL registers.
11. Write a pattern to the LCD0Dn registers.
12. Enable the LCD by setting bit 0 of LCD0MSCN to logic 1 (LCD0MSCN |= 0x01).

26.2. Mapping Data Registers to LCD Pins

The LCD0 data registers are organized as 16 byte-wide special function registers (LCD0Dn), each half-byte or nibble in these registers controls 1 LCD output pin. There are 32 nibbbles used to control the 32 segment pins.

Each LCD0 segment pin can control 1, 2, 3, or 4 LCD segments depending on the selected mux mode. The least significant bit of each nibble controls the segment connected to the backplane signal COM0. The next to least significant bit controls the segment associated with COM1, the next bit controls the segment associated with COM2, and the most significant bit in the 4-bit nibble controls the segment associated with COM3.

In static mode, only the least significant bit in each nibble is used and the three remaining bits in each nibble are ignored. In 2-mux mode, only the two least significant bits are used; in 3-mux mode, only the three least significant bits are used, and in 4-mux mode, each of the 4 bits in the nibble controls one LCD segment. Bits with a value of 1 turn on the associated segment and bits with a value of 0 turn off the associated segment.

SFR Definition 26.1. LCD0Dn: LCD0 Data

Bit	7	6	5	4	3	2	1	0
Name	LCD0Dn							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page: 0x2

Addresses: LCD0D0 = 0x89, LCD0D1 = 0x8A, LCD0D2 = 0x8B, LCD0D3 = 0x8C,
LCD0D4 = 0x8D, LCD0D5 = 0x8E, LCD0D6 = 0x91, LCD0D7 = 0x92,
LCD0D8 = 0x93, LCD0D9 = 0x94, LCD0DA = 0x95, LCD0DB = 0x96,
LCD0DC = 0x97, LCD0DD = 0x99, LCD0DE = 0x9A, LCD0DF = 0x9B.

Bit	Name	Function
7:0	LCD0Dn	**LCD Data.** Each nibble controls one LCD pin. See “Mapping Data Registers to LCD Pins” on page 335 for additional information.

26.6. Blinking LCD Segments

The LCD driver supports blinking LCD applications such as clock applications where the ":" separator toggles on and off once per second. If the LCD is only displaying the hours and minutes, then the device only needs to wake up once per minute to update the display. The once per second blinking is automatically handled by the C8051F96x.

The LCD0BLINK register can be used to enable blinking on any LCD segment connected to the LCD0 or LCD1 segment pin. In static mode, a maximum of 2 segments can blink. In 2-mux mode, a maximum of 4 segments can blink; in 3-mux mode, a maximum of 6 segments can blink; and in 4-mux mode, a maximum of 8 segments can blink. The LCD0BLINK mask register targets the same LCD segments as the LCD0D0 register. If an LCD0BLINK bit corresponding to an LCD segment is set to 1, then that segment will toggle at the frequency set by the LCD0TOGR register without any software intervention.

SFR Definition 26.10. LCD0BLINK: LCD0 Blink Mask

Bit	7	6	5	4	3	2	1	0
Name	LCD0BLINK[7:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x2; SFR Address = 0x9E

Bit	Name	Function
7:0	LCD0BLINK[7:0]	**LCD0 Blink Mask.** Each bit maps to a specific LCD segment connected to the LCD0 and LCD1 segment pins. A value of 1 indicates that the segment is blinking. A value of 0 indicates that the segment is not blinking. This bit to segment mapping is the same as the LCD0D0 register.

27.4. Port Match

Port match functionality allows system events to be triggered by a logic value change on P0 or P1. A software controlled value stored in the PnMAT registers specifies the expected or normal logic values of P0 and P1. A Port mismatch event occurs if the logic levels of the Port's input pins no longer match the software controlled value. This allows Software to be notified if a certain change or pattern occurs on P0 or P1 input pins regardless of the XBRn settings.

The PnMASK registers can be used to individually select which P0 and P1 pins should be compared against the PnMAT registers. A Port mismatch event is generated if (P0 & P0MASK) does not equal (PnMAT & P0MASK) or if (P1 & P1MASK) does not equal (PnMAT & P1MASK).

A Port mismatch event may be used to generate an interrupt or wake the device from a low power mode. See Section "17. Interrupt Handler" on page 232 and Section "19. Power Management" on page 257 for more details on interrupt and wake-up sources.

SFR Definition 27.4. P0MASK: Port0 Mask Register

Bit	7	6	5	4	3	2	1	0
Name	P0MASK[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page= 0x0; SFR Address = 0xC7

Bit	Name	Function
7:0	P0MASK[7:0]	**Port0 Mask Value.** Selects the P0 pins to be compared with the corresponding bits in P0MAT. 0: P0.n pin pad logic value is ignored and cannot cause a Port Mismatch event. 1: P0.n pin pad logic value is compared to P0MAT.n.

SFR Definition 27.5. P0MAT: Port0 Match Register

Bit	7	6	5	4	3	2	1	0
Name	P0MAT[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Page= 0x0; SFR Address = 0xD7

Bit	Name	Function
7:0	P0MAT[7:0]	**Port 0 Match Value.** Match comparison value used on Port 0 for bits in P0MASK which are set to 1. 0: P0.n pin logic value is compared with logic LOW. 1: P0.n pin logic value is compared with logic HIGH.

28. SMBus

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I^2C serial bus. Reads and writes to the interface by the system controller are byte oriented with the SMBus interface autonomously controlling the serial transfer of the data. Data can be transferred at up to 1/20th of the system clock as a master or slave (this can be faster than allowed by the SMBus specification, depending on the system clock used). A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus.

The SMBus interface may operate as a master and/or slave, and may function on a bus with multiple masters. The SMBus provides control of SDA (serial data), SCL (serial clock) generation and synchronization, arbitration logic, and START/STOP control and generation. The SMBus peripheral can be fully driven by software (i.e., software accepts/rejects slave addresses, and generates ACKs), or hardware slave address recognition and automatic ACK generation can be enabled to minimize software overhead. A block diagram of the SMBus peripheral and the associated SFRs is shown in Figure 28.1.

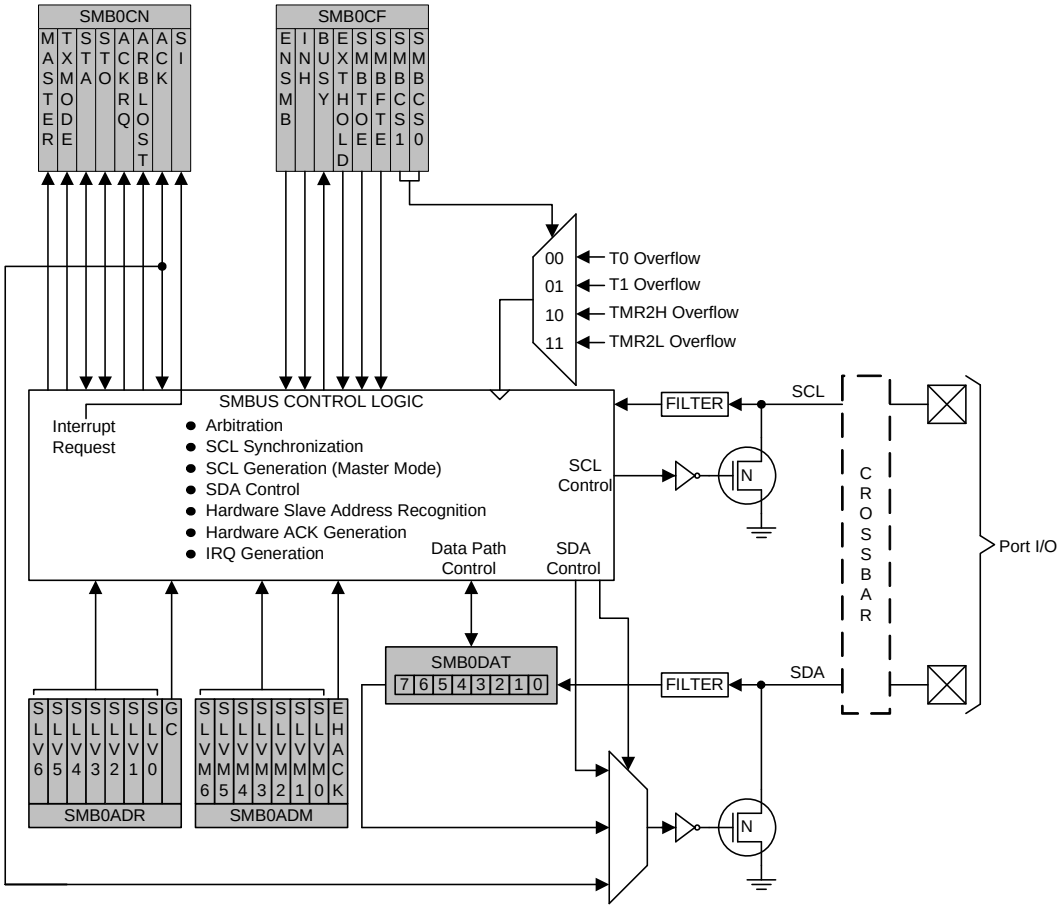

Figure 28.1. SMBus Block Diagram

SFR Definition 30.1. SPI0CFG: SPI0 Configuration

Bit	7	6	5	4	3	2	1	0
Name	SPIBSY	MSTEN	CKPHA	CKPOL	SLVSEL	NSSIN	SRMT	RXBMT
Type	R	R/W	R/W	R/W	R	R	R	R
Reset	0	0	0	0	0	1	1	1

SFR Page = 0x0; SFR Address = 0xA1

Bit	Name	Function
7	SPIBSY	**SPI Busy.** This bit is set to logic 1 when a SPI transfer is in progress (master or slave mode).
6	MSTEN	**Master Mode Enable.** 0: Disable master mode. Operate in slave mode. 1: Enable master mode. Operate as a master.
5	CKPHA	**SPI0 Clock Phase.** 0: Data centered on first edge of SCK period.* 1: Data centered on second edge of SCK period.*
4	CKPOL	**SPI0 Clock Polarity.** 0: SCK line low in idle state. 1: SCK line high in idle state.
3	SLVSEL	**Slave Selected Flag.** This bit is set to logic 1 whenever the NSS pin is low indicating SPI0 is the selected slave. It is cleared to logic 0 when NSS is high (slave not selected). This bit does not indicate the instantaneous value at the NSS pin, but rather a de-glitched version of the pin input.
2	NSSIN	**NSS Instantaneous Pin Input.** This bit mimics the instantaneous value that is present on the NSS port pin at the time that the register is read. This input is not de-glitched.
1	SRMT	**Shift Register Empty (valid in slave mode only).** This bit will be set to logic 1 when all data has been transferred in/out of the shift register, and there is no new information available to read from the transmit buffer or write to the receive buffer. It returns to logic 0 when a data byte is transferred to the shift register from the transmit buffer or by a transition on SCK. SRMT = 1 when in Master Mode.
0	RXBMT	**Receive Buffer Empty (valid in slave mode only).** This bit will be set to logic 1 when the receive buffer has been read and contains no new information. If there is new information available in the receive buffer that has not been read, this bit will return to logic 0. RXBMT = 1 when in Master Mode.

Note: In slave mode, data on MOSI is sampled in the center of each data bit. In master mode, data on MISO is sampled one SYSCLK before the end of each data bit, to provide maximum settling time for the slave device. See Table 30.1 for timing parameters.

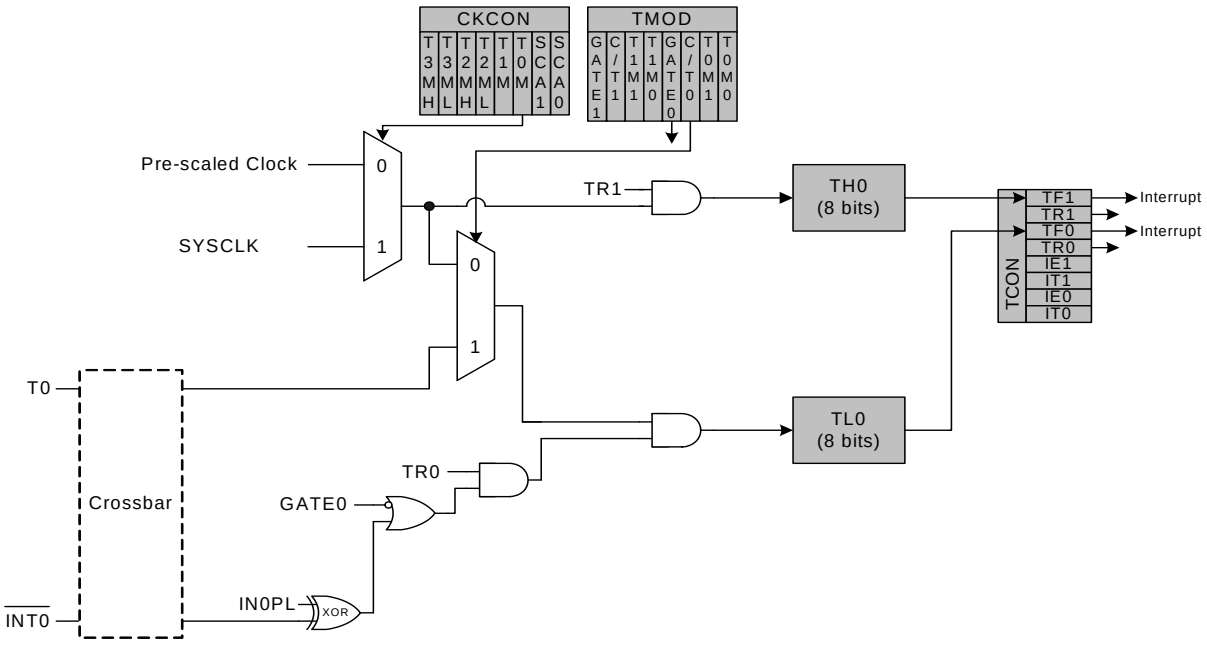

Figure 32.3. T0 Mode 3 Block Diagram

SFR Definition 32.6. TH0: Timer 0 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TH0[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0x8C

Bit	Name	Function
7:0	TH0[7:0]	**Timer 0 High Byte.** The TH0 register is the high byte of the 16-bit Timer 0.

SFR Definition 32.7. TH1: Timer 1 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TH1[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0x8D

Bit	Name	Function
7:0	TH1[7:0]	**Timer 1 High Byte.** The TH1 register is the high byte of the 16-bit Timer 1.