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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	DMA, LCD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8.25K × 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f965-a-gmr

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

# List of Figures

Figure 1.1. C8051F960 Block Diagram	23
Figure 1.2. C8051F961 Block Diagram	23
Figure 1.3. C8051F962 Block Diagram	24
Figure 1.4. C8051F963 Block Diagram	24
Figure 1.5. C8051F964 Block Diagram	25
Figure 1.6. C8051F965 Block Diagram	25
Figure 1.7. C8051F966 Block Diagram	26
Figure 1.8. C8051F967 Block Diagram	26
Figure 1.9. C8051F968 Block Diagram	27
Figure 1.10. C8051F969 Block Diagram	27
Figure 1.11. Port I/O Functional Block Diagram	29
Figure 1.12. PCA Block Diagram	30
Figure 1.13. ADC0 Functional Block Diagram	31
Figure 1.14. ADC0 Multiplexer Block Diagram	32
Figure 1.15. Comparator 0 Functional Block Diagram	33
Figure 1.16. Comparator 1 Functional Block Diagram	33
Figure 3.1. DQFN-76 Pinout Diagram (Top View)	43
Figure 3.2. QFN-40 Pinout Diagram (Top View)	44
Figure 3.3. TQFP-80 Pinout Diagram (Top View)	45
Figure 3.4. DQFN-76 Package Drawing	46
Figure 3.5. DQFN-76 Land Pattern	47
Figure 3.6. Recomended Inner Via Placement	49
Figure 3.7. Typical QFN-40 Package Drawing	50
Figure 3.8. QFN-40 Landing Diagram	51
Figure 3.9. TQFP-80 Package Drawing	52
Figure 3.10. TQFP80 Landing Diagram	54
Figure 4.1. Frequency Sensitivity (External CMOS Clock, 25°C)	64
Figure 4.2. Typical VOH Curves, 1.8–3.6 V	66
Figure 4.3. Typical VOL Curves, 1.8–3.6 V	67
Figure 5.1. ADC0 Functional Block Diagram	78
Figure 5.2. 10-Bit ADC Track and Conversion Example Timing	
(BURSTEN = 0)	81
Figure 5.3. Burst Mode Tracking Example with Repeat Count Set to 4	82
Figure 5.4. ADC0 Equivalent Input Circuits	83
Figure 5.5. ADC Window Compare Example: Right-Justified	
Single-Ended Data	94
Figure 5.6. ADC Window Compare Example: Left-Justified	
Single-Ended Data	94
Figure 5.7. ADC0 Multiplexer Block Diagram	95
Figure 5.8. Temperature Sensor Transfer Function	97
Figure 5.9. Temperature Sensor Error with 1-Point Calibration	
(V <sub>REF</sub> = 1.68 V)	98
Figure 5.10. Voltage Reference Functional Block Diagram 1	00



Table 15.5. Three-out-of-Six Decoding	211
Table 16.1. SFR Map (0xC0–0xFF)	222
Table 16.2. SFR Map (0x80–0xBF)	. 223
Table 16.3. Special Function Registers	224
Table 17.1. Interrupt Summary	234
Table 18.1. Flash Security Summary	248
Table 19.1. Power Modes	257
Table 20.1. IPeak Inductor Current Limit Settings	270
Table 23.1. Recommended XFCN Settings for Crystal Mode	288
Table 23.2. Recommended XFCN Settings for RC and C modes	289
Table 24.1. SmaRTClock Internal Registers	296
Table 24.2. SmaRTClock Load Capacitance Settings	302
Table 24.3. SmaRTClock Bias Settings	303
Table 25.1. Pull-Up Resistor Current	315
Table 25.2. Sample Rate Duty-Cycle Multiplier	315
Table 25.3. Pull-Up Duty-Cycle Multiplier	315
Table 25.4. Average Pull-Up Current (Sample Rate = 250 µs)	316
Table 25.5. Average Pull-Up Current (Sample Rate = 500 µs)	316
Table 25.6. Average Pull-Up Current (Sample Rate = 1 ms)	316
Table 25.7. Average Pull-Up Current (Sample Rate = 2 ms)	316
Table 26.1. Bit Configurations to select Contrast Control Modes	338
Table 27.1. Port I/O Assignment for Analog Functions	353
Table 27.2. Port I/O Assignment for Digital Functions	354
Table 27.3. Port I/O Assignment for External Digital Event Capture Functions	354
Table 28.1. SMBus Clock Source Selection	385
Table 28.2. Minimum SDA Setup and Hold Times	386
Table 28.3. Sources for Hardware Changes to SMB0CN	390
Table 28.4. Hardware Address Recognition Examples (EHACK = 1)	391
Table 28.5. SMBus Status Decoding With Hardware ACK Generation Disabled	
(EHACK = 0)	398
Table 28.6. SMBus Status Decoding With Hardware ACK Generation Enabled	
(EHACK = 1)	400
Table 29.1. Timer Settings for Standard Baud Rates	
Using The Internal 24.5 MHz Oscillator	409
Table 29.2. Timer Settings for Standard Baud Rates	
Using an External 22.1184 MHz Oscillator	409
Table 30.1. SPI Slave Timing Parameters	423
Table 31.1. SPI Slave Timing Parameters	443
Table 32.1. Timer 0 Running Modes	446
Table 33.1. PCA Timebase Input Options	467
Table 33.2. PCA0CPM and PCA0PWM Bit Settings for PCA	
Capture/Compare Modules	469
Table 33.3. Watchdog Timer Timeout Intervals1	479
-	



# C8051F96x

SFR Definition 27.24. P3MDIN: Port3 Input Mode	372
SFR Definition 27.25. P3MDOUT: Port3 Output Mode	372
SFR Definition 27.26. P3DRV: Port3 Drive Strength	373
SFR Definition 27.27. P4: Port4	373
SFR Definition 27.28. P4MDIN: Port4 Input Mode	374
SFR Definition 27.29. P4MDOUT: Port4 Output Mode	374
SFR Definition 27.30. P4DRV: Port4 Drive Strength	375
SFR Definition 27.31. P5: Port5	375
SFR Definition 27.32. P5MDIN: Port5 Input Mode	376
SFR Definition 27.33. P5MDOUT: Port5 Output Mode	376
SFR Definition 27.34. P5DRV: Port5 Drive Strength	377
SFR Definition 27.35. P6: Port6	377
SFR Definition 27.36. P6MDIN: Port6 Input Mode	378
SFR Definition 27.37. P6MDOUT: Port6 Output Mode	378
SFR Definition 27.38. P6DRV: Port6 Drive Strength	379
SFR Definition 27.39. P7: Port7	379
SFR Definition 27.40. P7MDOUT: Port7 Output Mode	380
SFR Definition 27.41. P7DRV: Port7 Drive Strength	380
SFR Definition 28.1. SMB0CF: SMBus Clock/Configuration	387
SFR Definition 28.2. SMB0CN: SMBus Control	389
SFR Definition 28.3. SMB0ADR: SMBus Slave Address	391
SFR Definition 28.4. SMB0ADM: SMBus Slave Address Mask	392
SFR Definition 28.5. SMB0DAT: SMBus Data	393
SFR Definition 29.1. SCON0: Serial Port 0 Control	407
SFR Definition 29.2. SBUF0: Serial (UART0) Port Data Buffer	408
SFR Definition 30.1. SPI0CFG: SPI0 Configuration	418
SFR Definition 30.2. SPI0CN: SPI0 Control	419
SFR Definition 30.3. SPI0CKR: SPI0 Clock Rate	420
SFR Definition 30.4. SPI0DAT: SPI0 Data	420
SFR Definition 31.1. SPI1CFG: SPI1 Configuration	438
SFR Definition 31.2. SPI1CN: SPI1 Control	439
SFR Definition 31.3. SPI1CKR: SPI1 Clock Rate	440
SFR Definition 31.4. SPI1DAT: SPI1 Data	440
SFR Definition 32.1. CKCON: Clock Control	445
SFR Definition 32.2. TCON: Timer Control	450
SFR Definition 32.3. TMOD: Timer Mode	451
SFR Definition 32.4. TL0: Timer 0 Low Byte	452
SFR Definition 32.5. TL1: Timer 1 Low Byte	452
SFR Definition 32.6. TH0: Timer 0 High Byte	453
SFR Definition 32.7. TH1: Timer 1 High Byte	453
SFR Definition 32.8. TMR2CN: Timer 2 Control	457
SFR Definition 32.9. TMR2RLL: Timer 2 Reload Register Low Byte	458
SFR Definition 32.10. TMR2RLH: Timer 2 Reload Register High Byte	458
SFR Definition 32.11. TMR2L: Timer 2 Low Byte	459
SFR Definition 32.12. TMR2H Timer 2 High Byte	459



SFR Definition 32.13. TMR3CN: Timer 3 Control463SFR Definition 32.14. TMR3RLL: Timer 3 Reload Register Low Byte464SFR Definition 32.15. TMR3RLH: Timer 3 Reload Register High Byte464SFR Definition 32.16. TMR3L: Timer 3 Low Byte465SFR Definition 32.17. TMR3H Timer 3 High Byte465SFR Definition 33.1. PCA0CN: PCA Control480SFR Definition 33.2. PCA0MD: PCA Mode481SFR Definition 33.3. PCA0PWM: PCA PWM Configuration482SFR Definition 33.4. PCA0CPMn: PCA Capture/Compare Mode483SFR Definition 33.5. PCA0L: PCA Counter/Timer Low Byte484SFR Definition 33.6. PCA0H: PCA Capture Module Low Byte485SFR Definition 33.7. PCA0CPLn: PCA Capture Module Low Byte485C2 Register Definition 34.1. C2ADD: C2 Address486C2 Register Definition 34.3. REVID: C2 Revision ID487C2 Register Definition 34.4. FPCTL: C2 Flash Programming Control488		
SFR Definition 32.14. TMR3RLL: Timer 3 Reload Register Low Byte464SFR Definition 32.15. TMR3RLH: Timer 3 Reload Register High Byte464SFR Definition 32.16. TMR3L: Timer 3 Low Byte465SFR Definition 32.17. TMR3H Timer 3 High Byte465SFR Definition 33.1. PCA0CN: PCA Control480SFR Definition 33.2. PCA0MD: PCA Mode481SFR Definition 33.3. PCA0PWM: PCA PWM Configuration482SFR Definition 33.4. PCA0CPMn: PCA Capture/Compare Mode483SFR Definition 33.5. PCA0L: PCA Counter/Timer Low Byte484SFR Definition 33.6. PCA0H: PCA Counter/Timer High Byte485SFR Definition 33.7. PCA0CPLn: PCA Capture Module Low Byte485SFR Definition 33.8. PCA0CPHn: PCA Capture Module High Byte485C2 Register Definition 34.1. C2ADD: C2 Address486C2 Register Definition 34.3. REVID: C2 Revision ID487C2 Register Definition 34.4. FPCTL: C2 Flash Programming Control488	SFR Definition 32.13. TMR3CN: Timer 3 Control	463
SFR Definition 32.15. TMR3RLH: Timer 3 Reload Register High Byte464SFR Definition 32.16. TMR3L: Timer 3 Low Byte465SFR Definition 32.17. TMR3H Timer 3 High Byte465SFR Definition 33.1. PCA0CN: PCA Control480SFR Definition 33.2. PCA0MD: PCA Mode481SFR Definition 33.3. PCA0PWM: PCA PWM Configuration482SFR Definition 33.4. PCA0CPMn: PCA Capture/Compare Mode483SFR Definition 33.5. PCA0L: PCA Counter/Timer Low Byte484SFR Definition 33.6. PCA0H: PCA Counter/Timer High Byte484SFR Definition 33.7. PCA0CPLn: PCA Capture Module Low Byte485SFR Definition 33.8. PCA0CPHn: PCA Capture Module High Byte485C2 Register Definition 34.1. C2ADD: C2 Address487C2 Register Definition 34.3. REVID: C2 Revision ID487C2 Register Definition 34.4. FPCTL: C2 Flash Programming Control488	SFR Definition 32.14. TMR3RLL: Timer 3 Reload Register Low Byte	464
SFR Definition 32.16. TMR3L: Timer 3 Low Byte465SFR Definition 32.17. TMR3H Timer 3 High Byte465SFR Definition 33.1. PCA0CN: PCA Control480SFR Definition 33.2. PCA0MD: PCA Mode481SFR Definition 33.3. PCA0PWM: PCA PWM Configuration482SFR Definition 33.4. PCA0CPMn: PCA Capture/Compare Mode483SFR Definition 33.5. PCA0L: PCA Counter/Timer Low Byte484SFR Definition 33.6. PCA0H: PCA Counter/Timer High Byte484SFR Definition 33.7. PCA0CPLn: PCA Capture Module Low Byte485SFR Definition 33.8. PCA0CPHn: PCA Capture Module Low Byte485C2 Register Definition 34.1. C2ADD: C2 Address486C2 Register Definition 34.3. REVID: C2 Revision ID487C2 Register Definition 34.4. FPCTL: C2 Flash Programming Control488	SFR Definition 32.15. TMR3RLH: Timer 3 Reload Register High Byte	464
SFR Definition 32.17. TMR3H Timer 3 High Byte465SFR Definition 33.1. PCA0CN: PCA Control480SFR Definition 33.2. PCA0MD: PCA Mode481SFR Definition 33.3. PCA0PWM: PCA PWM Configuration482SFR Definition 33.4. PCA0CPMn: PCA Capture/Compare Mode483SFR Definition 33.5. PCA0L: PCA Counter/Timer Low Byte484SFR Definition 33.6. PCA0H: PCA Counter/Timer High Byte484SFR Definition 33.7. PCA0CPLn: PCA Capture Module Low Byte485SFR Definition 33.8. PCA0CPHn: PCA Capture Module Low Byte485C2 Register Definition 34.1. C2ADD: C2 Address486C2 Register Definition 34.3. REVID: C2 Revision ID487C2 Register Definition 34.4. FPCTL: C2 Flash Programming Control488	SFR Definition 32.16. TMR3L: Timer 3 Low Byte	465
SFR Definition 33.1. PCA0CN: PCA Control480SFR Definition 33.2. PCA0MD: PCA Mode481SFR Definition 33.3. PCA0PWM: PCA PWM Configuration482SFR Definition 33.4. PCA0CPMn: PCA Capture/Compare Mode483SFR Definition 33.5. PCA0L: PCA Counter/Timer Low Byte484SFR Definition 33.6. PCA0H: PCA Counter/Timer High Byte484SFR Definition 33.7. PCA0CPLn: PCA Capture Module Low Byte485SFR Definition 33.8. PCA0CPLn: PCA Capture Module High Byte485C2 Register Definition 34.1. C2ADD: C2 Address486C2 Register Definition 34.2. DEVICEID: C2 Device ID487C2 Register Definition 34.3. REVID: C2 Revision ID487C2 Register Definition 34.4. FPCTL: C2 Flash Programming Control488	SFR Definition 32.17. TMR3H Timer 3 High Byte	465
SFR Definition 33.2. PCA0MD: PCA Mode481SFR Definition 33.3. PCA0PWM: PCA PWM Configuration482SFR Definition 33.4. PCA0CPMn: PCA Capture/Compare Mode483SFR Definition 33.5. PCA0L: PCA Counter/Timer Low Byte484SFR Definition 33.6. PCA0H: PCA Counter/Timer High Byte484SFR Definition 33.7. PCA0CPLn: PCA Capture Module Low Byte485SFR Definition 33.8. PCA0CPLn: PCA Capture Module High Byte485C2 Register Definition 34.1. C2ADD: C2 Address486C2 Register Definition 34.2. DEVICEID: C2 Device ID487C2 Register Definition 34.3. REVID: C2 Revision ID487C2 Register Definition 34.4. FPCTL: C2 Flash Programming Control488	SFR Definition 33.1. PCA0CN: PCA Control	480
SFR Definition 33.3. PCA0PWM: PCA PWM Configuration482SFR Definition 33.4. PCA0CPMn: PCA Capture/Compare Mode483SFR Definition 33.5. PCA0L: PCA Counter/Timer Low Byte484SFR Definition 33.6. PCA0H: PCA Counter/Timer High Byte484SFR Definition 33.7. PCA0CPLn: PCA Capture Module Low Byte485SFR Definition 33.8. PCA0CPHn: PCA Capture Module High Byte485C2 Register Definition 34.1. C2ADD: C2 Address486C2 Register Definition 34.2. DEVICEID: C2 Device ID487C2 Register Definition 34.3. REVID: C2 Revision ID487C2 Register Definition 34.4. FPCTL: C2 Flash Programming Control488	SFR Definition 33.2. PCA0MD: PCA Mode	481
SFR Definition 33.4. PCA0CPMn: PCA Capture/Compare Mode483SFR Definition 33.5. PCA0L: PCA Counter/Timer Low Byte484SFR Definition 33.6. PCA0H: PCA Counter/Timer High Byte484SFR Definition 33.7. PCA0CPLn: PCA Capture Module Low Byte485SFR Definition 33.8. PCA0CPHn: PCA Capture Module High Byte485C2 Register Definition 34.1. C2ADD: C2 Address486C2 Register Definition 34.2. DEVICEID: C2 Device ID487C2 Register Definition 34.3. REVID: C2 Revision ID487C2 Register Definition 34.4. FPCTL: C2 Flash Programming Control488	SFR Definition 33.3. PCA0PWM: PCA PWM Configuration	482
SFR Definition 33.5. PCA0L: PCA Counter/Timer Low Byte484SFR Definition 33.6. PCA0H: PCA Counter/Timer High Byte484SFR Definition 33.7. PCA0CPLn: PCA Capture Module Low Byte485SFR Definition 33.8. PCA0CPHn: PCA Capture Module High Byte485C2 Register Definition 34.1. C2ADD: C2 Address486C2 Register Definition 34.2. DEVICEID: C2 Device ID487C2 Register Definition 34.3. REVID: C2 Revision ID487C2 Register Definition 34.4. FPCTL: C2 Flash Programming Control488	SFR Definition 33.4. PCA0CPMn: PCA Capture/Compare Mode	483
SFR Definition 33.6. PCA0H: PCA Counter/Timer High Byte484SFR Definition 33.7. PCA0CPLn: PCA Capture Module Low Byte485SFR Definition 33.8. PCA0CPHn: PCA Capture Module High Byte485C2 Register Definition 34.1. C2ADD: C2 Address486C2 Register Definition 34.2. DEVICEID: C2 Device ID487C2 Register Definition 34.3. REVID: C2 Revision ID487C2 Register Definition 34.4. FPCTL: C2 Flash Programming Control488	SFR Definition 33.5. PCA0L: PCA Counter/Timer Low Byte	484
SFR Definition 33.7. PCA0CPLn: PCA Capture Module Low Byte485SFR Definition 33.8. PCA0CPHn: PCA Capture Module High Byte485C2 Register Definition 34.1. C2ADD: C2 Address486C2 Register Definition 34.2. DEVICEID: C2 Device ID487C2 Register Definition 34.3. REVID: C2 Revision ID487C2 Register Definition 34.4. FPCTL: C2 Flash Programming Control488	SFR Definition 33.6. PCA0H: PCA Counter/Timer High Byte	484
SFR Definition 33.8. PCA0CPHn: PCA Capture Module High Byte485C2 Register Definition 34.1. C2ADD: C2 Address486C2 Register Definition 34.2. DEVICEID: C2 Device ID487C2 Register Definition 34.3. REVID: C2 Revision ID487C2 Register Definition 34.4. FPCTL: C2 Flash Programming Control488	SFR Definition 33.7. PCA0CPLn: PCA Capture Module Low Byte	485
C2 Register Definition 34.1. C2ADD: C2 Address486C2 Register Definition 34.2. DEVICEID: C2 Device ID487C2 Register Definition 34.3. REVID: C2 Revision ID487C2 Register Definition 34.4. FPCTL: C2 Flash Programming Control488	SFR Definition 33.8. PCA0CPHn: PCA Capture Module High Byte	485
C2 Register Definition 34.2. DEVICEID: C2 Device ID	C2 Register Definition 34.1. C2ADD: C2 Address	486
C2 Register Definition 34.3. REVID: C2 Revision ID	C2 Register Definition 34.2. DEVICEID: C2 Device ID	487
C2 Register Definition 34.4. FPCTL: C2 Flash Programming Control 488	C2 Register Definition 34.3. REVID: C2 Revision ID	487
	C2 Register Definition 34.4. FPCTL: C2 Flash Programming Control	488
C2 Register Definition 34.5. FPDAT: C2 Flash Programming Data	C2 Register Definition 34.5. FPDAT: C2 Flash Programming Data	488



## 4.2. Electrical Characteristics

### **Table 4.2. Global Electrical Characteristics**

-40 to +85 °C, 25 MHz system clock unless otherwise specified.

Parameter	Condition	Min	Тур	Max	Unit		
Supply Voltage (V <sub>BAT</sub> )		1.8		3.8	V		
Minimum RAM Data Retention Voltage <sup>1</sup>		1.4 0.3	— 0.5	V			
SYSCLK (System Clock) <sup>2</sup>		0	—	25	MHz		
T <sub>SYSH</sub> (SYSCLK High Time)		18		_	ns		
T <sub>SYSL</sub> (SYSCLK Low Time)		18	_	—	ns		
Specified Operating Temperature Range	-40	_	+85	°C			
<ul> <li>Notes:</li> <li>1. Based on device characterization data; Not production tested.</li> <li>2. SYSCLK must be at least 32 kHz to enable debugging.</li> </ul>							

### Table 4.3. Digital Supply Current at VBAT pin with DC-DC Converter Enabled

-40 to +85 °C, VBAT = 3.6V, VDC = 1.9 V, 24.5 MHz system clock unless otherwise specified.

Parameter	Parameter Condition							
Digital Supply Current—CPU Active (Normal Mode, fetching instructions from flash, no external load)								
I <sub>BAT</sub> <sup>1,2,3</sup>	V <sub>BAT</sub> = 3.0 V	—	4.1		mA			
	V <sub>BAT</sub> = 3.3 V	—	4.0	_	mA			
	—	3.8	_	mA				
Digital Supply Current—CP	U Inactive (Sleep Mode, sourcing curren	t to ext	ernal d	evice)				
I <sub>BAT</sub> 1	sourcing 9 mA to external device	—	6.5	_	mA			
2,11	sourcing 19 mA to external device	—	13	_	mA			
Notes: 1. Based on device characte	erization data; Not production tested.							

2. Digital Supply Current depends upon the particular code being executed. The values in this table are obtained with the CPU executing a mix of instructions in two loops: djnz R1, \$, followed by a loop that accesses an SFR, and moves data around using the CPU (between accumulator and b-register). The supply current will vary slightly based on the physical location of this code in flash. As described in the Flash Memory chapter, it is best to align the jump addresses with a flash word address (byte location /4), to minimize flash accesses and power consumption.

**3.** Includes oscillator and regulator supply current.



#### 5.2.3. Burst Mode

Burst Mode is a power saving feature that allows ADC0 to remain in a low power state between conversions. When Burst Mode is enabled, ADC0 wakes from a low power state, accumulates 1, 4, 8, 16, 32, or 64 using an internal Burst Mode clock (approximately 20 MHz), then re-enters a low power state. Since the Burst Mode clock is independent of the system clock, ADC0 can perform multiple conversions then enter a low power state within a single system clock cycle, even if the system clock is slow (e.g. 32.768 kHz), or suspended.

Burst Mode is enabled by setting BURSTEN to logic 1. When in Burst Mode, AD0EN controls the ADC0 idle power state (i.e. the state ADC0 enters when not tracking or performing conversions). If AD0EN is set to logic 0, ADC0 is powered down after each burst. If AD0EN is set to logic 1, ADC0 remains enabled after each burst. On each convert start signal, ADC0 is awakened from its Idle Power State. If AD0C0 is powered down, it will automatically power up and wait the programmable Power-Up Time controlled by the AD0PWR bits. Otherwise, ADC0 will start tracking and converting immediately. Figure 5.3 shows an example of Burst Mode Operation with a slow system clock and a repeat count of 4.

When Burst Mode is enabled, a single convert start will initiate a number of conversions equal to the repeat count. When Burst Mode is disabled, a convert start is required to initiate each conversion. In both modes, the ADC0 End of Conversion Interrupt Flag (AD0INT) will be set after "repeat count" conversions have been accumulated. Similarly, the Window Comparator will not compare the result to the greater-than and less-than registers until "repeat count" conversions have been accumulated.

In Burst Mode, tracking is determined by the settings in AD0PWR and AD0TK. The default settings for these registers will work in most applications without modification; however, settling time requirements may need adjustment in some applications. Refer to "5.2.4. Settling Time Requirements" on page 83 for more details.

Notes:

- Setting AD0TM to 1 will insert an additional 3 SAR clocks of tracking before each conversion, regardless of the settings of AD0PWR and AD0TK.
- When using Burst Mode, care must be taken to issue a convert start signal no faster than once every four SYSCLK periods. This includes external convert start signals.







Figure 5.3. Burst Mode Tracking Example with Repeat Count Set to 4



## 5.5. Low Power Mode

The SAR converter provides a low power mode that allows a significant reduction in operating current when operating at low SAR clock frequencies. Low power mode is enabled by setting the AD0LPM bit (ADC0PWR.7) to 1. In general, low power mode is recommended when operating with SAR conversion clock frequency at 4 MHz or less. See the Electrical Characteristics chapter for details on power consumption and the maximum clock frequencies allowed in each mode. Setting the Low Power Mode bit reduces the bias currents in both the SAR converter and in the High-Speed Voltage Reference.

	No	rmal Power I	Mode	Low Power Mode			
	8 bit	10 bit	12 bit	8 bit	10 bit	12 bit	
Highest nominal SAR clock frequency	8.17 MHz (24.5/3)	8.17 MHz (24.5/3)	6.67 MHz (20.0/3)	4.08 MHz (24.5/6)	4.08 MHz (24.5/6)	4.00 MHz (20.0/5)	
Total number of conversion clocks required	11	13	52 (13 x 4)	11	13	52 (13*4)	
Total tracking time (min)	1.5 µs	1.5 µs	4.8 μs (1.5+3 x 1.1)	1.5 µs	1.5 µs	4.8 μs (1.5+3 x 1.1)	
Total time for one conversion2.85		3.09 µs	12.6 µs	4.19 µs	4.68 µs	17.8 µs	
ADC Throughput	351 ksps	323 ksps	79 ksps	238 ksps	214 ksps	56 ksps	
Energy per conversion	8.2 nJ	8.9 nJ	36.5 nJ	6.5 nJ	7.3 nJ	27.7 nJ	

# Table 5.1. Representative Conversion Times and Energy Consumption for the SAR ADC with 1.65 V High-Speed VREF

**Note:** This table assumes that the 24.5 MHz precision oscillator is used for 8- and 10-bit modes, and the 20 MHz low power oscillator is used for 12-bit mode. The values in the table assume that the oscillators run at their nominal frequencies. The maximum SAR clock values given in Table 4.12 allow for maximum oscillation frequencies of 25.0 MHz and 22 MHz for the precision and low-power oscillators, respectively, when using the given SAR clock divider values. Energy calculations are for the ADC subsystem only and do not include CPU current.



## 7.3. Comparator Response Time

Comparator response time may be configured in software via the CPTnMD registers described on "CPT0MD: Comparator 0 Mode Selection" on page 109 and "CPT1MD: Comparator 1 Mode Selection" on page 111. Four response time settings are available: Mode 0 (Fastest Response Time), Mode 1, Mode 2, and Mode 3 (Lowest Power). Selecting a longer response time reduces the Comparator active supply current. The Comparators also have low power shutdown state, which is entered any time the comparator is disabled. Comparator rising edge and falling edge response times are typically not equal. See Table 4.16 on page 74 for complete comparator timing and supply current specifications.

## 7.4. Comparator Hysterisis

The Comparators feature software-programmable hysterisis that can be used to stabilize the comparator output while a transition is occurring on the input. Using the CPTnCN registers, the user can program both the amount of hysteresis voltage (referred to the input voltage) and the positive and negative-going symmetry of this hysteresis around the threshold voltage (i.e., the comparator negative input).

Figure 7.3 shows that when positive hysterisis is enabled, the comparator output does not transition from logic 0 to logic 1 until the comparator positive input voltage has exceeded the threshold voltage by an amount equal to the programmed hysterisis. It also shows that when negative hysterisis is enabled, the comparator output does not transition from logic 1 to logic 0 until the comparator positive input voltage has fallen below the threshold voltage by an amount equal to the programmed hysterisis.

The amount of positive hysterisis is determined by the settings of the CPnHYP bits in the CPTnCN register and the amount of negative hysteresis voltage is determined by the settings of the CPnHYN bits in the same register. Settings of 20 mV, 10 mV, 5 mV, or 0 mV can be programmed for both positive and negative hysterisis. See Section "Table 4.16. Comparator Electrical Characteristics" on page 74 for complete comparator hysterisis specifications.



Figure 7.3. Comparator Hysteresis Plot



# SFR Definition 11.1. DMA0EN: DMA0 Channel Enable

Bit	7	6	5	4	3	2	1	0
Name		CH6_EN	CH5_EN	CH4_EN	CH3_EN	CH2_EN	CH1_EN	CH0_EN
Туре	R	R/W						
Reset	0	0	0	0	0	0	0	0

## SFR Page = 0x2; SFR Address = 0xD2

Bit	Name	Function
7	Unused	Read = 0b, Write = Don't Care
6	CH6_EN	Channel 6 Enable. 0: Disable DMA0 channel 6. 1: Enable DMA0 channel 6.
5	CH5_EN	Channel 5 Enable. 0: Disable DMA0 channel 5. 1: Enable DMA0 channel 5.
4	CH4_EN	Channel 4 Enable. 0: Disable DMA0 channel 4. 1: Enable DMA0 channel 4.
3	CH3_EN	Channel 3 Enable. 0: Disable DMA0 channel 3. 1: Enable DMA0 channel 3.
2	CH2_EN	Channel 2 Enable. 0: Disable DMA0 channel 2. 1: Enable DMA0 channel 2.
1	CH1_EN	Channel 1 Enable. 0: Disable DMA0 channel 1. 1: Enable DMA0 channel 1.
0	CH0_EN	Channel 0 Enable. 0: Disable DMA0 channel 0. 1: Enable DMA0 channel 0.



#### The 16-bit C8051F96x CRC algorithm can be described by the following code:

```
unsigned short UpdateCRC (unsigned short CRC_acc, unsigned char CRC_input)
ł
   unsigned char i;
                                       // loop counter
   #define POLY 0x1021
   // Create the CRC "dividend" for polynomial arithmetic (binary arithmetic
   // with no carries)
   CRC_acc = CRC_acc ^ (CRC_input << 8);</pre>
   // "Divide" the poly into the dividend using CRC XOR subtraction
   // CRC_acc holds the "remainder" of each divide
   11
   // Only complete this division for 8 bits since input is 1 byte
   for (i = 0; i < 8; i++)
   {
      // Check if the MSB is set (if MSB is 1, then the POLY can "divide"
      // into the "dividend")
      if ((CRC_acc & 0x8000) == 0x8000)
      {
         // if so, shift the CRC value, and XOR "subtract" the poly
         CRC_acc = CRC_acc << 1;</pre>
         CRC_acc ^= POLY;
      }
      else
      {
         // if not, just shift the CRC value
         CRC_acc = CRC_acc << 1;
      }
   }
   // Return the final remainder (CRC value)
   return CRC_acc;
}
```

The following table lists several input values and the associated outputs using the 16-bit C8051F96x CRC algorithm:

Input	Output
0x63	0xBD35
0x8C	0xB1F4
0x7D	0x4ECA
0xAA, 0xBB, 0xCC	0x6CF6
0x00, 0x00, 0xAA, 0xBB, 0xCC	0xB166

### Table 12.1. Example 16-bit CRC Outputs



## 14.4. AES Block Cipher Data Flow

The AES0 module data flow for AES Block Cipher encryption and decryption shown in Figure 14.3. The data flow is the same for encryption and decryption. The AES0DCF sfr is always configured to route the AES core output to AES0YOUT. The XOR on the input and output paths are not used.

For an encryption operation, the core is configured for an encryption cipher, the encryption key is written to AES0KIN, the plaintext is written to the AES0BIN sfr. and the ciphertext is read from AES0YOUT.

For a decryption operation, the core is configured for an decryption cipher, the decryption key is written to AES0KIN, the ciphertext is written to the AES0BIN sfr. and the plaintext is read from AES0YOUT.

The key size is set to the desired key size.



Figure 14.3. AES Block Cipher Data Flow



# SFR Definition 17.6. EIP2: Extended Interrupt Priority 2

Bit	7	6	5	4	3	2	1	0
Name	PAES0	PENC0	PDMA0	PPC0	PSPI1	PRTC0F	PMAT	PWARN
Туре	R	R	R	R	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = All Pages; SFR Address = 0xF7

Bit	Name	Function
7	PAES0	AES0 Interrupt Priority Control. This bit sets the priority of the AES0 interrupt. 0: AES0 interrupt set to low priority level. 1: AES0 interrupt set to high priority level.
6	PENC0	Encoder (ENC0) Interrupt Priority Control. This bit sets the priority of the ENC0 interrupt. 0: ENC0 interrupt set to low priority level. 1: SPI0 interrupt set to high priority level.
5	PDMA0	<ul> <li>DMA0 Interrupt Priority Control.</li> <li>This bit sets the priority of the DMA0 interrupt.</li> <li>0: DMA0 interrupt set to low priority level.</li> <li>1: DMA0 interrupt set to high priority level.</li> </ul>
4	PPC0	Pulse Counter (PC0) Interrupt Priority Control.This bit sets the priority of the PC0 interrupt.0: PC0 interrupt set to low priority level.1: PC0 interrupt set to high priority level.
3	PSPI1	<ul> <li>Serial Peripheral Interface (SPI1) Interrupt Priority Control.</li> <li>This bit sets the priority of the SPI0 interrupt.</li> <li>0: SPI1 interrupt set to low priority level.</li> <li>1: SPI1 interrupt set to high priority level.</li> </ul>
2	PRTC0F	<ul> <li>SmaRTClock Oscillator Fail Interrupt Priority Control.</li> <li>This bit sets the priority of the SmaRTClock Alarm interrupt.</li> <li>0: SmaRTClock Alarm interrupt set to low priority level.</li> <li>1: SmaRTClock Alarm interrupt set to high priority level.</li> </ul>
1	PMAT	<ul> <li>Port Match Interrupt Priority Control.</li> <li>This bit sets the priority of the Port Match Event interrupt.</li> <li>0: Port Match interrupt set to low priority level.</li> <li>1: Port Match interrupt set to high priority level.</li> </ul>
0	PWARN	<ul> <li>VDD/DC+ Supply Monitor Early Warning Interrupt Priority Control.</li> <li>This bit sets the priority of the VDD/DC+ Supply Monitor Early Warning interrupt.</li> <li>0: VDD/DC+ Supply Monitor Early Warning interrupt set to low priority level.</li> <li>1: VDD/DC+ Supply Monitor Early Warning interrupt set to high priority level.</li> </ul>



SFR De	finition 19.3.	CLKMODE:	Clock Mode
--------	----------------	----------	------------

Bit	7	6	5	4	3	2	1	0	
Name	Reserved	red Reserved Reserved Re		Reserved	Reserved	LPMEN	Reserved	Reserved	
Туре	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0 0		0	0	0	0	0	

SFR Page = 0xF; SFR Address = 0xFD; Bit-Addressable

Bit	Name	Function
7:3	Reserved	Read = 0b; Write = Must write 00000b.
2	LPMEN	Low Power Mode Enable.
		Setting this bit allows the device to enter Low Power Active or Idle Mode.
1	Reserved	Read = 0b; Must write 0b.
0	Reserved	Read = 0b; Must write 0b.



# SFR Definition 20.1. DC0CN: DC-DC Converter Control

Bit	7	6	5	4	3	2	1	0				
Name	e CLKSEL	CLKD	IV[1:0]	AD0CKINV	CLKINV	SYNC	MINP	W[1:0]				
Туре	e R	R/W	R/W	R/W	R/W	R/W	R/	/W				
Rese	<b>t</b> 0	0	0	0	0	0	1	1				
SFR F	age = 0x0; SF	R Address =	= 0x97									
Bit	Name Function											
7	CLKSEL	DC-DC Co	C-DC Converter Clock Source Select.									
		Specifies th 0: The dc-d 1: The dc-d	Specifies the dc-dc converter clock source. ): The dc-dc converter is clocked from its local oscillator. I: The dc-dc converter is clocked from the system clock.									
6:5	CLKDIV[1:0]	DC-DC Clo	ock Divider.									
		Divides the source for c 00: The dc- 01: The dc- 10: The dc- 11: The dc-	dc-dc conve dc-dc converte dc converte dc converte dc converte dc converte	erter clock wh rter. Ignored a r clock is syst r clock is syst r clock is syst r clock is syst	en the syste II other time em clock div em clock div em clock div em clock div	em clock is s s. vided by 1. vided by 2. vided by 4. vided by 8.	elected as th	ne clock				
4	AD0CKINV	ADC0 Cloc	k Inversior	(Clock Inve	rt During Sy	/nc).						
		Inverts the bit (DC0CN 0: ADC0 SA 1: ADC0 SA	ADC0 SAR I.3) is enable AR clock is in AR clock is r	clock derived ed. This bit is nverted. not inverted.	from the dc- ignored whe	dc converteen the SYNC	r clock wher bit is set to	the SYNC zero.				
3	CLKINV	DC-DC Co	nverter Clo	ck Invert.								
		Inverts the s 0: The dc-d 1: The dc-d	system cloc c converter c converter	k used as the clock is not in clock is invert	input to the verted. ed.	dc-dc clock	divider.					
2	SYNC	ADC0 Synd	chronizatio	n Enable.			-					
		<ul> <li>When synchronization is enabled, the ADC0SC[4:0] bits in the ADC0CF register must be set to 00000b.</li> <li>0: The ADC is not synchronized to the dc-dc converter.</li> <li>1: The ADC is synchronized to the dc-dc converter. ADC0 tracking is performed during the longest quiet time of the dc-dc converter switching cycle and ADC0 SAR clock is also synchronized to the dc-dc converter switching cycle.</li> </ul>										
1:0	MINPW[1:0]	DC-DC Converter Minimum Pulse Width.										
		Specifies th 00: Minimul 01: Minimul 10: Minimul 11: Minimur	DC-DC Converter Minimum Pulse Width. Specifies the minimum pulse width. 00: Minimum pulse detection logic is disabled (no pulse skipping). 01: Minimum pulse width is 10 ns. 10: Minimum pulse width is 20 ns. 11: Minimum pulse width is 40 ns.									



# 21. Voltage Regulator (VREG0)

C8051F96x devices include an internal voltage regulator (VREG0) to regulate the internal core supply to 1.8 V from a VDD/DC+ supply of 1.8 to 3.6 V. Electrical characteristics for the on-chip regulator are specified in the Electrical Specifications chapter.

The REGOCN register allows the Precision Oscillator Bias to be disabled, reducing supply current in all non-sleep power modes. This bias should only be disabled when the precision oscillator is not being used.

The internal regulator (VREG0) is disabled when the device enters sleep mode and remains enabled when the device enters suspend mode. See Section "19. Power Management" on page 257 for complete details about low power modes.

SFR Definition 21.1.	<b>REG0CN: Voltage</b>	<b>Regulator Control</b>
----------------------	------------------------	--------------------------

Bit	7	6	5	4	3	2	1	0
Name				OSCBIAS				
Туре	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	1	0	0	0	0

### SFR Page = 0x0; SFR Address = 0xC9

Bit	Name	Function
7:5	Reserved	Read = 000b. Must Write 000b.
4	OSCBIAS	Precision Oscillator Bias.
		When set to 1, the bias used by the precision oscillator is forced on. If the precision oscillator is not being used, this bit may be cleared to 0 to to save supply current in all non-Sleep power modes.
3:0	Reserved	Read = 0000b. Must Write 0000b.

## 21.1. Voltage Regulator Electrical Specifications

See Table 4.17 on page 75 for detailed Voltage Regulator Electrical Specifications.



# SFR Definition 28.4. SMB0ADM: SMBus Slave Address Mask

Bit	7	6	5	4	3	2	1	0			
Name	SLVM[6:0]										
Туре	R/W										
Reset	1	1	1	1	1	1	1	0			

SFR Page = 0x0; SFR Address = 0xF5

Bit	Name	Function
7:1	SLVM[6:0]	SMBus Slave Address Mask.
		Defines which bits of register SMB0ADR are compared with an incoming address byte, and which bits are ignored. Any bit set to 1 in SLVM[6:0] enables comparisons with the corresponding bit in SLV[6:0]. Bits set to 0 are ignored (can be either 0 or 1 in the incoming address).
0	EHACK	Hardware Acknowledge Enable.
		Enables hardware acknowledgement of slave address and received data bytes. 0: Firmware must manually acknowledge all incoming address and data bytes. 1: Automatic Slave Address Recognition and Hardware Acknowledge is Enabled.



	Valu	es I	Rea	d			Values to Write			us ected
Mode	Status Vector	ACKRQ	ARBLOST	ACK	Current SMbus State	Typical Response Options	STA	STO	ACK	Next Stat Vector Expo
	1110	0	0	х	A master START was gener- ated.	Load slave address + R/W into SMB0DAT.	0	0	х	1100
		_	_	_	A master data or address byte	Set STA to restart transfer.	1	0	Х	1110
smitter		0	0	0	was transmitted; NACK received.	Abort transfer.	0	1	х	-
						Load next data byte into SMB0- DAT.	0	0	х	1100
Trar						End transfer with STOP.	0	1	Х	-
Master <sup>-</sup>	1100	0	0	1	A master data or address byte was transmitted: ACK	End transfer with STOP and start another transfer.	1	1	х	-
		Ŭ			received.	Send repeated START.	1	0	Х	1110
						Switch to Master Receiver Mode (clear SI without writing new data to SMB0DAT). Set ACK for initial data byte.	0	0	1	1000
						Set ACK for next data byte; Read SMB0DAT.	0	0	1	1000
		0	0	1	A master data byte was	Set NACK to indicate next data byte as the last data byte; Read SMB0DAT.	0	0	0	1000
5					Tecelved, ACK Sent.	Initiate repeated START.	1	0	0	1110
er Receive	1000					Switch to Master Transmitter Mode (write to SMB0DAT before clearing SI).	0	0	x	1100
aste						Read SMB0DAT; send STOP.	0	1	0	-
Σ					A master data byte was	Read SMB0DAT; Send STOP followed by START.	1	1	0	1110
		0	0	0	received; NACK sent (last	Initiate repeated START.	1	0	0	1110
					byte).	Switch to Master Transmitter Mode (write to SMB0DAT before clearing SI).	0	0	x	1100

# Table 28.6. SMBus Status Decoding With Hardware ACK Generation Enabled (EHACK = 1)



# C8051F96x

To to initiate a fixed-length SPI Slave mode bidirectional data transfer:

- 1. Configure the SPI1 SFRs normally for Slave mode.
  - a. Enable Slave mode by clearing bit 6 in SPI1CFG.
  - b. Configure the clock polarity CKPOL and clock phase CKPHA as desired in SPI1CFG.
  - c. Configure SPI1CKR for the desired SPI clock rate.
  - d. Configure SPI1CN for 4-wire slave mode.
  - e. Enable the SPI by setting bit 0 of SPI1CN.
- 2. Configure the first DMA channel for the XRAM-to-SPI1DATA transfer:
  - a. Disable the first DMA channel by clearing the corresponding bit in DMA0EN.
  - b. Select the first DMA channel by writing to DMA0SEL.
  - c. Configure the selected DMA channel to use the XRAM-to-SPI1DAT peripheral request by writing 0x03 to DMA0NCF.
  - d. Write 0 to DMA0NMD to disable wrapping.
  - e. Write the address of the first byte of the slave output (MISO) data to DMA0NBAH:L.
  - f. Write the size of the SPI transfer in bytes to DMA0NSZH:L.
  - g. Clear the address offset SFRs DMA0A0H:L.
- 3. Configure the second DMA channel for the SPI1DAT-to-XRAM transfer:
  - a. Disable the second DMA channel by clearing the corresponding bit in DMA0EN.
  - b. Select the second DMA channel by writing to DMA0SEL.
  - c. Configure the selected DMA channel to use the SPI1DAT-to-XRAM peripheral request by writing 0x04 to DMA0NCF.
  - d. Enable DMA interrupts for the second channel by setting bit 7 of DMA0NCF.
  - e. Write 0 to DMA0NMD to disable wrapping.
  - f. Write the address for the first byte of the slave input (MOSI) data to DMA0NBAH:L.
  - g. Write the size of the SPI transfer in bytes to DMA0NSZH:L.
  - h. Clear the address offset SFRs DMA0A0H:L.
  - i. Enable the interrupt on the second channel by setting the corresponding bit in DMA0INT.
  - j. Enable DMA interrupts by setting bit 5 of EIE2.
- 4. Clear the interrupt bits in DMA0INT for both channels.
- 5. Enable both channels by setting the corresponding bits in the DMA0EN SFR to initiate the SPI transfer operation.
- 6. Wait on the DMA interrupt.
- 7. Clear the DMA enables in the DMA0EN SFR.
- 8. Clear the DMA interrupts in the DMA0INT SFR.





Figure 33.2. PCA Counter/Timer Block Diagram

# 33.2. PCA0 Interrupt Sources

Figure 33.3 shows a diagram of the PCA interrupt tree. There are eight independent event flags that can be used to generate a PCA0 interrupt. They are: the main PCA counter overflow flag (CF), which is set upon a 16-bit overflow of the PCA0 counter, an intermediate overflow flag (COVF), which can be set on an overflow from the 8th, 9th, 10th, or 11th bit of the PCA0 counter, and the individual flags for each PCA channel (CCF0, CCF1, CCF2, CCF3, CCF4, and CCF5), which are set according to the operation mode of that module. These event flags are always set when the trigger condition occurs. Each of these flags can be individually selected to generate a PCA0 interrupt, using the corresponding interrupt enable flag (ECF for CF, ECOV for COVF, and ECCFn for each CCFn). PCA0 interrupts must be globally enabled before any individual interrupt sources are recognized by the processor. PCA0 interrupts are globally enabled by setting the EA bit and the EPCA0 bit to logic 1.



# C8051F96x



Figure 33.8. PCA 8-Bit PWM Mode Diagram

### 33.3.5.2. 9/10/11-bit Pulse Width Modulator Mode

The duty cycle of the PWM output signal in 9/10/11-bit PWM mode should be varied by writing to an "Auto-Reload" Register, which is dual-mapped into the PCA0CPHn and PCA0CPLn register locations. The data written to define the duty cycle should be right-justified in the registers. The auto-reload registers are accessed (read or written) when the bit ARSEL in PCA0PWM is set to 1. The capture/compare registers are accessed when ARSEL is set to 0.

When the least-significant N bits of the PCA0 counter match the value in the associated module's capture/compare register (PCA0CPn), the output on CEXn is asserted high. When the counter overflows from the Nth bit, CEXn is asserted low (see Figure 33.9). Upon an overflow from the Nth bit, the COVF flag is set, and the value stored in the module's auto-reload register is loaded into the capture/compare register. The value of N is determined by the CLSEL bits in register PCA0PWM.

The 9, 10 or 11-bit PWM mode is selected by setting the ECOMn and PWMn bits in the PCA0CPMn register, and setting the CLSEL bits in register PCA0PWM to the desired cycle length (other than 8-bits). If the MATn bit is set to 1, the CCFn flag for the module will be set each time a comparator match (rising edge) occurs. The COVF flag in PCA0PWM can be used to detect the overflow (falling edge), which will occur every 512 (9-bit), 1024 (10-bit) or 2048 (11-bit) PCA clock cycles. The duty cycle for 9/10/11-Bit PWM Mode is given in Equation 33.3, where N is the number of bits in the PWM cycle.

**Important Note About PCA0CPHn and PCA0CPLn Registers**: When writing a 16-bit value to the PCA0CPn registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

Duty Cycle = 
$$\frac{(2^N - PCA0CPn)}{2^N}$$

Equation 33.3. 9, 10, and 11-Bit PWM Duty Cycle

A 0% duty cycle may be generated by clearing the ECOMn bit to 0.

