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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, LCD, POR, PWM, WDT
Number of I/O	57
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f966-a-gqr

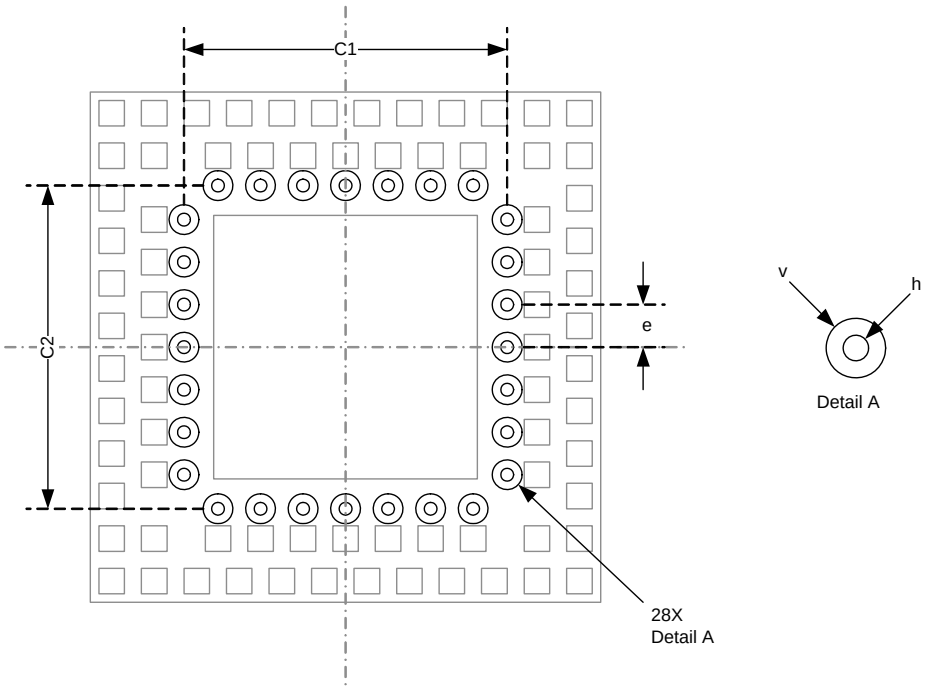


Figure 3.6. Recomended Inner Via Placement

Table 3.4. Recomended Inner Via Placement Dimensions

Dimension	Min	Nominal	Max
C1	—	3.8	—
C2	—	3.8	—
v	—	0.35	—
h	—	0.150	—

Notes:
1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Via hole should be 0.150 mm (6 mil) laser drilled.

Table 4.16. Comparator Electrical Characteristics (Continued)

V_{BAT} = 1.8 to 3.8 V, –40 to +85 °C unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
Hysteresis					
Mode 0					
Hysteresis 1	(CPnHYP/N1–0 = 00)	—	0	—	mV
Hysteresis 2	(CPnHYP/N1–0 = 01)	—	8.5	—	mV
Hysteresis 3	(CPnHYP/N1–0 = 10)	—	17	—	mV
Hysteresis 4	(CPnHYP/N1–0 = 11)	—	34	—	mV
Mode 1					
Hysteresis 1	(CPnHYP/N1–0 = 00)	—	0	—	mV
Hysteresis 2	(CPnHYP/N1–0 = 01)	—	6.5	—	mV
Hysteresis 3	(CPnHYP/N1–0 = 10)	—	13	—	mV
Hysteresis 4	(CPnHYP/N1–0 = 11)	—	26	—	mV
Mode 2					
Hysteresis 1	(CPnHYP/N1–0 = 00)	—	0	1	mV
Hysteresis 2	(CPnHYP/N1–0 = 01)	2	5	10	mV
Hysteresis 3	(CPnHYP/N1–0 = 10)	5	10	20	mV
Hysteresis 4	(CPnHYP/N1–0 = 11)	12	20	30	mV
Mode 3					
Hysteresis 1	(CPnHYP/N1–0 = 00)	—	0	—	mV
Hysteresis 2	(CPnHYP/N1–0 = 01)	—	4.5	—	mV
Hysteresis 3	(CPnHYP/N1–0 = 10)	—	9	—	mV
Hysteresis 4	(CPnHYP/N1–0 = 11)	—	17	—	mV
***Note:** Vcm is the common-mode voltage on CP0+ and CP0–.					

Table 4.17. VREG0 Electrical Characteristics

V_{BAT} = 1.8 to 3.8 V, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Input Voltage Range		1.8	—	3.8	V
Bias Current	Normal, idle, suspend, or stop mode	—	20	—	µA

SFR Definition 5.3. ADC0AC: ADC0 Accumulator Configuration

Bit	7	6	5	4	3	2	1	0
Name	AD012BE	AD0AE	AD0SJST[2:0]			AD0RPT[2:0]		
Type	R/W	W	R/W			R/W		
Reset	0	0	0	0	0	0	0	0

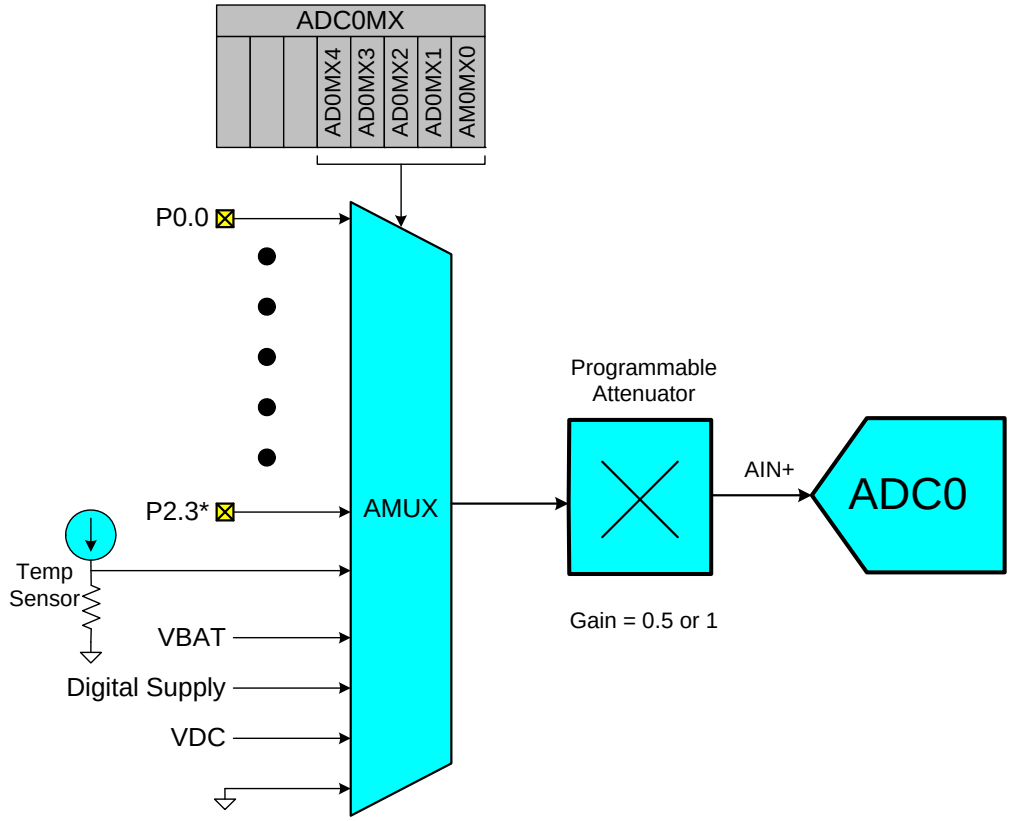
SFR Page = 0x0; SFR Address = 0xBA

Bit	Name	Function
7	AD012BE	**ADC0 12-Bit Mode Enable.** Enables 12-bit Mode. 0: 12-bit Mode Disabled. 1: 12-bit Mode Enabled.
6	AD0AE	**ADC0 Accumulate Enable.** Enables multiple conversions to be accumulated when burst mode is disabled. 0: ADC0H:ADC0L contain the result of the latest conversion when Burst Mode is disabled. 1: ADC0H:ADC0L contain the accumulated conversion results when Burst Mode is disabled. Software must write 0x0000 to ADC0H:ADC0L to clear the accumulated result. This bit is write-only. Always reads 0b.
5:3	AD0SJST[2:0]	**ADC0 Accumulator Shift and Justify.** Specifies the format of data read from ADC0H:ADC0L. 000: Right justified. No shifting applied. 001: Right justified. Shifted right by 1 bit. 010: Right justified. Shifted right by 2 bits. 011: Right justified. Shifted right by 3 bits. 100: Left justified. No shifting applied. All remaining bit combinations are reserved.
2:0	AD0RPT[2:0]	**ADC0 Repeat Count.** Selects the number of conversions to perform and accumulate in Burst Mode. This bit field must be set to 000 if Burst Mode is disabled. 000: Perform and Accumulate 1 conversion. 001: Perform and Accumulate 4 conversions. 010: Perform and Accumulate 8 conversions. 011: Perform and Accumulate 16 conversions. 100: Perform and Accumulate 32 conversions. 101: Perform and Accumulate 64 conversions. All remaining bit combinations are reserved.

5.7. ADC0 Analog Multiplexer

ADC0 on C8051F96x has an analog multiplexer, referred to as AMUX0.

AMUX0 selects the positive inputs to the single-ended ADC0. Any of the following may be selected as the positive input: Port I/O pins, the on-chip temperature sensor, the VBAT Power Supply, Regulated Digital Supply Voltage (Output of VREG0), VDC Supply, or the positive input may be connected to GND. The ADC0 input channels are selected in the ADC0MX register described in SFR Definition 5.12.



*P1.0 – P1.3 are not available as analog inputs

Figure 5.7. ADC0 Multiplexer Block Diagram

Important Note About ADC0 Input Configuration: Port pins selected as ADC0 inputs should be configured as analog inputs, and should be skipped by the Digital Crossbar. To configure a Port pin for analog input, set to 0 the corresponding bit in register PnMDIN and disable the digital driver (PnMDOUT = 0 and Port Latch = 1). To force the Crossbar to skip a Port pin, set to 1 the corresponding bit in register PnSKIP. See Section “27. Port Input/Output” on page 351 for more Port I/O configuration details.

SFR Definition 6.2. IREF0CF: Current Reference Configuration

Bit	7	6	5	4	3	2	1	0
Name	PWMEN					PWMSS[2:0]		
Type	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0	0	0

SFR Page = 0xF; SFR Address = 0xB9

Bit	Name	Function
7	PWMEN	**PWM Enhanced Mode Enable.** Enables the PWM Enhanced Mode. 0: PWM Enhanced Mode disabled. 1: PWM Enhanced Mode enabled.
6:3	Unused	Read = 0000b, Write = don't care.
2:0	PWMSS[2:0]	**PWM Source Select.** Selects the PCA channel to use for the fine-tuning control signal. 000: CEX0 selected as fine-tuning control signal. 001: CEX1 selected as fine-tuning control signal. 010: CEX2 selected as fine-tuning control signal. 011: CEX3 selected as fine-tuning control signal. 100: CEX4 selected as fine-tuning control signal. 101: CEX5 selected as fine tuning control signal. All Other Values: Reserved.

6.2. IREF0 Specifications

See Table 4.15 on page 73 for a detailed listing of IREF0 specifications.

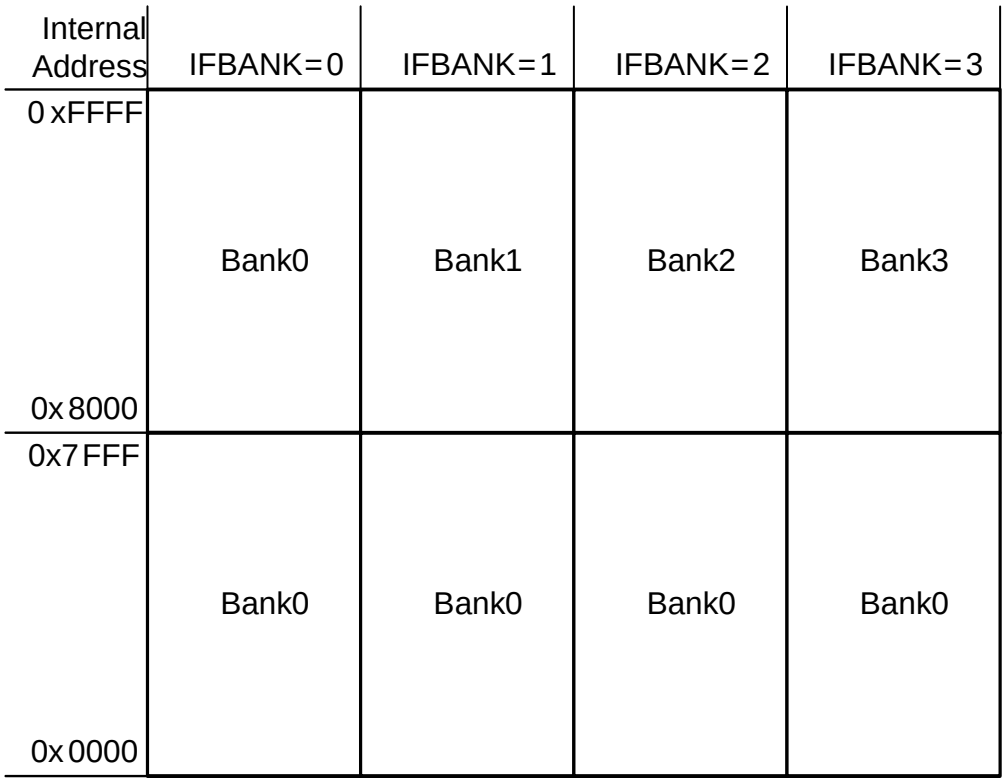


Figure 9.3. Address Memory Map for Instruction Fetches

SFR Definition 11.8. DMA0NBAH: Memory Base Address High Byte

Bit	7	6	5	4	3	2	1	0
Name					NBAH[3:0]			
Type	R	R	R	R	R/W			
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x2; SFR Address = 0xCB

Bit	Name	Function
7:4	Unused	Read = 0b, Write = Don't Care
3:0	NBAH[3:0]	**Memory Base Address High Byte.** Sets high byte of the memory base address which is the DMA0 XRAM starting address of the selected channel if the channel's address offset DMA0NAO is reset to 0.
Note: This sfr is a DMA channel indirect register. Select the desired channel first using the DMA0SEL sfr.		

SFR Definition 11.9. DMA0NBAL: Memory Base Address Low Byte

Bit	7	6	5	4	3	2	1	0
Name	NBAL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x2; SFR Address = 0xCA

Bit	Name	Function
7:0	NBAL[7:0]	**Memory Base Address Low Byte.** Sets low byte of the memory base address which is the DMA0 XRAM starting address of the selected channel if the channel's address offset DMA0NAO is reset to 0.
Note: This sfr is a DMA channel indirect register. Select the desired channel first using the DMA0SEL sfr.		

SFR Definition 12.4. CRC0AUTO: CRC0 Automatic Control

Bit	7	6	5	4	3	2	1	0
Name	AUTOEN	CRCDONE	CRC0ST[5:0]					
Type	R/W							R/W
Reset	0	1	0	0	0	0	0	0

SFR Page = 0xF; SFR Address = 0x96

Bit	Name	Function
7	AUTOEN	**Automatic CRC Calculation Enable.** When AUTOEN is set to 1, any write to CRC0CN will initiate an automatic CRC starting at flash sector CRC0ST and continuing for CRC0CNT sectors.
6	CRCDONE	**CRCDONE Automatic CRC Calculation Complete.** Set to 0 when a CRC calculation is in progress. Note that code execution is stopped during a CRC calculation, therefore reads from firmware will always return 1.
5:0	CRC0ST[5:0]	**Automatic CRC Calculation Starting Flash Sector.** These bits specify the flash sector to start the automatic CRC calculation. The starting address of the first flash sector included in the automatic CRC calculation is CRC0ST x 1024. For 128 kB devices, pages 32–63 access the upper code bank as selected by the IFBANK bits in the PSBANK SFR.

SFR Definition 12.5. CRC0CNT: CRC0 Automatic Flash Sector Count

Bit	7	6	5	4	3	2	1	0
Name			CRC0CNT[5:0]					
Type	R/W							R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = 0xF; SFR Address = 0x97

Bit	Name	Function
7:6	Unused	Read = 00b; Write = Don’t Care.
5:0	CRC0CNT[5:0]	**Automatic CRC Calculation Flash Sector Count.** These bits specify the number of flash sectors to include in an automatic CRC calculation. The starting address of the last flash sector included in the automatic CRC calculation is (CRC0ST+CRC0CNT) x 1024. The last page should not exceed page 63. Setting both CRC0ST and CRC0CNT to 0 will perform a CRC over the 64kB banked memory space.

13. DMA-Enabled Cyclic Redundancy Check Module (CRC1)

C8051F96x devices include a DMA-enabled cyclic redundancy check module (CRC1) that can perform a CRC of data using an arbitrary 16-bit polynomial. This peripheral can compute CRC results using direct DMA access to data in XRAM.

Using a DMA transfer provides much higher data throughput than using SFR access. Since the CPU can be in Idle mode while the CRC is calculated, CRC1 also provides substantial power savings. The CRC1 module is not restricted to a limited list of fixed polynomials. Instead, the user can specify any valid 16-bit polynomial.

CRC1 accepts a stream of 8-bit data written to the CRC1IN register. A DMA transfer can be used to autonomously transfer data from XRAM to the CRC1IN SFR. The CRC1 module may also be used with SFR access by writing directly to the CRC1IN SFR. After each byte is written, the CRC resultant is updated on the CRC1OUTH:L SFRs. After writing all data bytes, the final CRC results are available from the CRC1OUTH:L registers. The final results may be flipped or inverted using the FLIP and INV bits in the CRC1CN SFR. The initial seed value can be reset to 0x0000 or seeded with 0xFFFF.

13.1. Polynomial Specification

The arbitrary polynomial should be written to the CRC1POLH:L SFRs before writing data to the CRCIN SFR.

A valid 16-bit CRC polynomial must have an x^{16} term and an x^0 term. Theoretically, a 16-bit polynomial might have 17 terms total. However, the polynomial SFR is only 16-bits wide. The convention used is to omit the x^{16} term. The polynomial should be written in big endian bit order. The most significant bit corresponds to the highest order term. Thus, the most significant bit in the CRC1POLH SFR represents the x^{15} term, and the least significant bit in the CRC1POLL SFR represents the x^0 term. The least significant bit of CRC1POLL should always be set to one. The CRC results are undefined if this bit is cleared to a zero.

Figure 13.1 depicts the polynomial representation for the CRC-16-CCIT polynomial $x^{16} + x^{12} + x^5 + 1$, or 0x1021.

CRC1POLH:L = 0x1021

	CRC1POLH								CRC1POLL							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	1
	↓			↓							↓					↓
	$x^{16}+$			$x^{12}+$							x^5+					1

Figure 13.1. Polynomial Representation

14.6.5.1. CTR Data Flow

The AES0 module data flow for CTR encryption and decryption shown in Figure 14.5. The data flow is the same for encryption and decryption. The AES0DCF sfr is always configured to XOR AES0XIN with the AES Core output.The XOR on the input is not used. The AES core is configured for an encryption operation. The encryption key is written to AES0KIN. The key size is set to the desired key size.

For an encryption operation, the plaintext is written to the AES0BIN sfr and the ciphertext is read from AES0YOUT. For decryption, the ciphertext is written to AES0BIN and the plaintext is read from AES0YOUT.

Note the counter must be incremented after each block using software.

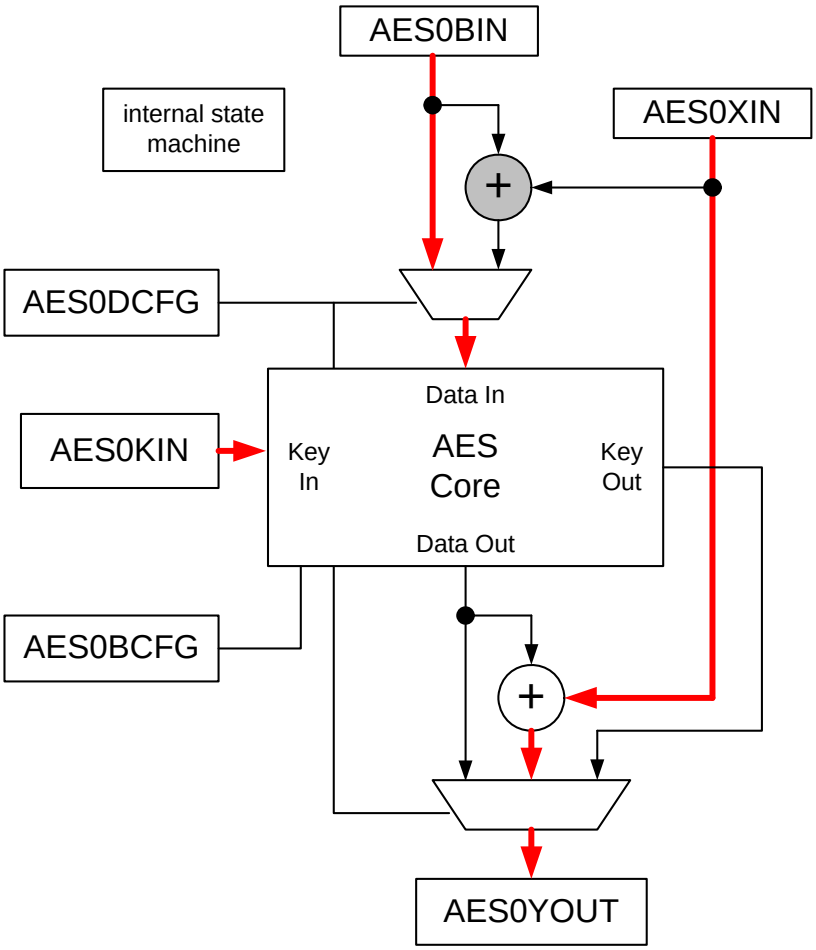


Figure 14.8. Counter Mode Data Flow

17.3. Interrupt Priorities

Each interrupt source can be individually programmed to one of two priority levels: low or high. A low priority interrupt service routine can be preempted by a high priority interrupt. A high priority interrupt cannot be preempted. If a high priority interrupt preempts a low priority interrupt, the low priority interrupt will finish execution after the high priority interrupt completes. Each interrupt has an associated interrupt priority bit in in the Interrupt Priority and Extended Interrupt Priority registers used to configure its priority level. Low priority is the default.

If two interrupts are recognized simultaneously, the interrupt with the higher priority is serviced first. If both interrupts have the same priority level, a fixed priority order is used to arbitrate. See Table 17.1 on page 234 to determine the fixed priority order used to arbitrate between simultaneously recognized interrupts.

17.4. Interrupt Latency

Interrupt response time depends on the state of the CPU when the interrupt occurs. Pending interrupts are sampled and priority decoded each system clock cycle. Therefore, the fastest possible response time is 7 system clock cycles: 1 clock cycle to detect the interrupt, 1 clock cycle to execute a single instruction, and 5 clock cycles to complete the LCALL to the ISR. If an interrupt is pending when a RETI is executed, a single instruction is executed before an LCALL is made to service the pending interrupt. Therefore, the maximum response time for an interrupt (when no other interrupt is currently being serviced or the new interrupt is of greater priority) occurs when the CPU is performing an RETI instruction followed by a DIV as the next instruction. In this case, the response time is 19 system clock cycles: 1 clock cycle to detect the interrupt, 5 clock cycles to execute the RETI, 8 clock cycles to complete the DIV instruction and 5 clock cycles to execute the LCALL to the ISR. If the CPU is executing an ISR for an interrupt with equal or higher priority, the new interrupt will not be serviced until the current ISR completes, including the RETI and following instruction.

SFR Definition 18.4. FLKEY: Flash Lock and Key

Bit	7	6	5	4	3	2	1	0
Name	FLKEY[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xB6

Bit	Name	Function
7:0	FLKEY[7:0]	**Flash Lock and Key Register.** Write: This register provides a lock and key function for flash erasures and writes. Flash writes and erases are enabled by writing 0xA5 followed by 0xF1 to the FLKEY register. Flash writes and erases are automatically disabled after the next write or erase is complete. If any writes to FLKEY are performed incorrectly, or if a flash write or erase operation is attempted while these operations are disabled, the flash will be permanently locked from writes or erasures until the next device reset. If an application never writes to flash, it can intentionally lock the flash by writing a non-0xA5 value to FLKEY from software. Read: When read, bits 1–0 indicate the current flash lock state. 00: Flash is write/erase locked. 01: The first key code has been written (0xA5). 10: Flash is unlocked (writes/erases allowed). 11: Flash writes/erases disabled until the next reset.

25.10.2. Flutter Detection

The flutter detection can be used with either quadrature counter mode or dual counter mode when the two inputs are expected to be in step. Flutter refers to the case where one input continues toggling while the other input stops toggling. This may indicate a broken reed switch or a pressure oscillation when the wheel magnet stops at just the right distance from the reed switch. If a pressure oscillation causes a slight rotational oscillation in the wheel, it could cause a number of pulses on one of the inputs, but not on the other. All four edges are checked by the flutter detection feature (PC1 positive, PC1 negative, PC0 positive, and PC0 negative).When enabled, Flutter detection may be used as an interrupt or wake-up source.

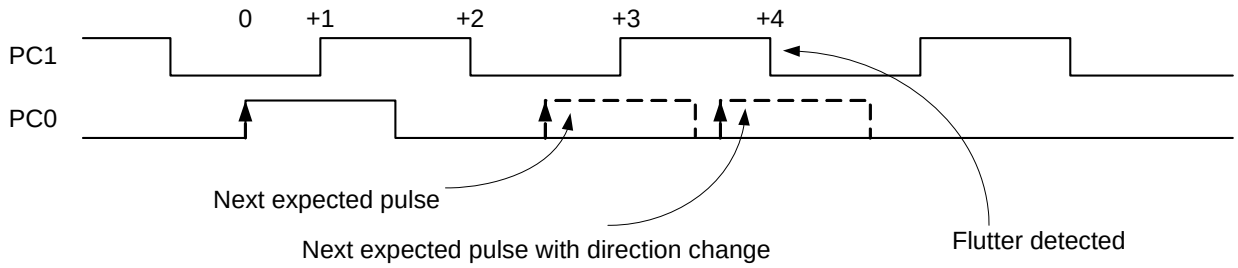


Figure 25.5. Flutter Example

For example, flutter detected on the PC0 positive edge means that 4 edges (positive or negative) were detected on PC1 since the last PC0 positive edge. Each PC0 positive edge resets the flutter detection counter while either PC1 edge increments the counter. There are similar counters for all four edges.

The flutter detection circuit provides interrupts or wake-up sources, but firmware must also read the Pulse Counter registers to determine what corrective action, if any, must be taken.

On the start of flutter event, the firmware should save both counter values and the PC0HIST register. Once the end of flutter event occurs the firmware should also save both counter values and the PC0HIST register. The stop count on flutter, STPCNTFLTR (PCMD[2]), be used to stop the counters when flutter is occurring (quadrature mode only). For quadrature mode, the opposite counter should be decremented by one. In other words, if the direction was clock-wise, the counter clock-wise counter (counter 1) should be decremented by one to correct for one increment before flutter was detected. For dual mode, two reed switches can be used to get a redundant count. If flutter starts during dual mode, both counters should be saved by firmware. After flutter stops, both counters should be read again. The counter that incremented the most was the one that picked up the flutter. There is also a mode to switch from quadrature to dual (PC0MD[1]) when flutter occurs. This changes the counter style from quadrature (count on any edge of PC1 or PC0) to dual to allow all counts to be recorded. Once flutter ends, this mode switches the counters back to quadrature mode. STPCNTFLTR does not function when PC0MD[1] is set.

SFR Definition 25.4. PC0STAT: PC0 Status

Bit	7	6	5	4	3	2	1	0
Name	FLUTTER	DIRECTION	STATE[1:0]		PC1PREV	PC0PREV	PC1	PC0
Type	RO	RO	RO		RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0

SFR Address = 0xC1; SFR Page = 0x2

Bit	Name	Function
7	FLUTTER	**Flutter** During quadrature mode, a disparity may occur between the number of negative edges of PC1 and PC0 or the number of positive edges of PC1 and PC0. This could indicate flutter on one reed switch or one reed switch may be faulty. 0: No flutter detected. 1: Flutter detected.
6	DIRECTION	**Direction** Only applicable for quadrature mode. (First letter is PC1; second letter is PC0) 0: Counter clock-wise - (LL-LH-HH-HL) 1: Clock-wise - (LL-HL-HH-LH)
5:4	STATE[1:0]	**PC0 State** Current State of Internal State Machine.
3	PC1PREV	**PC1 Previous** Previous Output of PC1 Integrator.
2	PC0PREV	**PC0 Previous** Previous Output of PC0 Integrator.
1	PC1	**PC1** Current Output of PC1 Integrator.
0	PC0	**PC0** Current Output of PC0 Integrator.

SFR Definition 26.4. LCD0MSCN: LCD0 Master Control

Bit	7	6	5	4	3	2	1	0
Name		BIASEN	DCBIASOE	CLKOE		LOWDRV	LCDRST	LCDEN
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	1	0	0	0	0	0

SFR Page = 0x2; SFR Address = 0xAB

Bit	Name	Function
7	Reserved	Read = 0b. Must write 0b.
6	BIASEN	**LCD0 Bias Enable.** LCD0 bias may be disabled when using a static LCD (single backplane), contrast control mode 1 (Bypass Mode) is selected, and the VLCD/VIO Supply Comparator is disabled (LCD0CF.5 = 1). It is required for all other modes. 0: LCD0 Bias is disabled. 1: LCD0 Bias is enabled
5	DCBIASOE	**DCDC Converter Bias Output Enable. (Note 1)** 0: The bias for the DCDC converter is gated off. 1: LCD0 provides the bias for the DCDC converter.
4	CLKOE	**LCD Clock Output Enable.** 0: The clock signal to the LCD0 module is gated off. 1: The SmaRTClock provides the undivided clock to the LCD0 Module.
3	Reserved	Read = 0b. Must write 0b.
2	LOWDRV	**Charge Pump Reduced Drive Mode.** This bit should be set to 1 in Contrast Control Mode 3 and Mode 4 for minimum power consumption. This bit may be set to 0 in these modes to support higher load current requirements. 0: The charge pump operates at full power. 1: The charge pump operates at reduced power.
1	LCDRST	**LCD0 Reset.** Writing a 1 to this bit will clear all the LCD0Dn registers to 0x00. This bit must be cleared by software.
0	LCDEN	**LCD0 Enable.** 0: LCD0 is disabled. 1: LCD0 is enabled.
Note 1: To same bias generator is shared by the DCDC Converter and LCD0.		

27. Port Input/Output

Digital and analog resources are available through 57 I/O pins (C8051F960/2/4/6/8) or 34 I/O pins (C8051F961/3/5/7/9). Port pins are organized as eight byte-wide ports. Port pins can be defined as digital or analog I/O. Digital I/O pins can be assigned to one of the internal digital resources or used as general purpose I/O (GPIO). Analog I/O pins are used by the internal analog resources. P7.0 can be used as GPIO and is shared with the C2 Interface Data signal (C2D). See Section “34. C2 Interface” on page 486 for more details.

The designer has complete control over which digital and analog functions are assigned to individual port pins. This resource assignment flexibility is achieved through the use of a Priority Crossbar Decoder. See Section 27.3 for more information on the Crossbar.

For Port I/Os configured as push-pull outputs, current is sourced from the VIO or VIORF supply pin. On 40-pin devices, the VIO and VIORF supply pins are internally tied to VBAT. See Section 27.1 for more information on Port I/O operating modes and the electrical specifications chapter for detailed electrical specifications.

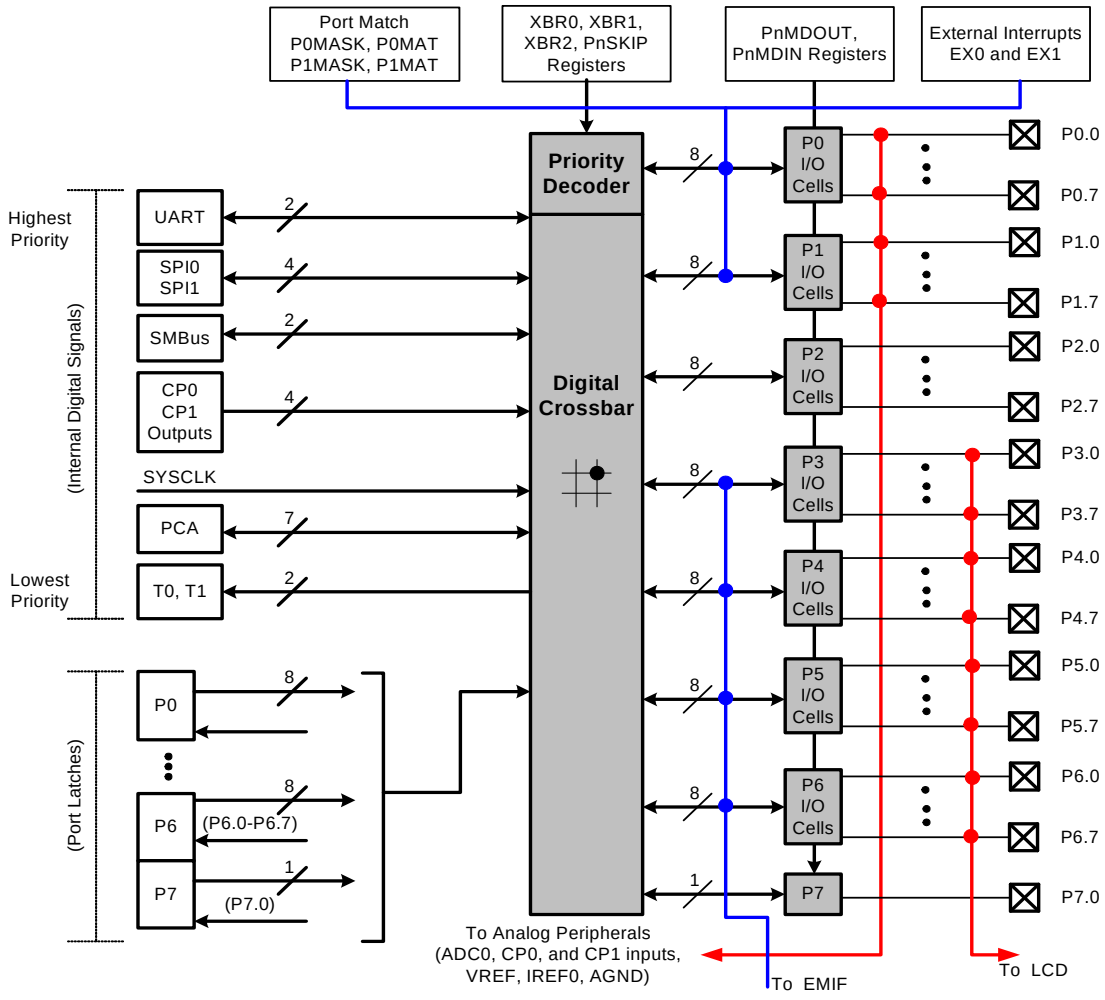


Figure 27.1. Port I/O Functional Block Diagram

SFR Definition 27.12. P0DRV: Port0 Drive Strength

Bit	7	6	5	4	3	2	1	0
Name	P0DRV[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0xF; SFR Address = 0xA4

Bit	Name	Function
7:0	P0DRV[7:0]	**Drive Strength Configuration Bits for P0.7–P0.0 (respectively).** Configures digital I/O Port cells to high or low output drive strength. 0: Corresponding P0.n Output has low output drive strength. 1: Corresponding P0.n Output has high output drive strength.

SFR Definition 27.13. P1: Port1

Bit	7	6	5	4	3	2	1	0
Name	P1[7:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

SFR Page = All Pages; SFR Address = 0x90; Bit-Addressable

Bit	Name	Description	Write	Read
7:0	P1[7:0]	**Port 1 Data.** Sets the Port latch logic value or reads the Port pin logic state in Port cells configured for digital I/O.	0: Set output latch to logic LOW. 1: Set output latch to logic HIGH.	0: P1.n Port pin is logic LOW. 1: P1.n Port pin is logic HIGH.

SFR Definition 28.2. SMB0CN: SMBus Control

Bit	7	6	5	4	3	2	1	0
Name	MASTER	TXMODE	STA	STO	ACKRQ	ARBLOST	ACK	SI
Type	R	R	R/W	R/W	R	R	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xC0; Bit-Addressable

Bit	Name	Description	Read	Write
7	MASTER	**SMBus Master/Slave Indicator.** This read-only bit indicates when the SMBus is operating as a master.	0: SMBus operating in slave mode. 1: SMBus operating in master mode.	N/A
6	TXMODE	**SMBus Transmit Mode Indicator.** This read-only bit indicates when the SMBus is operating as a transmitter.	0: SMBus in Receiver Mode. 1: SMBus in Transmitter Mode.	N/A
5	STA	**SMBus Start Flag.**	0: No Start or repeated Start detected. 1: Start or repeated Start detected.	0: No Start generated. 1: When Configured as a Master, initiates a START or repeated START.
4	STO	**SMBus Stop Flag.**	0: No Stop condition detected. 1: Stop condition detected (if in Slave Mode) or pending (if in Master Mode).	0: No STOP condition is transmitted. 1: When configured as a Master, causes a STOP condition to be transmitted after the next ACK cycle. Cleared by Hardware.
3	ACKRQ	**SMBus Acknowledge Request.**	0: No Ack requested 1: ACK requested	N/A
2	ARBLOST	**SMBus Arbitration Lost Indicator.**	0: No arbitration error. 1: Arbitration Lost	N/A
1	ACK	**SMBus Acknowledge.**	0: NACK received. 1: ACK received.	0: Send NACK 1: Send ACK
0	SI	**SMBus Interrupt Flag.** This bit is set by hardware under the conditions listed in Table 15.3. SI must be cleared by software. While SI is set, SCL is held low and the SMBus is stalled.	**0: No interrupt pending** 1: Interrupt Pending	0: Clear interrupt, and initiate next state machine event. 1: Force interrupt.

32. Timers

Each MCU includes four counter/timers: two are 16-bit counter/timers compatible with those found in the standard 8051, and two are 16-bit auto-reload timer for use with the ADC, SMBus, or for general purpose use. These timers can be used to measure time intervals, count external events and generate periodic interrupt requests. Timer 0 and Timer 1 are nearly identical and have four primary modes of operation. Timer 2 and Timer 3 offer 16-bit and split 8-bit timer functionality with auto-reload. Additionally, Timer 2 and Timer 3 have a Capture Mode that can be used to measure the SmaRTClock, Comparator, or external clock period with respect to another oscillator. The ability to measure the Comparator period with respect to another oscillator is particularly useful when interfacing to capacitive sensors.

Timer 0 and Timer 1 Modes:	Timer 2 Modes:	Timer 3 Modes:
13-bit counter/timer	16-bit timer with auto-reload	16-bit timer with auto-reload
16-bit counter/timer		
8-bit counter/timer with auto-reload	Two 8-bit timers with auto-reload	Two 8-bit timers with auto-reload
Two 8-bit counter/timers (Timer 0 only)		

Timers 0 and 1 may be clocked by one of five sources, determined by the Timer Mode Select bits (T1M–T0M) and the Clock Scale bits (SCA1–SCA0). The Clock Scale bits define a pre-scaled clock from which Timer 0 and/or Timer 1 may be clocked (See SFR Definition 32.1 for pre-scaled clock selection).

Timer 0/1 may then be configured to use this pre-scaled clock signal or the system clock. Timer 2 and Timer 3 may be clocked by the system clock, the system clock divided by 12. Timer 2 may additionally be clocked by the SmaRTClock divided by 8 or the Comparator0 output. Timer 3 may additionally be clocked by the external oscillator clock source divided by 8 or the Comparator1 output.

Timer 0 and Timer 1 may also be operated as counters. When functioning as a counter, a counter/timer register is incremented on each high-to-low transition at the selected input pin (T0 or T1). Events with a frequency of up to one-fourth the system clock frequency can be counted. The input signal need not be periodic, but it should be held at a given level for at least two full system clock cycles to ensure the level is properly sampled.

33. Programmable Counter Array

The Programmable Counter Array (PCA0) provides enhanced timer functionality while requiring less CPU intervention than the standard 8051 counter/timers. The PCA consists of a dedicated 16-bit counter/timer and six 16-bit capture/compare modules. Each capture/compare module has its own associated I/O line (CEXn) which is routed through the Crossbar to Port I/O when enabled. The counter/timer is driven by a programmable timebase that can select between seven sources: system clock, system clock divided by four, system clock divided by twelve, the external oscillator clock source divided by 8, SmaRTClock divided by 8, Timer 0 overflows, or an external clock signal on the ECI input pin. Each capture/compare module may be configured to operate independently in one of six modes: Edge-Triggered Capture, Software Timer, High-Speed Output, Frequency Output, 8 to 11-Bit PWM, or 16-Bit PWM (each mode is described in Section “33.3. Capture/Compare Modules” on page 469). The external oscillator clock option is ideal for real-time clock (RTC) functionality, allowing the PCA to be clocked by a precision external oscillator while the internal oscillator drives the system clock. The PCA is configured and controlled through the system controller's Special Function Registers. The PCA block diagram is shown in Figure 33.1

Important Note: The PCA Module 5 may be used as a watchdog timer (WDT), and is enabled in this mode following a system reset. **Access to certain PCA registers is restricted while WDT mode is enabled**. See Section 33.4 for details.

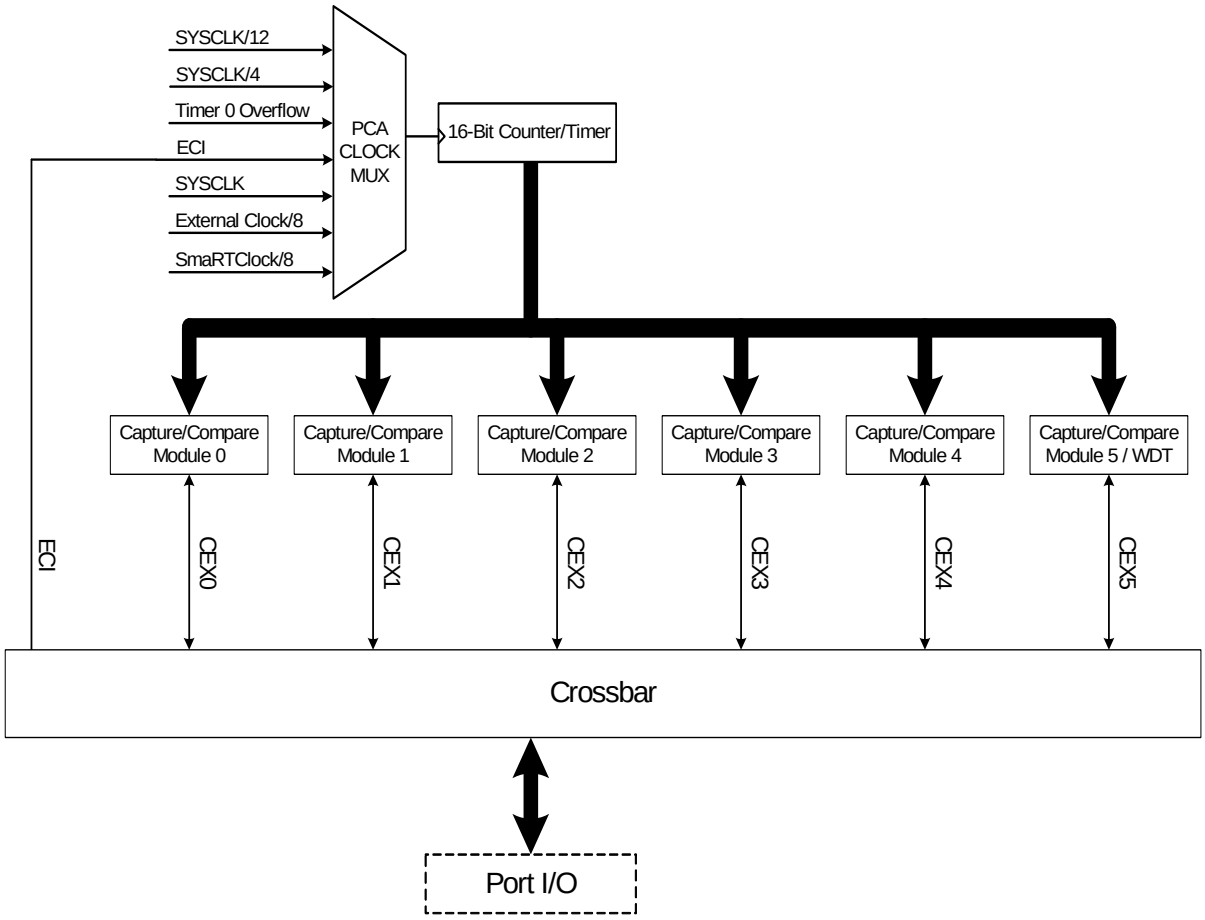


Figure 33.1. PCA Block Diagram