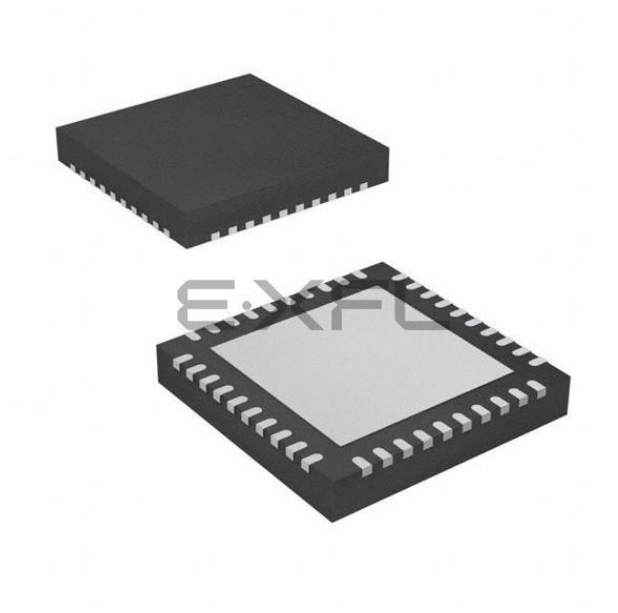

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, LCD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f967-b-gmr

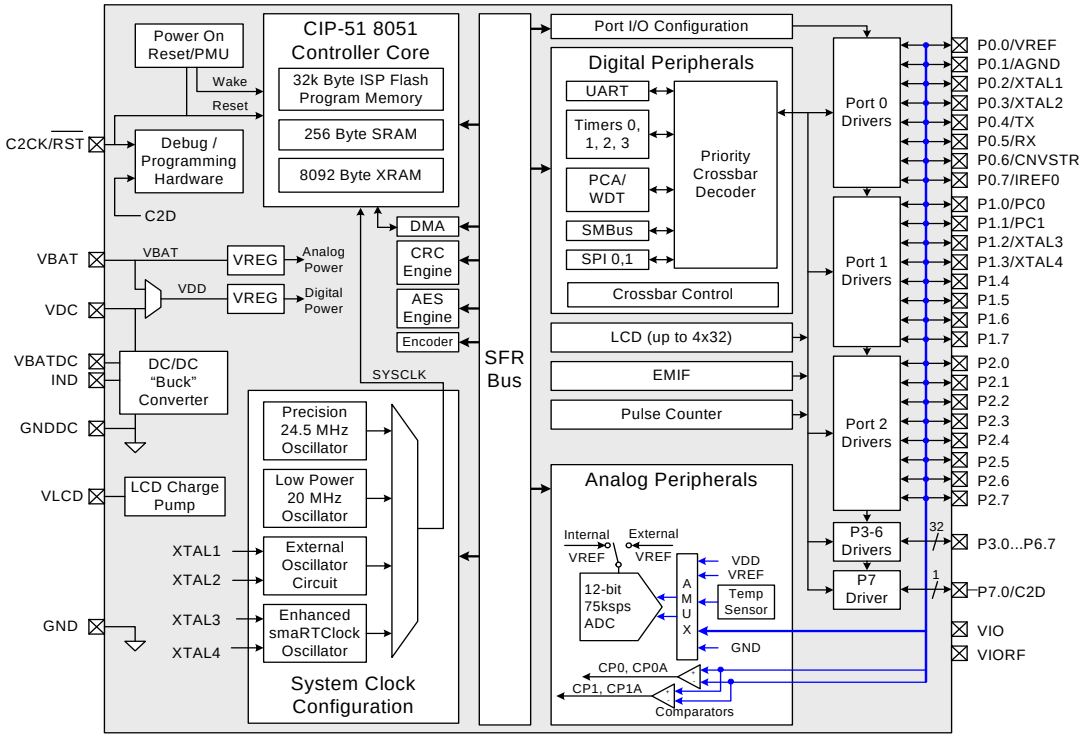


Figure 1.7. C8051F966 Block Diagram

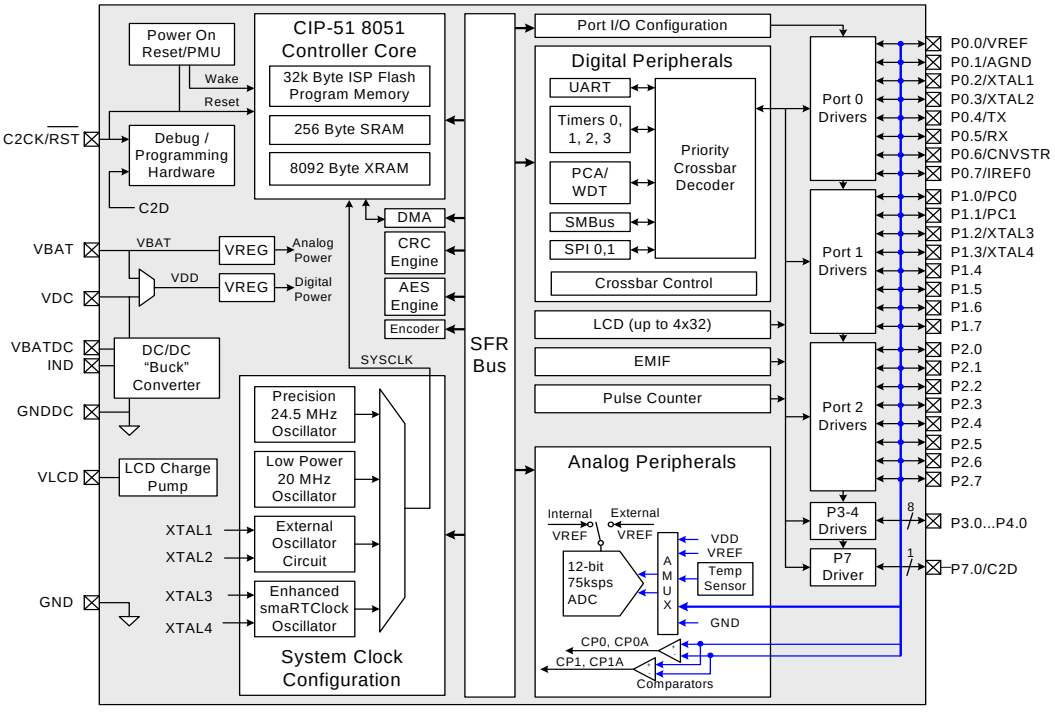


Figure 1.8. C8051F967 Block Diagram

1.1. CIP-51™ Microcontroller Core

1.1.1. Fully 8051 Compatible

The C8051F96x family utilizes Silicon Labs' proprietary CIP-51 microcontroller core. The CIP-51 is fully compatible with the MCS-51™ instruction set; standard 803x/805x assemblers and compilers can be used to develop software. The CIP-51 core offers all the peripherals included with a standard 8052.

1.1.2. Improved Throughput

The CIP-51 employs a pipelined architecture that greatly increases its instruction throughput over the standard 8051 architecture. In a standard 8051, all instructions except for MUL and DIV take 12 or 24 system clock cycles to execute with a maximum system clock of 12–24 MHz. By contrast, the CIP-51 core executes 70% of its instructions in one or two system clock cycles, with only four instructions taking more than four system clock cycles.

The CIP-51 has a total of 109 instructions. The table below shows the total number of instructions that require each execution time.

Clocks to Execute	1	2	2/3	3	3/4	4	4/5	5	8
Number of Instructions	26	50	5	14	7	3	1	2	1

With the CIP-51's maximum system clock at 25 MHz, it has a peak throughput of 25 MIPS.

1.1.3. Additional Features

The C8051F96x SoC family includes several key enhancements to the CIP-51 core and peripherals to improve performance and ease of use in end applications.

The extended interrupt handler provides multiple interrupt sources into the CIP-51 allowing numerous analog and digital peripherals to interrupt the controller. An interrupt driven system requires less intervention by the MCU, giving it more effective throughput. The extra interrupt sources are very useful when building multi-tasking, real-time systems.

Eight reset sources are available: power-on reset circuitry (POR), an on-chip V_{DD} monitor (forces reset when power supply voltage drops below safe levels), a watchdog timer (WDT), a missing clock detector, SmaRTClock oscillator fail or alarm, a voltage level detection from Comparator0, a forced software reset, an external reset pin, and an illegal flash access protection circuit. Each reset source except for the POR, reset input pin, or flash error may be disabled by the user in software. The WDT may be permanently disabled in software after a power-on reset during MCU initialization.

The internal oscillator factory calibrated to 24.5 MHz and is accurate to ±2% over the full temperature and supply range. The internal oscillator period can also be adjusted by user firmware. An additional 20 MHz low power oscillator is also available which facilitates low-power operation. An external oscillator drive circuit is included, allowing an external crystal, ceramic resonator, capacitor, RC, or CMOS clock source to generate the system clock. If desired, the system clock source may be switched on-the-fly between both internal and external oscillator circuits. An external oscillator can also be extremely useful in low power applications, allowing the MCU to run from a slow (power saving) source, while periodically switching to the fast (up to 25 MHz) internal oscillator as needed.

Table 4.11. SmaRTClock Characteristics

V_{BAT} = 1.8 to 3.8 V; T_A = –40 to +85 °C unless otherwise specified; Using factory-calibrated settings.

Parameter	Conditions	Min	Typ	Max	Units
Oscillator Frequency (LFO)		13.1	16.4	19.7	kHz

Table 4.12. ADC0 Electrical Characteristics

V_{BAT} = 1.8 to 3.8 V, VREF = 1.65 V (REFSL[1:0] = 11), –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
DC Accuracy					
Resolution	12-bit mode 10-bit mode		12 10		bits
Integral Nonlinearity	12-bit mode[1] 10-bit mode	— —	±1 ±0.5	±3 ±1	LSB
Differential Nonlinearity (Guaranteed Monotonic)	12-bit mode[1] 10-bit mode	— —	±0.8 ±0.5	±2 ±1	LSB
Offset Error	12-bit mode 10-bit mode	— —	±<1 ±<1	±3 ±3	LSB
Full Scale Error	12-bit mode[2] 10-bit mode	— —	±1 ±1	±4 ±2.5	LSB
Dynamic performance (10 kHz sine-wave single-ended input, 1 dB below Full Scale, maximum sampling rate)					
Signal-to-Noise Plus Distortion[3]	12-bit mode 10-bit mode	62 54	65 58	— —	dB
Signal-to-Distortion[3]	12-bit mode 10-bit mode	— —	76 73	— —	dB
Spurious-Free Dynamic Range[3]	12-bit mode 10-bit mode	— —	82 75	— —	dB
Conversion Rate					
SAR Conversion Clock	Normal Power Mode Low Power Mode	— —	— —	8.33 4.4	MHz
Conversion Time in SAR Clocks	10-bit Mode 8-bit Mode	13 11	— —	— —	clocks
Track/Hold Acquisition Time	Initial Acquisition Subsequent Acquisitions (dc input, burst mode)	1.5 1.1	— —	— —	us
Throughput Rate	12-bit mode 10-bit mode	— —	— —	75 300	ksps

1. INL and DNL specifications for 12-bit mode do not include the first or last four ADC codes.
2. The maximum code in 12-bit mode is 0xFFFC. The Full Scale Error is referenced from the maximum code.
3. Performance in 8-bit mode is similar to 10-bit mode.

Table 4.16. Comparator Electrical Characteristics

V_{BAT} = 1.8 to 3.8 V, –40 to +85 °C unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
Response Time: Mode 0, V_{BAT} = 2.4 V, V_{CM}* = 1.2 V	CP0+ – CP0– = 100 mV	—	120	—	ns
	CP0+ – CP0– = –100 mV	—	110	—	ns
Response Time: Mode 1, V_{BAT} = 2.4 V, V_{CM}* = 1.2 V	CP0+ – CP0– = 100 mV	—	180	—	ns
	CP0+ – CP0– = –100 mV	—	220	—	ns
Response Time: Mode 2, V_{BAT} = 2.4 V, V_{CM}* = 1.2 V	CP0+ – CP0– = 100 mV	—	350	—	ns
	CP0+ – CP0– = –100 mV	—	600	—	ns
Response Time: Mode 3, V_{BAT} = 2.4 V, V_{CM}* = 1.2 V	CP0+ – CP0– = 100 mV	—	1240	—	ns
	CP0+ – CP0– = –100 mV	—	3200	—	ns
Common-Mode Rejection Ratio		—	1.5	—	mV/V
Inverting or Non-Inverting Input Voltage Range		–0.25	—	V_{BAT} + 0.25	V
Input Capacitance		—	12	—	pF
Input Bias Current		—	1	—	nA
Input Offset Voltage		–10	—	+10	mV
Power Supply					
Power Supply Rejection		—	0.1	—	mV/V
Power-up Time	V_{BAT} = 3.8 V	—	0.6	—	µs
	V_{BAT} = 3.0 V	—	1.0	—	µs
	V_{BAT} = 2.4 V	—	1.8	—	µs
	V_{BAT} = 1.8 V	—	10	—	µs
Supply Current at DC	Mode 0	—	23	—	µA
	Mode 1	—	8.8	—	µA
	Mode 2	—	2.6	—	µA
	Mode 3	—	0.4	—	µA

***Note:** Vcm is the common-mode voltage on CP0+ and CP0–.

SFR Definition 5.4. ADC0PWR: ADC0 Burst Mode Power-Up Time

Bit	7	6	5	4	3	2	1	0
Name	AD0LPM				AD0PWR[3:0]			
Type	R/W	R	R	R	R/W			
Reset	0	0	0	0	1	1	1	1

SFR Page = 0xF; SFR Address = 0xBA

Bit	Name	Function
7	AD0LPM	**ADC0 Low Power Mode Enable.** Enables Low Power Mode Operation. 0: Low Power Mode disabled. 1: Low Power Mode enabled.
6:4	Unused	Read = 0000b; Write = Don't Care.
3:0	AD0PWR[3:0]	**ADC0 Burst Mode Power-Up Time.** Sets the time delay required for ADC0 to power up from a low power state. For BURSTEN = 0: ADC0 power state controlled by AD0EN. For BURSTEN = 1 and AD0EN = 1: ADC0 remains enabled and does not enter a low power state after all conversions are complete. Conversions can begin immediately following the start-of-conversion signal. For BURSTEN = 1 and AD0EN = 0: ADC0 enters a low power state after all conversions are complete. Conversions can begin a programmed delay after the start-of-conversion signal. The ADC0 Burst Mode Power-Up time is programmed according to the following equation: $$AD0PWR = \frac{Tstartup}{400ns} - 1$$ or $$Tstartup = (AD0PWR + 1)400ns$$ **Note:** Setting AD0PWR to 0x04 provides a typical tracking time of 2 us for the first sample taken after the start of conversion.

SFR Definition 11.7. DMA0NCF: DMA Channel Configuration

Bit	7	6	5	4	3	2	1	0
Name	INTEN	MINTEN	STALL	ENDIAN	PERIPH[3:0]			
Type	R/W	R/W	R/W	R/W	R	R/W		
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x2; SFR Address = 0xC9

Bit	Name	Function
7	INTEN	**Full-Length Interrupt Enable.** 0: Disable the full-length interrupt of the selected channel. 1: Enable the full-length interrupt of the selected channel.
6	MINTEN	**Mid-Point Interrupt Enable.** 0: Disable the mid-point interrupt of the selected channel. 1: Enable the mid-point interrupt of the selected channel.
5	STALL	**DMA0 Stall.** Setting this bit stalls the DMA0 transfer on the selected channel. After a Stall, this bit must be cleared by software to resume normal operation. 0: The DMA0 transfer of the selected channel is not being stalled. 1: The DMA0 transfer of the selected channel is stalled.
4	ENDIAN	**Data Transfer Endianness.** This bit sets the byte order for multi-byte transfers. This is only relevant for two or three byte transfers. The value of this bit does not matter for single byte transfers. 0: Little Endian 1: Big Endian
3:0	PERIPH[2:0]	**Peripheral Selection of The Selected Channel.** These bits choose one of the nine DMA0 transfer functions for the selected channel. 0000: XRAM to ENC0L/M/H 0001: ENC0L/M/H sfrs to XRAM 0010: XRAM to CRC1IN sfr 0011: XRAM to SPI1DAT sfr 0100: SPI1DAT sfr to XRAM 0101: XRAM to AES0KIN sfr 0110: XRAM to AES0BIN sfr 0111: XRAM to AES0XIN sfr 1000: AES0YOUT sfr to XRAM
Note: This sfr is a DMA channel indirect register. Select the desired channel first using the DMA0SEL sfr.		

SFR Definition 17.1. IE: Interrupt Enable

Bit	7	6	5	4	3	2	1	0
Name	EA	ESPI0	ET2	ES0	ET1	EX1	ET0	EX0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = All Pages; SFR Address = 0xA8; Bit-Addressable

Bit	Name	Function
7	EA	**Enable All Interrupts.** Globally enables/disables all interrupts. It overrides individual interrupt mask settings. 0: Disable all interrupt sources. 1: Enable each interrupt according to its individual mask setting.
6	ESPI0	**Enable Serial Peripheral Interface (SPI0) Interrupt.** This bit sets the masking of the SPI0 interrupts. 0: Disable all SPI0 interrupts. 1: Enable interrupt requests generated by SPI0.
5	ET2	**Enable Timer 2 Interrupt.** This bit sets the masking of the Timer 2 interrupt. 0: Disable Timer 2 interrupt. 1: Enable interrupt requests generated by the TF2L or TF2H flags.
4	ES0	**Enable UART0 Interrupt.** This bit sets the masking of the UART0 interrupt. 0: Disable UART0 interrupt. 1: Enable UART0 interrupt.
3	ET1	**Enable Timer 1 Interrupt.** This bit sets the masking of the Timer 1 interrupt. 0: Disable all Timer 1 interrupt. 1: Enable interrupt requests generated by the TF1 flag.
2	EX1	**Enable External Interrupt 1.** This bit sets the masking of External Interrupt 1. 0: Disable external interrupt 1. 1: Enable interrupt requests generated by the $\overline{\text{INT1}}$ input.
1	ET0	**Enable Timer 0 Interrupt.** This bit sets the masking of the Timer 0 interrupt. 0: Disable all Timer 0 interrupt. 1: Enable interrupt requests generated by the TF0 flag.
0	EX0	**Enable External Interrupt 0.** This bit sets the masking of External Interrupt 0. 0: Disable external interrupt 0. 1: Enable interrupt requests generated by the $\overline{\text{INT0}}$ input.

SFR Definition 17.5. EIE2: Extended Interrupt Enable 2

Bit	7	6	5	4	3	2	1	0
Name	EAES0	EENC0	EDMA0	EPC0	ESPI1	ERTC0F	EMAT	EWARN
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = All Pages;SFR Address = 0xE7

Bit	Name	Function
7	EAES0	**Enable AES0 Interrupt.** This bit sets the masking of AES0 interrupts. 0: Disable all AES0 interrupts. 1: Enable interrupt requests generated by AES0.
6	EENC0	**Enable Encoder (ENC0) Interrupt.** This bit sets the masking of ENC0 interrupts. 0: Disable all ENC0 interrupts. 1: Enable interrupt requests generated by ENC0.
5	EDMA0	**Enable DMA0 Interrupt.** This bit sets the masking of DMA0 interrupts. 0: Disable all DMA0 interrupts. 1: Enable interrupt requests generated by DMA0.
4	EPC0	**Enable Pulse Counter (PC0) Interrupt.** This bit sets the masking of PC0 interrupts. 0: Disable all PC0 interrupts. 1: Enable interrupt requests generated by PC0.
3	ESPI1	**Enable Serial Peripheral Interface (SPI1) Interrupt.** This bit sets the masking of the SPI1 interrupts. 0: Disable all SPI1 interrupts. 1: Enable interrupt requests generated by SPI1.
2	ERTC0F	**Enable SmaRTClock Oscillator Fail Interrupt.** This bit sets the masking of the SmaRTClock Alarm interrupt. 0: Disable SmaRTClock Alarm interrupts. 1: Enable interrupt requests generated by SmaRTClock Alarm.
1	EMAT	**Enable Port Match Interrupts.** This bit sets the masking of the Port Match Event interrupt. 0: Disable all Port Match interrupts. 1: Enable interrupt requests generated by a Port Match.
0	EWARN	**Enable VDD/DC+ Supply Monitor Early Warning Interrupt.** This bit sets the masking of the VDD/DC+ Supply Monitor Early Warning interrupt. 0: Disable the VDD/DC+ Supply Monitor Early Warning interrupt. 1: Enable interrupt requests generated by VDD/DC+ Supply Monitor.

20.2. High Power Applications

The dc-dc converter is designed to provide the system with 150 mW of output power. At high output power, an inductor with low dc resistance should be chosen in order to minimize power loss and maximize efficiency. At load currents higher than 20 mA, efficiency improvents may be achieved by placing a schottky diode (e.g. MBR052LT1) between the IND pin and GND in parallel with the internal diode (see Figure 20.1).

20.3. Pulse Skipping Mode

The dc-dc converter allows the user to set the minimum pulse width such that if the duty cycle needs to decrease below a certain width in order to maintain regulation, an entire "clock pulse" will be skipped.

Pulse skipping can provide substantial power savings, particularly at low values of load current. The converter will continue to maintain a minimum output voltage at its programmed value when pulse skipping is employed, though the output voltage ripple can be higher. Another consideration is that the dc-dc will operate with pulse-frequency modulation rather than pulse-width modulation, which makes the switching frequency spectrum less predictable; this could be an issue if the dc-dc converter is used to power a radio.

20.4. Optimizing Board Layout

The PCB layout does have an effect on the overall efficiency. The following guidelines are recommended to acheive the optimum layout:

- Place the input capacitor stack as close as possible to the VBATDC pin. The smallest capacitors in the stack should be placed closest to the VBATDC pin.
- Place the output capacitor stack as close as possible to the VDC pin. The smallest capacitors in the stack should be placed closest to the VDC pin.
- Minimize the trace length between the IND pin, the inductor, and the VDC pin.

20.5. Selecting the Optimum Switch Size

The dc-dc converter provides the ability to change the size of the built-in switches. To maximize efficiency, one of two switch sizes may be selected. The large switches are ideal for carrying high currents and the small switches are ideal for low current applications. The ideal switchover point to switch from the small switches to the large switches is at approximately 5 mA total output current.

20.6. DC-DC Converter Clocking Options

The dc-dc converter may be clocked from its internal oscillator, or from any system clock source, selectable by the CLKSEL bit (DC0CF.0). The dc-dc converter internal oscillator frequency is approximately 2.4 MHz. For a more accurate clock source, the system clock, or a divided version of the system clock may be used as the dc-dc clock source. The dc-dc converter has a built in clock divider (configured using DC0CF[6:5]) which allows any system clock frequency over 1.6 MHz to generate a valid clock in the range of 1.9 to 3.8 MHz.

When the precision internal oscillator is selected as the system clock source, the OSCICL register may be used to fine tune the oscillator frequency and the dc-dc converter clock. The oscillator frequency should only be decreased since it is factory calibrated at its maximum frequency. The minimum frequency which can be reached by the oscillator after taking into account process variations is approximately 16 MHz. The system clock routed to the dc-dc converter clock divider also may be inverted by setting the CLKINV bit (DC0CF.3) to logic 1. These options can be used to minimize interference in noise sensitive applications.

24.1. SmaRTClock Interface

The SmaRTClock Interface consists of three registers: RTC0KEY, RTC0ADR, and RTC0DAT. These interface registers are located on the CIP-51's SFR map and provide access to the SmaRTClock internal registers listed in Table 24.1. The SmaRTClock internal registers can only be accessed indirectly through the SmaRTClock Interface.

Table 24.1. SmaRTClock Internal Registers

SmaRTClock Address	SmaRTClock Register	Register Name	Description
0x00–0x03	CAPTUREn	SmaRTClock Capture Registers	Four Registers used for setting the 32-bit SmaRTClock timer or reading its current value.
0x04	RTC0CN	SmaRTClock Control Register	Controls the operation of the SmaRTClock State Machine.
0x05	RTC0XCN	SmaRTClock Oscillator Control Register	Controls the operation of the SmaRTClock Oscillator.
0x06	RTC0XCF	SmaRTClock Oscillator Configuration Register	Controls the value of the progammable oscillator load capacitance and enables/disables AutoStep.
0x07	RTC0CF	SmaRTClock Configuration Register	Contains an alarm enable and flag for each SmaRTClock alarm.
0x08–0x0B	ALARM0Bn	SmaRTClock Alarm Registers	Four registers used for setting or reading the 32-bit SmaRTClock alarm value.
0x0C–0x0F	ALARM1Bn	SmaRTClock Alarm Registers	Four registers used for setting or reading the 32-bit SmaRTClock alarm value.
0x10–0x13	ALARM2Bn	SmaRTClock Alarm Registers	Four registers used for setting or reading the 32-bit SmaRTClock alarm value.

Table 24.2. SmaRTClock Load Capacitance Settings

LOADCAP	Crystal Load Capacitance	Equivalent Capacitance seen on XTAL3 and XTAL4
0000	4.0 pF	8.0 pF
0001	4.5 pF	9.0 pF
0010	5.0 pF	10.0 pF
0011	5.5 pF	11.0 pF
0100	6.0 pF	12.0 pF
0101	6.5 pF	13.0 pF
0110	7.0 pF	14.0 pF
0111	7.5 pF	15.0 pF
1000	8.0 pF	16.0 pF
1001	8.5 pF	17.0 pF
1010	9.0 pF	18.0 pF
1011	9.5 pF	19.0 pF
1100	10.5 pF	21.0 pF
1101	11.5 pF	23.0 pF
1110	12.5 pF	25.0 pF
1111	13.5 pF	27.0 pF

24.2.5. Automatic Gain Control (Crystal Mode Only) and SmaRTClock Bias Doubling

Automatic Gain Control allows the SmaRTClock oscillator to trim the oscillation amplitude of a crystal in order to achieve the lowest possible power consumption. Automatic Gain Control automatically detects when the oscillation amplitude has reached a point where it safe to reduce the drive current, therefore, it may be enabled during crystal startup. It is recommended to enable Automatic Gain Control in most systems which use the SmaRTClock oscillator in Crystal Mode. The following are recommended crystal specifications and operating conditions when Automatic Gain Control is enabled:

- ESR < 50 kΩ
- Load Capacitance < 10 pF
- Supply Voltage < 3.0 V
- Temperature > –20 °C

When using Automatic Gain Control, it is recommended to perform an oscillation robustness test to ensure that the chosen crystal will oscillate under the worst case condition to which the system will be exposed. The worst case condition that should result in the least robust oscillation is at the following system conditions: lowest temperature, highest supply voltage, highest ESR, highest load capacitance, and lowest bias current (AGC enabled, Bias Double Disabled).

To perform the oscillation robustness test, the SmaRTClock oscillator should be enabled and selected as the system clock source. Next, the SYSCLK signal should be routed to a port pin configured as a push-pull digital output. The positive duty cycle of the output clock can be used as an indicator of oscillation robust-

27.1.3. Interfacing Port I/O to High Voltage Logic

All Port I/O configured for digital, open-drain operation are capable of interfacing to digital logic operating at a supply voltage up to VBAT + 2.0 V. An external pull-up resistor to the higher supply voltage is typically required for most systems.

27.1.4. Increasing Port I/O Drive Strength

Port I/O output drivers support a high and low drive strength; the default is low drive strength. The drive strength of a Port I/O can be configured using the PnDRV registers. See Section “4. Electrical Characteristics” on page 56 for the difference in output drive strength between the two modes.

27.2. Assigning Port I/O Pins to Analog and Digital Functions

Port I/O pins P0.0–P2.6 can be assigned to various analog, digital, and external interrupt functions. The Port pins assigned to analog functions should be configured for analog I/O and Port pins assigned to digital or external interrupt functions should be configured for digital I/O.

27.2.1. Assigning Port I/O Pins to Analog Functions

Table 27.1 shows all available analog functions that need Port I/O assignments. **Port pins selected for these analog functions should have their digital drivers disabled (PnMDOUT.n = 0 and Port Latch = 1) and their corresponding bit in PnSKIP set to 1.** This reserves the pin for use by the analog function and does not allow it to be claimed by the Crossbar. Table 27.1 shows the potential mapping of Port I/O to each analog function.

Table 27.1. Port I/O Assignment for Analog Functions

Analog Function	Potentially Assignable Port Pins	SFR(s) used for Assignment
ADC Input	P0.0–P0.7, P1.4–P2.3	ADC0MX, PnSKIP
Comparator0 Input	P0.0–P0.7, P1.4–P2.3	CPT0MX, PnSKIP
Comparator1 Input	P0.0–P0.7, P1.4–P2.3	CPT1MX, PnSKIP
LCD Pins (LCD0)	P2.4–P6.7	PnMDIN, PnSKIP
Pulse Counter (PC0)	P1.0, P1.1	P1MDIN, PnSKIP
Voltage Reference (VREF0)	P0.0	REF0CN, PnSKIP
Analog Ground Reference (AGND)	P0.1	REF0CN, PnSKIP
Current Reference (IREF0)	P0.7	IREF0CN, PnSKIP
External Oscillator Input (XTAL1)	P0.2	OSCXCN, PnSKIP
External Oscillator Output (XTAL2)	P0.3	OSCXCN, PnSKIP
SmaRTClock Input (XTAL3)	P1.2	P1MDIN, PnSKIP
SmaRTClock Output (XTAL4)	P1.3	P1MDIN, PnSKIP

27.3. Priority Crossbar Decoder

The Priority Crossbar Decoder assigns a Port I/O pin to each software selected digital function using the fixed peripheral priority order shown in Figure 27.3. The registers XBR0, XBR1, and XBR2 defined in SFR Definition 27.1, SFR Definition 27.2, and SFR Definition 27.3 are used to select digital functions in the Crossbar. The Port pins available for assignment by the Crossbar include all Port pins (P0.0–P2.6) which have their corresponding bit in PnSKIP set to 0.

From Figure 27.3, the highest priority peripheral is UART0. If UART0 is selected in the Crossbar (using the XBRn registers), then P0.4 and P0.5 will be assigned to UART0. The next highest priority peripheral is SPI1. If SPI1 is selected in the Crossbar, then P2.0–P2.2 will be assigned to SPI1. P2.3 will be assigned if SPI1 is configured for 4-wire mode. The user should ensure that the pins to be assigned by the Crossbar have their PnSKIP bits set to 0.

For all remaining digital functions selected in the Crossbar, starting at the top of Figure 27.3 going down, the least-significant unskipped, unassigned Port pin(s) are assigned to that function. If a Port pin is already assigned (e.g., UART0 or SPI1 pins), or if its PnSKIP bit is set to 1, then the Crossbar will skip over the pin and find next available unskipped, unassigned Port pin. All Port pins used for analog functions, GPIO, or dedicated digital functions such as the EMIF should have their PnSKIP bit set to 1.

Figure 27.3 shows the Crossbar Decoder priority with no Port pins skipped (P0SKIP, P1SKIP, P2SKIP = 0x00); Figure 27.4 shows the Crossbar Decoder priority with the External Oscillator pins (XTAL1 and XTAL2) skipped (P0SKIP = 0x0C).

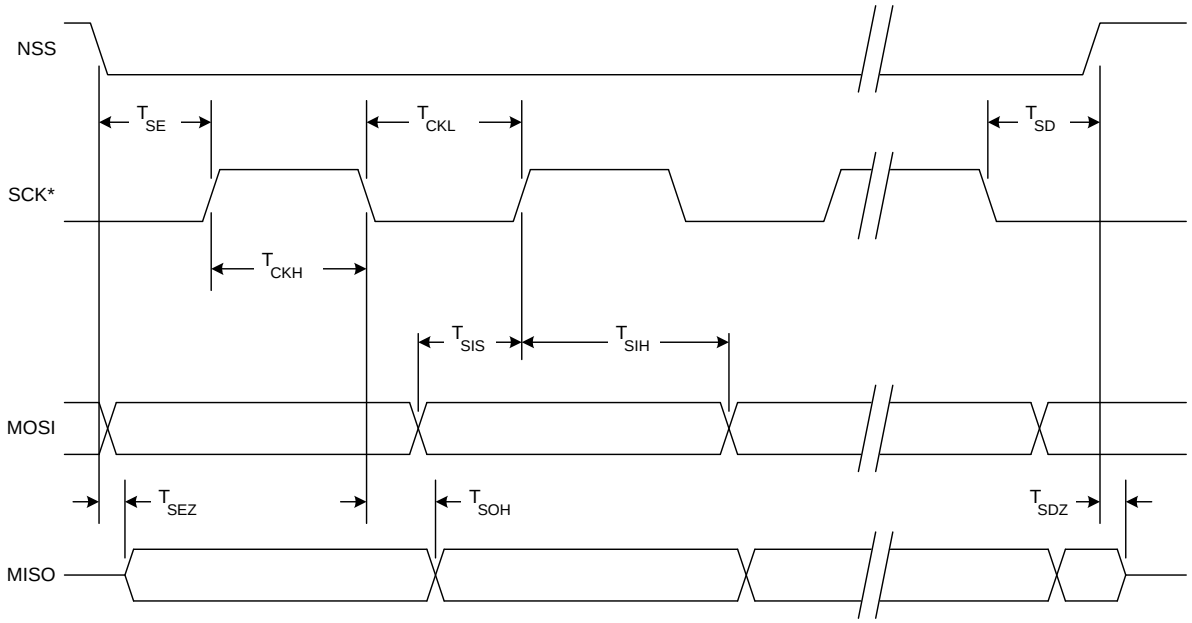
Important Notes:

- The Crossbar must be enabled (XBARE = 1) before any Port pin is used as a digital output. Port output drivers are disabled while the Crossbar is disabled.
- When SMBus is selected in the Crossbar, the pins associated with SDA and SCL will automatically be forced into open-drain output mode regardless of the PnMDOUT setting.
- SPI0 can be operated in either 3-wire or 4-wire modes, depending on the state of the NSSMD1-NSSMD0 bits in register SPI0CN. The NSS signal is only routed to a Port pin when 4-wire mode is selected. When SPI0 is selected in the Crossbar, the SPI0 mode (3-wire or 4-wire) will affect the pinout of all digital functions lower in priority than SPI0.
- For given XBRn, PnSKIP, and SPInCN register settings, one can determine the I/O pin-out of the device using Figure 27.3 and Figure 27.4.

Table 29.2. Timer Settings for Standard Baud Rates Using an External 22.1184 MHz Oscillator

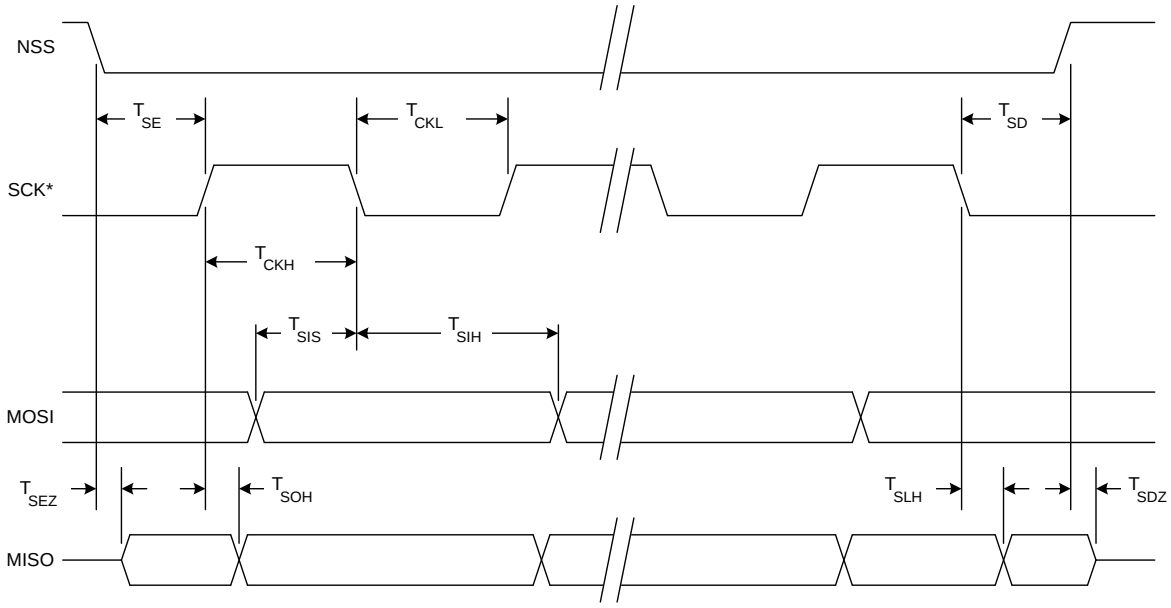
	Frequency: 22.1184 MHz						
	Target Baud Rate (bps)	Baud Rate % Error	Oscillator Divide Factor	Timer Clock Source	SCA1–SCA0 (pre-scale select)[1]	T1M[1]	Timer 1 Reload Value (hex)
SYSCLK from Internal Osc.	230400	0.00%	96	EXTCLK / 8	11	0	0xFA
	115200	0.00%	192	EXTCLK / 8	11	0	0xF4
	57600	0.00%	384	EXTCLK / 8	11	0	0xE8
	28800	0.00%	768	EXTCLK / 8	11	0	0xD0
	14400	0.00%	1536	EXTCLK / 8	11	0	0xA0
	9600	0.00%	2304	EXTCLK / 8	11	0	0x70

Notes:
1. SCA1–SCA0 and T1M bit definitions can be found in Section 32.1.
2. X = Don't care.



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 31.10. SPI Slave Timing (CKPHA = 0)



* SCK is shown for CKPOL = 0. SCK is the opposite polarity for CKPOL = 1.

Figure 31.11. SPI Slave Timing (CKPHA = 1)

32.1. Timer 0 and Timer 1

Each timer is implemented as a 16-bit register accessed as two separate bytes: a low byte (TL0 or TL1) and a high byte (TH0 or TH1). The Counter/Timer Control register (TCON) is used to enable Timer 0 and Timer 1 as well as indicate status. Timer 0 interrupts can be enabled by setting the ET0 bit in the IE register (Section “17.5. Interrupt Register Descriptions” on page 235); Timer 1 interrupts can be enabled by setting the ET1 bit in the IE register (Section “17.5. Interrupt Register Descriptions” on page 235). Both counter/timers operate in one of four primary modes selected by setting the Mode Select bits T1M1–T0M0 in the Counter/Timer Mode register (TMOD). Each timer can be configured independently. Each operating mode is described below.

32.1.1. Mode 0: 13-bit Counter/Timer

Timer 0 and Timer 1 operate as 13-bit counter/timers in Mode 0. The following describes the configuration and operation of Timer 0. However, both timers operate identically, and Timer 1 is configured in the same manner as described for Timer 0.

The TH0 register holds the eight MSBs of the 13-bit counter/timer. TL0 holds the five LSBs in bit positions TL0.4–TL0.0. The three upper bits of TL0 (TL0.7–TL0.5) are indeterminate and should be masked out or ignored when reading. As the 13-bit timer register increments and overflows from 0x1FFF (all ones) to 0x0000, the timer overflow flag TF0 (TCON.5) is set and an interrupt will occur if Timer 0 interrupts are enabled.

The C/T0 bit (TMOD.2) selects the counter/timer's clock source. When C/T0 is set to logic 1, high-to-low transitions at the selected Timer 0 input pin (T0) increment the timer register (Refer to Section “27.3. Priority Crossbar Decoder” on page 355 for information on selecting and configuring external I/O pins). Clearing C/T selects the clock defined by the T0M bit (CKCON.3). When T0M is set, Timer 0 is clocked by the system clock. When T0M is cleared, Timer 0 is clocked by the source selected by the Clock Scale bits in CKCON (see SFR Definition 32.1).

Setting the TR0 bit (TCON.4) enables the timer when either GATE0 (TMOD.3) is logic 0 or the input signal $\overline{\text{INT0}}$ is active as defined by bit IN0PL in register IT01CF (see SFR Definition 17.7). Setting GATE0 to 1 allows the timer to be controlled by the external input signal $\overline{\text{INT0}}$ (see Section “17.5. Interrupt Register Descriptions” on page 235), facilitating pulse width measurements

Table 32.1. Timer 0 Running Modes

TR0	GATE0	$\overline{\text{INT0}}$	Counter/Timer
0	X	X	Disabled
1	0	X	Enabled
1	1	0	Disabled
1	1	1	Enabled
Note: X = Don't Care			

Setting TR0 does not force the timer to reset. The timer registers should be loaded with the desired initial value before the timer is enabled.

TL1 and TH1 form the 13-bit register for Timer 1 in the same manner as described above for TL0 and TH0. Timer 1 is configured and controlled using the relevant TCON and TMOD bits just as with Timer 0. The input signal $\overline{\text{INT1}}$ is used with Timer 1; the $\overline{\text{INT1}}$ polarity is defined by bit IN1PL in register IT01CF (see SFR Definition 17.7).

SFR Definition 32.4. TL0: Timer 0 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TL0[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0x8A

Bit	Name	Function
7:0	TL0[7:0]	**Timer 0 Low Byte.** The TL0 register is the low byte of the 16-bit Timer 0.

SFR Definition 32.5. TL1: Timer 1 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TL1[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0x8B

Bit	Name	Function
7:0	TL1[7:0]	**Timer 1 Low Byte.** The TL1 register is the low byte of the 16-bit Timer 1.

SFR Definition 32.13. TMR3CN: Timer 3 Control

Bit	7	6	5	4	3	2	1	0
Name	TF3H	TF3L	TF3LEN	TF3CEN	T3SPLIT	TR3	T3XCLK[1:0]	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0x91

Bit	Name	Function
7	TF3H	**Timer 3 High Byte Overflow Flag.** Set by hardware when the Timer 3 high byte overflows from 0xFF to 0x00. In 16 bit mode, this will occur when Timer 3 overflows from 0xFFFF to 0x0000. When the Timer 3 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 3 interrupt service routine. This bit is not automatically cleared by hardware.
6	TF3L	**Timer 3 Low Byte Overflow Flag.** Set by hardware when the Timer 3 low byte overflows from 0xFF to 0x00. TF3L will be set when the low byte overflows regardless of the Timer 3 mode. This bit is not automatically cleared by hardware.
5	TF3LEN	**Timer 3 Low Byte Interrupt Enable.** When set to 1, this bit enables Timer 3 Low Byte interrupts. If Timer 3 interrupts are also enabled, an interrupt will be generated when the low byte of Timer 3 overflows.
4	TF3CEN	**Timer 3 SmaRTClock/External Oscillator Capture Enable.** When set to 1, this bit enables Timer 3 Capture Mode.
3	T3SPLIT	**Timer 3 Split Mode Enable.** When this bit is set, Timer 3 operates as two 8-bit timers with auto-reload. 0: Timer 3 operates in 16-bit auto-reload mode. 1: Timer 3 operates as two 8-bit auto-reload timers.
2	TR3	**Timer 3 Run Control.** Timer 3 is enabled by setting this bit to 1. In 8-bit mode, this bit enables/disables TMR3H only; TMR3L is always enabled in split mode.
1:0	T3XCLK[1:0]	**Timer 3 External Clock Select.** This bit selects the “external” and “capture trigger” clock sources for Timer 3. If Timer 3 is in 8-bit mode, this bit selects the “external” clock source for both timer bytes. Timer 3 Clock Select bits (T3MH and T3ML in register CKCON) may still be used to select between the “external” clock and the system clock for either timer. Note: External clock sources are synchronized with the system clock. 00: External Clock is SYSCLK /12. Capture trigger is SmaRTClock. 01: External Clock is External Oscillator/8. Capture trigger is SmaRTClock. 10: External Clock is SYSCLK/12. Capture trigger is External Oscillator/8. 11: External Clock is SmaRTClock. Capture trigger is External Oscillator/8.

SFR Definition 32.16. TMR3L: Timer 3 Low Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR3L[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0x94

Bit	Name	Function
7:0	TMR3L[7:0]	**Timer 3 Low Byte.** In 16-bit mode, the TMR3L register contains the low byte of the 16-bit Timer 3. In 8-bit mode, TMR3L contains the 8-bit low byte timer value.

SFR Definition 32.17. TMR3H Timer 3 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TMR3H[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0x95

Bit	Name	Function
7:0	TMR3H[7:0]	**Timer 3 High Byte.** In 16-bit mode, the TMR3H register contains the high byte of the 16-bit Timer 3. In 8-bit mode, TMR3H contains the 8-bit high byte timer value.