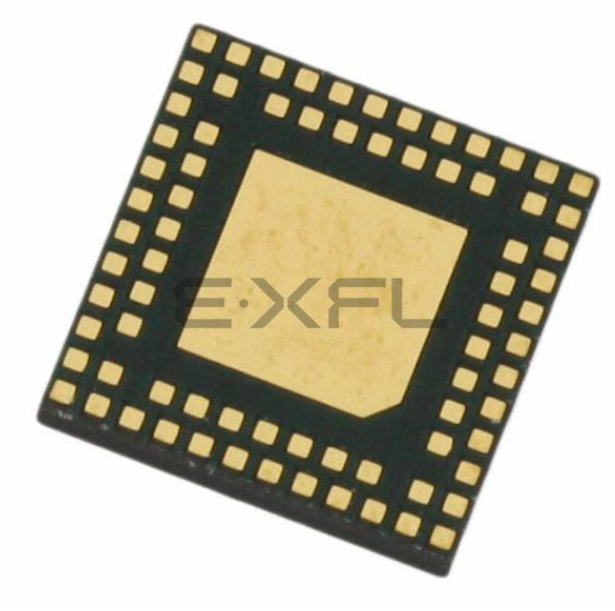

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, LCD, POR, PWM, WDT
Number of I/O	57
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	76-VFQFN Dual Rows, Exposed Pad
Supplier Device Package	76-DQFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f968-a-gmr

Table 4.7. Power Management Electrical Specifications

V_{BAT} = 1.8 to 3.8 V, –40 to +85 °C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Idle Mode Wake-up Time		2	—	3	SYSCLKs
Suspend Mode Wake-up Time	CLKDIV = 0x00 Low Power or Precision Osc.	—	400	—	ns
Sleep Mode Wake-up Time		—	2	—	µs

Table 4.8. Flash Electrical Characteristics

V_{BAT} = 1.8 to 3.8 V, –40 to +85 °C unless otherwise specified.,

Parameter	Conditions	Min	Typ	Max	Units
Flash Size	C8051F960/1/2/3	131072	—	—	bytes
	C8051F964/5	65536	—	—	bytes
	C8051F966/7	32768	—	—	bytes
	C8051F968/9	16384	—	—	bytes
Endurance		20 k	100k	—	Erase/Write Cycles
Erase Cycle Time		28	32	36	ms
Write Cycle Time		57	64	71	µs

Table 4.9. Internal Precision Oscillator Electrical Characteristics

V_{BAT} = 1.8 to 3.8 V; T_A = –40 to +85 °C unless otherwise specified; Using factory-calibrated settings.

Parameter	Conditions	Min	Typ	Max	Units
Oscillator Frequency	–40 to +85 °C, V_{BAT} = 1.8–3.8 V	24	24.5	25	MHz
Oscillator Supply Current (from V_{BAT})	25 °C; includes bias current of 50 µA typical	—	300*	—	µA
***Note:** Does not include clock divider or clock tree supply current.					

Table 4.10. Internal Low-Power Oscillator Electrical Characteristics

V_{BAT} = 1.8 to 3.8 V; T_A = –40 to +85 °C unless otherwise specified; Using factory-calibrated settings.

Parameter	Conditions	Min	Typ	Max	Units
Oscillator Frequency	–40 to +85 °C, V_{BAT} = 1.8–3.8 V	18	20	22	MHz
Oscillator Supply Current (from V_{BAT})	25 °C No separate bias current required	—	100*	—	µA
***Note:** Does not include clock divider or clock tree supply current.					

SFR Definition 11.5. DMA0SEL: DMA0 Channel Select for Configuration

Bit	7	6	5	4	3	2	1	0
Name						DMA0SEL[2:0]		
Type	R	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x2; SFR Address = 0xD1

Bit	Name	Function
7:3	Unused	Read = 0b, Write = Don't Care
2:0	DMA0SEL[2:0]	**Channel Select for Configuration.** These bits select the channel for configuration of the DMA0 transfer. The first step to configure a channel for DMA0 transfer is to select the desired channel, and then write to channel specific registers DMA0NCF, DMA0NBAL/H, DMA0NAOL/H, DMA0NSZL/H. 000: Select channel 0 001: Select channel 1 010: Select channel 2 011: Select channel 3 100: Select channel 4 101: Select channel 5 110: Select channel 6 111: Invalid

SFR Definition 13.1. CRC1CN: CRC1 Control

Bit	7	6	5	4	3	2	1	0
Name	CLR				DMA	FLIP	INV	SEED
Type	R/W	R	R	R	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x2; SFR Address = 0xBE; Not Bit-Addressable

Bit	Name	Function
7	CLR	**Reset.** Setting this bit to 1 will reset the CRC module and set the CRC results SFR to the seed value as specified by the SEED bit. The CRC module should be reset before starting a new CRC. This bit is self-clearing.
6:4	Reserved	
3	DMA	**DMA Mode.** Setting this bit will configure the CRC1 module for DMA mode. Once a DMA channel has been configured to use accept peripheral requests from CRC1, setting this bit will initiate a DMA CRC operation. This bit should be cleared after each CRC DMA transfer.
2	FLIP	**Flip.** Setting this bit will flip the contents of the 16-bit CRC result SFRs. (CRC0OUTH:CRC0OUTL) This operation is normally performed only on the final CRC results. This bit should be cleared before starting a new CRC computation.
1	INV	**Invert.** Setting this bit will invert the contents of the 16-bit CRC result SFR. (CRC0OUTH:CRC0OUTL) This operation is normally performed only on the final CRC results. This bit should be cleared before starting a new CRC computation.
0	SEED	**Seed Polarity.** If this bit is zero, a seed value or 0x0000 will be used. If this bit is 1, a seed value of 0xFFFF will be used. This bit should be set before setting the RST bit.

14.5. AES Block Cipher Decryption

14.5.1. AES Block Cipher Decryption using DMA

Normally, the AES block is used with the DMA. This provides the best performance and lowest power consumption. Code examples are provided in 8051 compiler independent C code using the DMA. It is highly recommended to use with the code examples. The steps are documented in the datasheet for completeness.

- Prepare decryption key and data to be decryption in xram.
- Reset AES module by clearing bit 2 of AES0BCFG.
- sable the first three DMA channels by clearing bits 0 to 2 in the DMA0EN sfr.
- Configure the first DMA channel for the AES0KIN sfr
  - Select the first DMA channel by writing 0x00 to the DMA0SEL sfr
  - Configure the first DMA channel to move xram to AES0KIN sfr by writing 0x05 to the DMA0NCF sfr
  - Write 0x01 to DMA0NMD to enable wrapping
  - Write the xram location of decryption key to the DMA0NBAH and DMA0NBAL sfrs.
  - Write the key length in bytes to DMA0NSZL sfr
  - Clear the DMA0NSZH sfr
  - Clear the DMA0NAOH and DMA0NAOL sfrs.
- Configure the second DMA channel for the AES0BIN sfr.
  - Select the second DMA channel by writing 0x01 to the DMA0SEL sfr.
  - Configure the second DMA channel to move xram to AES0BIN sfr by writing 0x06 to the DMA0NCF sfr.
  - Clear DMA0NMD to disable wrapping.
  - Write the xram address of the data to be decrypted to the DMA0NBAH and DMA0NBAL sfrs.
  - Write the number of bytes to be decrypted in multiples of 16 bytes to the DMA0NSZH and DMA0NSZL sfrs.
  - Clear the DMA0NAOH and DMA0NAOL sfrs.
- Configure the third DMA channel for the AES0YOUT sfr
  - Select the third DMA channel by writing 0x02 to the DMA0SEL sfr
  - Configure the third DMA channel to move the contents of the AES0YOUT sfr to xram by writing 0x08 to the DMA0NCF sfr
  - Enable transfer complete interrupt by setting bit 7 of DMA0NCF sfr
  - Clear DMA0NMD to disable wrapping
  - Write the xram address for decrypted data to the DMA0NBAH and DMA0NBAL sfrs.
  - Write the number of bytes to be decrypted in multiples of 16 bytes to the DMA0NSZH and DMA0NSZL sfrs.
  - Clear the DMA0NSZH sfr
  - Clear the DMA0NAOH and DMA0NAOL sfrs.
- Clear first three DMA interrupts by clearing bits 0 to 2 in the DMA0INT sfr.
- Enable first three DMA channels setting bits 0 to 2 in the DMA0EN sfr
- Configure the AES Module data flow for AES Block Cipher by writing 0x00 to the AES0DCFG sfr.
- Write key size to bits 1 and 0 of the AES0BCFG
- Configure the AES core for decryption by clearing bit 2 of AES0BCFG
- Initiate the encryption operation be setting bit 3 of AES0BCFG
- Wait on the DMA interrupt from DMA channel 2
- Disable the AES Module by clearing bit 2 of AES0BCFG
- Disable the DMA by writing 0x00 to DMA0EN

14.6.4.2. CBC Decryption using SFRs

- First Configure AES Module for CBC Block Cipher Mode Decryption
  - Reset AES module by writing 0x00 to AES0BCFG.
  - Configure the AES Module data flow for XOR on output data by writing 0x02 to the AES0DCFG sfr.
  - Write key size to bits 1 and 0 of the AES0BCFG.
  - Configure the AES core for decryption by setting bit 2 of AES0BCFG.
  - Enable the AES core by setting bit 3 of AES0BCFG.
- Repeat alternating write sequence 16 times
  - Write plaintext byte to AES0BIN.
  - Write encryption key byte to AES0KIN.
- Write remaining encryption key bytes to AES0KIN for 192-bit and 256-bit decryption only.
- Wait on AES done interrupt or poll bit 5 of AES0BCFG.
- Repeat alternating write read sequence 16 times
  - Write initialization vector to AES0XIN
  - Read decrypted data from AES0YOUT

If decrypting multiple blocks, this process may be repeated. It is not necessary reconfigure the AES module for each block. When using Cipher Block Chaining the initialization vector is written to the AES0XIN sfr for the first block only, as described. Additional blocks will chain the ciphertext data from the previous block.

15.1. Manchester Encoding

To encode Manchester Data, first clear the MODE bit for Manchester encoding or decoding.

To encode, one byte of data is written to the data register ENC0L.

Setting the ENC bit will initiate encoding. After encoding, the encoded data will be in ENC0M and ENC0L. The upper nibble of the input data is encoded and placed in ENC0M. The lower nibble is encoded and placed in ENC0L.

Note that the input data should be readable in the data register until the encode bit is set. Once the READY bit is set, the input data has been replaced by the output data.

The ENC and DEC bits are self clearing. The READY bit is not cleared by hardware and must be cleared manually. The control register does not need to be bit addressable. The READY bit can be cleared while setting the ENC or DEC bit using a direct or immediate SFR mov instruction.

Table 15.2. Manchester Encoding

Input Data			Encoded Output		
nibble			byte		
dec	hex	bin	bin	hex	dec
0	0	0000	10101010	AA	170
1	1	0001	10101001	A9	169
2	2	0010	10100110	A6	166
3	3	0011	10100101	A5	165
4	4	0100	10011010	9A	154
5	5	0101	10011001	99	153
6	6	0110	10010110	96	150
7	7	0111	10010101	95	149
8	8	1000	01101010	6A	106
9	9	1001	01101001	69	105
10	A	1010	01100110	66	102
11	B	1011	01100101	65	101
12	C	1100	01011010	5A	90
13	D	1101	01011001	59	89
14	E	1110	01010110	56	86
15	F	1111	01010101	55	85

Table 17.1. Interrupt Summary

Interrupt Source	Interrupt Vector	Priority Order	Pending Flag	Bit addressable?	Cleared by HW?	Enable Flag	Priority Control
SmaRTClock Oscillator Fail	0x008B	17	OSCFAIL (RTC0CN.5)[2]	N	N	ERTC0F (EIE2.2)	PFRTC0F (EIP2.2)
SPI1	0x0093	18	SPIF (SPI1CN.7) WCOL (SPI1CN.6) MODF (SPI1CN.5) RXOVRN (SPI1CN.4)	N	N	ESPI1 (EIE2.3)	PSPI1 (EIP2.3)
Pulse Counter	0x009B	19	C0ZF (PC0CN.4) C1ZF (PC0CN.6)	N	N	EPC0 (EIE2.4)	PPC0 (EIP2.4)
DMA0	0x00A3	20	DMAINT0...7 DMAMINT0...7	N	N	EDMA0 (EIE2.5)	PDMA0 (EIP2.5)
Encoder0	0x00AB	21	ENCERR(ENCCN.6)	N	N	EENC0 (EIE2.6)	PENC0 (EIP2.6)
AES	0x00B3	22	AESDONE (AESBCF.5)	N	N	EAES0 (EIE2.7)	PAES0 (EIP2.7)

Notes:
1. Indicates a read-only interrupt pending flag. The interrupt enable may be used to prevent software from vectoring to the associated interrupt service routine.
2. Indicates a register located in an indirect memory space.

17.5. Interrupt Register Descriptions

The SFRs used to enable the interrupt sources and set their priority level are described in the following register descriptions. Refer to the data sheet section associated with a particular on-chip peripheral for information regarding valid interrupt conditions for the peripheral and the behavior of its interrupt-pending flag(s).

SFR Definition 17.4. EIP1: Extended Interrupt Priority 1

Bit	7	6	5	4	3	2	1	0
Name	PT3	PCP1	PCP0	PPCA0	PADC0	PWADC0	PRTC0A	PSMB0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = All Pages; SFR Address = 0xF6

Bit	Name	Function
7	PT3	**Timer 3 Interrupt Priority Control.** This bit sets the priority of the Timer 3 interrupt. 0: Timer 3 interrupts set to low priority level. 1: Timer 3 interrupts set to high priority level.
6	PCP1	**Comparator1 (CP1) Interrupt Priority Control.** This bit sets the priority of the CP1 interrupt. 0: CP1 interrupt set to low priority level. 1: CP1 interrupt set to high priority level.
5	PCP0	**Comparator0 (CP0) Interrupt Priority Control.** This bit sets the priority of the CP0 interrupt. 0: CP0 interrupt set to low priority level. 1: CP0 interrupt set to high priority level.
4	PPCA0	**Programmable Counter Array (PCA0) Interrupt Priority Control.** This bit sets the priority of the PCA0 interrupt. 0: PCA0 interrupt set to low priority level. 1: PCA0 interrupt set to high priority level.
3	PADC0	**ADC0 Conversion Complete Interrupt Priority Control.** This bit sets the priority of the ADC0 Conversion Complete interrupt. 0: ADC0 Conversion Complete interrupt set to low priority level. 1: ADC0 Conversion Complete interrupt set to high priority level.
2	PWADC0	**ADC0 Window Comparator Interrupt Priority Control.** This bit sets the priority of the ADC0 Window interrupt. 0: ADC0 Window interrupt set to low priority level. 1: ADC0 Window interrupt set to high priority level.
1	PRTC0A	**SmaRTClock Alarm Interrupt Priority Control.** This bit sets the priority of the SmaRTClock Alarm interrupt. 0: SmaRTClock Alarm interrupt set to low priority level. 1: SmaRTClock Alarm interrupt set to high priority level.
0	PSMB0	**SMBus (SMB0) Interrupt Priority Control.** This bit sets the priority of the SMB0 interrupt. 0: SMB0 interrupt set to low priority level. 1: SMB0 interrupt set to high priority level.

18.5. Flash Write and Erase Guidelines

Any system which contains routines which write or erase flash memory from software involves some risk that the write or erase routines will execute unintentionally if the CPU is operating outside its specified operating range of VDD, system clock frequency, or temperature. This accidental execution of flash modifying code can result in alteration of flash memory contents causing a system failure that is only recoverable by re-Flashing the code in the device.

To help prevent the accidental modification of flash by firmware, the VDD Monitor must be enabled and enabled as a reset source on C8051F96x devices for the flash to be successfully modified. **If either the VDD Monitor or the VDD Monitor reset source is not enabled, a Flash Error Device Reset will be generated when the firmware attempts to modify the flash.**

The following guidelines are recommended for any system that contains routines which write or erase flash from code.

18.5.1. VDD Maintenance and the VDD Monitor

1. If the system power supply is subject to voltage or current "spikes," add sufficient transient protection devices to the power supply to ensure that the supply voltages listed in the Absolute Maximum Ratings table are not exceeded.
2. Make certain that the minimum VDD rise time specification of 1 ms is met. If the system cannot meet this rise time specification, then add an external VDD brownout circuit to the $\overline{\text{RST}}$ pin of the device that holds the device in reset until VDD reaches the minimum device operating voltage and re-asserts $\overline{\text{RST}}$ if VDD drops below the minimum device operating voltage.
3. Keep the on-chip VDD Monitor enabled and enable the VDD Monitor as a reset source as early in code as possible. This should be the first set of instructions executed after the Reset Vector. For C-based systems, this will involve modifying the startup code added by the 'C' compiler. See your compiler documentation for more details. Make certain that there are no delays in software between enabling the VDD Monitor and enabling the VDD Monitor as a reset source. Code examples showing this can be found in “AN201: Writing to Flash from Firmware," available from the Silicon Laboratories web site.

Notes:
On C8051F96x devices, both the VDD Monitor and the VDD Monitor reset source must be enabled to write or erase flash without generating a Flash Error Device Reset.

On C8051F96x devices, both the VDD Monitor and the VDD Monitor reset source are enabled by hardware after a power-on reset.

4. As an added precaution, explicitly enable the VDD Monitor and enable the VDD Monitor as a reset source inside the functions that write and erase flash memory. The VDD Monitor enable instructions should be placed just after the instruction to set PSWE to a 1, but before the flash write or erase operation instruction.
5. Make certain that all writes to the RSTSRC (Reset Sources) register use direct assignment operators and explicitly DO NOT use the bit-wise operators (such as AND or OR). For example, "RSTSRC = 0x02" is correct, but "RSTSRC |= 0x02" is incorrect.
6. Make certain that all writes to the RSTSRC register explicitly set the PORSF bit to a '1'. Areas to check are initialization code which enables other reset sources, such as the Missing Clock Detector or Comparator, for example, and instructions which force a Software Reset. A global search on "RSTSRC" can quickly verify this.

23.3.2. External RC Mode

If an RC network is used as the external oscillator, the circuit should be configured as shown in Figure 23.1, Option 2. The RC network should be added to XTAL2, and XTAL2 should be configured for analog I/O with the digital output drivers disabled. XTAL1 is not affected in RC mode.

The capacitor should be no greater than 100 pF; however for very small capacitors, the total capacitance may be dominated by parasitic capacitance in the PCB layout. The resistor should be no smaller than 10 kΩ. The oscillation frequency can be determined by the following equation:

$$f = \frac{1.23 \times 10^3}{R \times C}$$

where
f = frequency of clock in MHzR = pull-up resistor value in kΩ
V_{DD} = power supply voltage in VoltsC = capacitor value on the XTAL2 pin in pF

To determine the required External Oscillator Frequency Control value (XFCN) in the OSCXCN Register, first select the RC network value to produce the desired frequency of oscillation. For example, if the frequency desired is 100 kHz, let R = 246 kΩ and C = 50 pF:

$$f = \frac{1.23 \times 10^3}{R \times C} = \frac{1.23 \times 10^3}{246 \times 50} = 100 \text{ kHz}$$

where
f = frequency of clock in MHz R = pull-up resistor value in kΩ
V_{DD} = power supply voltage in Volts C = capacitor value on the XTAL2 pin in pF

Referencing Table 23.2, the recommended XFCN setting is 010.

Table 23.2. Recommended XFCN Settings for RC and C modes

XFCN	Approximate Frequency Range (RC and C Mode)	K Factor (C Mode)	Typical Supply Current/ Actual Measured Frequency (C Mode, VDD = 2.4 V)
000	f ≤ 25 kHz	K Factor = 0.87	3.0 µA, f = 11 kHz, C = 33 pF
001	25 kHz < f ≤ 50 kHz	K Factor = 2.6	5.5 µA, f = 33 kHz, C = 33 pF
010	50 kHz < f ≤ 100 kHz	K Factor = 7.7	13 µA, f = 98 kHz, C = 33 pF
011	100 kHz < f ≤ 200 kHz	K Factor = 22	32 µA, f = 270 kHz, C = 33 pF
100	200 kHz < f ≤ 400 kHz	K Factor = 65	82 µA, f = 310 kHz, C = 46 pF
101	400 kHz < f ≤ 800 kHz	K Factor = 180	242 µA, f = 890 kHz, C = 46 pF
110	800 kHz < f ≤ 1.6 MHz	K Factor = 664	1.0 mA, f = 2.0 MHz, C = 46 pF
111	1.6 MHz < f ≤ 3.2 MHz	K Factor = 1590	4.6 mA, f = 6.8 MHz, C = 46 pF

When the RC oscillator is first enabled, the external oscillator valid detector allows software to determine when oscillation has stabilized. The recommended procedure for starting the RC oscillator is as follows:

1. Configure XTAL2 for analog I/O and disable the digital output drivers.
2. Configure and enable the external oscillator.
3. Poll for XTLVLD $\geq$ 1.
4. Switch the system clock to the external oscillator.

24. SmaRTClock (Real Time Clock)

C8051F96x devices include an ultra low power 32-bit SmaRTClock Peripheral (Real Time Clock) with alarm. The SmaRTClock has a dedicated 32 kHz oscillator that can be configured for use with or without a crystal. No external resistor or loading capacitors are required. The on-chip loading capacitors are programmable to 16 discrete levels allowing compatibility with a wide range of crystals. The SmaRTClock can operate directly from a 1.8–3.6 V battery voltage and remains operational even when the device goes into its lowest power down mode. The SmaRTClock output can be buffered and routed to a GPIO pin to provide an accurate, low frequency clock to other devices while the MCU is in its lowest power down mode (see “PMU0MD: Power Management Unit Mode” on page 267 for more details). C8051F96x devices also support an ultra low power internal LFO that reduces sleep mode current.

The SmaRTClock allows a maximum of 36 hour 32-bit independent time-keeping when used with a 32.768 kHz Watch Crystal. The SmaRTClock provides an Alarm and Missing SmaRTClock events, which could be used as reset or wakeup sources. See Section “22. Reset Sources” on page 278 and Section “19. Power Management” on page 257 for details on reset sources and low power mode wake-up sources, respectively.

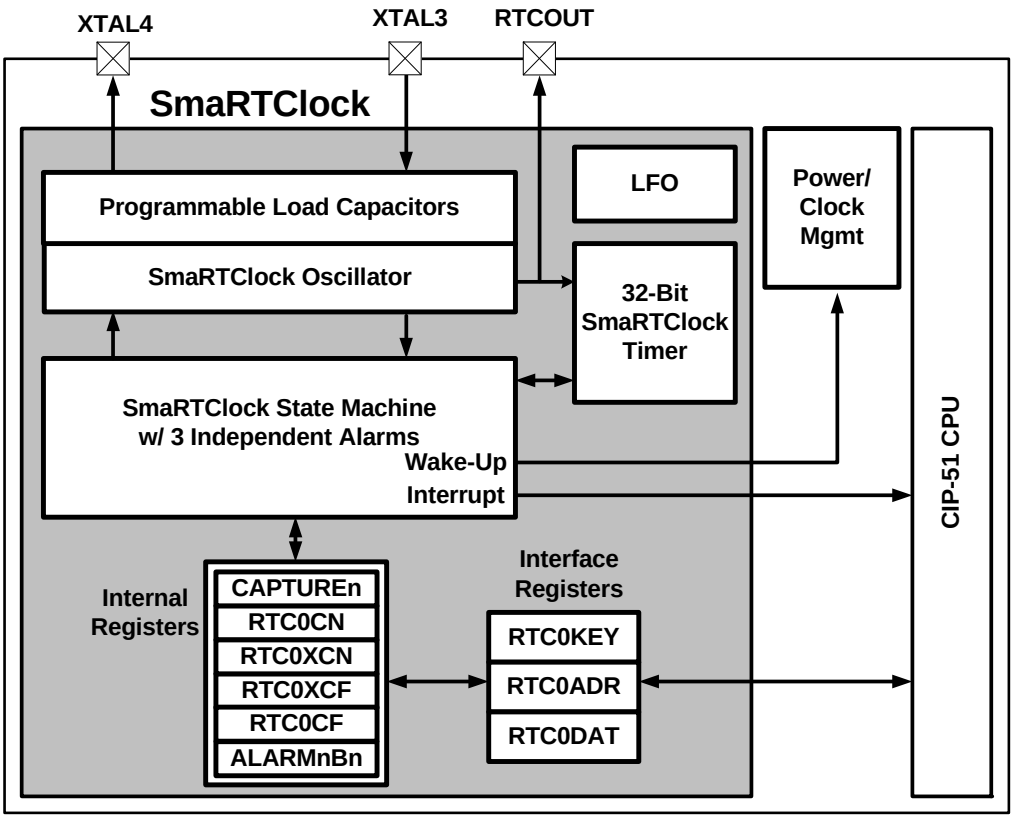

Figure 24.1. SmaRTClock Block Diagram

SFR Definition 26.2. LCD0CN: LCD0 Control Register

Bit	7	6	5	4	3	2	1	0
Name		CLKDIV[1:0]		BLANK	SIZE	MUXMD[1:0]		BIAS
Type	R/W	R/W	R/W	R/W	R/W	R/W		R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x2; SFR Address = 0x9D

Bit	Name	Function
7	Reserved	Read = 0. Must Write 0b.
6:5	CLKDIV[1:0]	**LCD0 Clock Divider.** Divides the SmaRTClock output for use by the LCD0 module. See Table 4.18 on page 76 for LCD clock frequency range. 00: The LCD clock is the SmaRTClock divided by 1. 01: The LCD clock is the SmaRTClock divided by 2. 10: The LCD clock is the SmaRTClock divded by 4. 11: Reserved.
4	BLANK	**Blank All Segments.** Blanks all LCD segments using a single bit. 0: All LCD segments are controlled by the LCD0Dn registers. 1: All LCD segments are blank (turned off).
3	SIZE	**LCD Size Select.** Selects whether 16 or 32 segment pins will be used for the LCD function. 0: P0 and P1 are used as LCD segment pins. 1: P0, P1, P2, and P3 are used as LCD segment pins.
2:1	MUXMD[1:0]	**LCD Bias Power Mode.** Selects the mux mode. 00: Static mode selected. 01: 2-mux mode selected. 10: 3-mux mode selected. 11: 4-mux mode selected.
0	BIAS	**Bias Select**. Selects between 1/2 Bias and 1/3 Bias. This bit is ignored if Static mode is selected. 0: LCD0 is configured for 1/3 Bias. 1: LCD0 is configured for 1/2 Bias.

26.3. LCD Contrast Adjustment

The LCD Bias voltages which determine the LCD contrast are generated using the VBAT supply voltage or the on-chip charge pump. There are four contrast control modes to accomodate a wide variety of applications and supply voltages. The target contrast voltage is programmable in 60 mV steps from 1.9 to 3.72 V. The LCD contrast voltage is controlled by the LCD0CNTRST register and the contrast control mode is selected by setting the appropriate bits in the LCD0MSCN, LCD0MSCF, LCD0PWR, and LCD0VBMCN registers.

Note: An external 10 µF decoupling capacitor is required on the VLCD pin to create a charge reservoir at the output of the charge pump.

Table 26.1. Bit Configurations to select Contrast Control Modes

Mode	LCD0MSCN.2	LCD0MSCF.0	LCD0PWR.3	LCD0VBMCN.7
1	0	1	0	0
2	0	1	1	1
3	1*	0	1	1
4	1*	0	0	1
*** May be set to 0 to support increased load currents.**				

26.3.1. Contrast Control Mode 1 (Bypass Mode)

In Contrast Control Mode 1, the contrast control circuitry is disabled and the VLCD voltage follows the VBAT supply voltage, as shown in Figure 26.3. This mode is useful in systems where the VBAT voltage always remains constant and will provide the lowest LCD power consumption. Bypass Mode is selected using the following procedure:

1. Clear Bit 2 of the LCD0MSCN register to 0b (LCD0MSCN &= ~0x04)
2. Set Bit 0 of the LCD0MSCF register to 1b (LCD0MSCF |= 0x01)
3. Clear Bit 3 of the LCD0PWR register to 0b (LCD0PWR &= ~0x08)
4. Clear Bit 7 of the LCD0VBMCN register to 0b (LCD0VBMCN &= ~0x80)

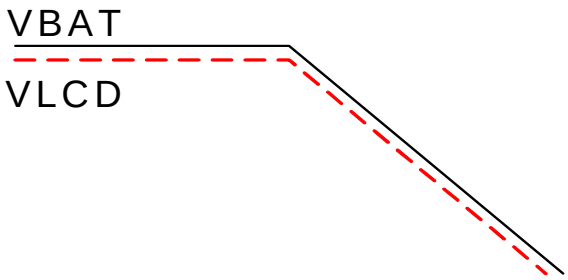

Figure 26.3. Contrast Control Mode 1

29.2. Operational Modes

UART0 provides standard asynchronous, full duplex communication. The UART mode (8-bit or 9-bit) is selected by the S0MODE bit (SCON0.7). Typical UART connection options are shown below.

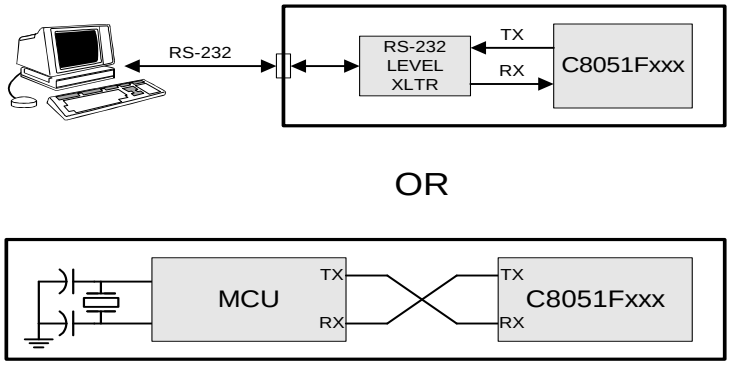

Figure 29.3. UART Interconnect Diagram

29.2.1. 8-Bit UART

8-Bit UART mode uses a total of 10 bits per data byte: one start bit, eight data bits (LSB first), and one stop bit. Data are transmitted LSB first from the TX0 pin and received at the RX0 pin. On receive, the eight data bits are stored in SBUF0 and the stop bit goes into RB80 (SCON0.2).

Data transmission begins when software writes a data byte to the SBUF0 register. The TI0 Transmit Interrupt Flag (SCON0.1) is set at the end of the transmission (the beginning of the stop-bit time). Data reception can begin any time after the REN0 Receive Enable bit (SCON0.4) is set to logic 1. After the stop bit is received, the data byte will be loaded into the SBUF0 receive register if the following conditions are met: RI0 must be logic 0, and if MCE0 is logic 1, the stop bit must be logic 1. In the event of a receive data overrun, the first received 8 bits are latched into the SBUF0 receive register and the following overrun data bits are lost.

If these conditions are met, the eight bits of data is stored in SBUF0, the stop bit is stored in RB80 and the RI0 flag is set. If these conditions are not met, SBUF0 and RB80 will not be loaded and the RI0 flag will not be set. An interrupt will occur if enabled when either TI0 or RI0 is set.

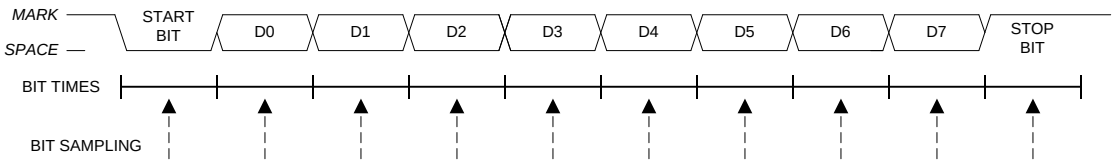

Figure 29.4. 8-Bit UART Timing Diagram

29.2.2. 9-Bit UART

9-bit UART mode uses a total of eleven bits per data byte: a start bit, 8 data bits (LSB first), a programmable ninth data bit, and a stop bit. The state of the ninth transmit data bit is determined by the value in TB80 (SCON0.3), which is assigned by user software. It can be assigned the value of the parity flag (bit P in register PSW) for error detection, or used in multiprocessor communications. On receive, the ninth data bit goes into RB80 (SCON0.2) and the stop bit is ignored.

30. Enhanced Serial Peripheral Interface (SPI0)

The Enhanced Serial Peripheral Interface (SPI0) provides access to a flexible, full-duplex synchronous serial bus. SPI0 can operate as a master or slave device in both 3-wire or 4-wire modes, and supports multiple masters and slaves on a single SPI bus. The slave-select (NSS) signal can be configured as an input to select SPI0 in slave mode, or to disable Master Mode operation in a multi-master environment, avoiding contention on the SPI bus when more than one master attempts simultaneous data transfers. NSS can also be configured as a chip-select output in master mode, or disabled for 3-wire operation. Additional general purpose port I/O pins can be used to select multiple slave devices in master mode.

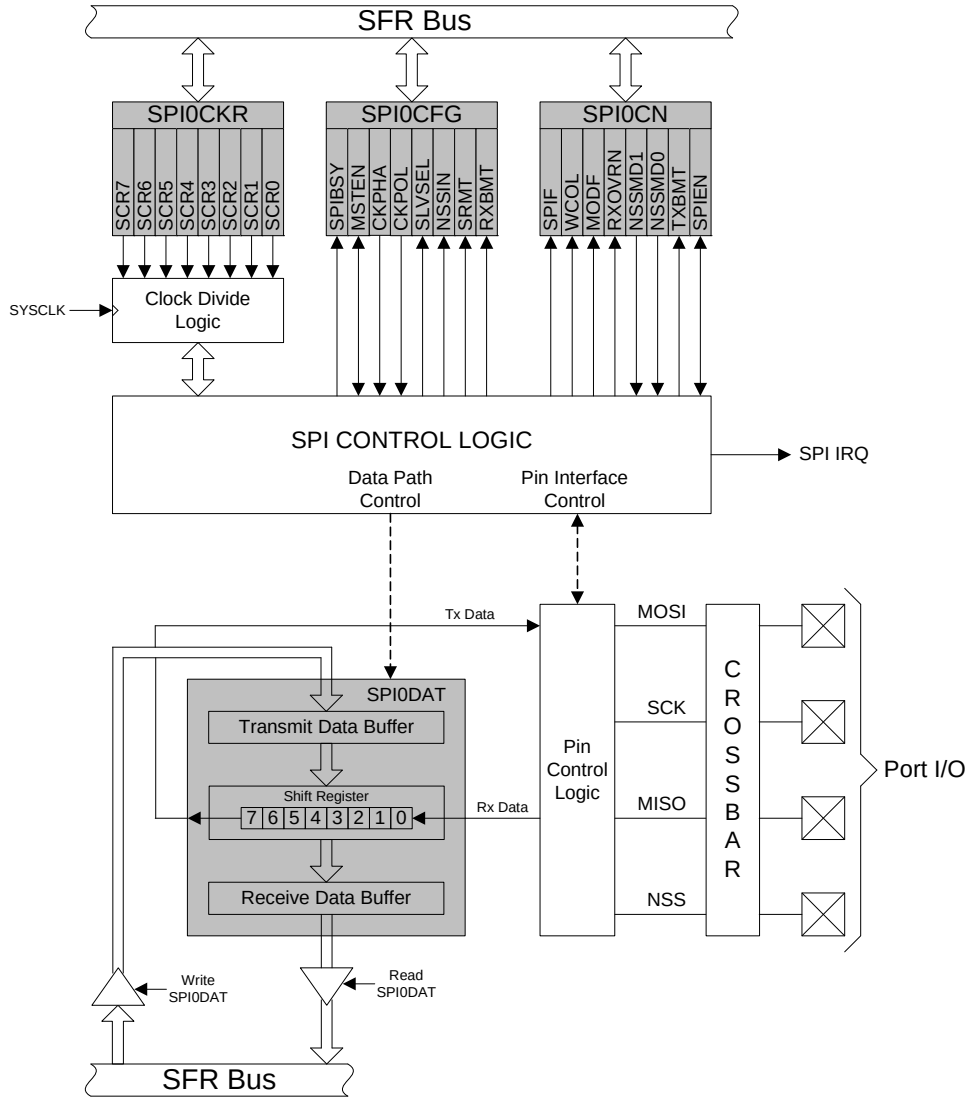

Figure 30.1. SPI Block Diagram

32.1. Timer 0 and Timer 1

Each timer is implemented as a 16-bit register accessed as two separate bytes: a low byte (TL0 or TL1) and a high byte (TH0 or TH1). The Counter/Timer Control register (TCON) is used to enable Timer 0 and Timer 1 as well as indicate status. Timer 0 interrupts can be enabled by setting the ET0 bit in the IE register (Section “17.5. Interrupt Register Descriptions” on page 235); Timer 1 interrupts can be enabled by setting the ET1 bit in the IE register (Section “17.5. Interrupt Register Descriptions” on page 235). Both counter/timers operate in one of four primary modes selected by setting the Mode Select bits T1M1–T0M0 in the Counter/Timer Mode register (TMOD). Each timer can be configured independently. Each operating mode is described below.

32.1.1. Mode 0: 13-bit Counter/Timer

Timer 0 and Timer 1 operate as 13-bit counter/timers in Mode 0. The following describes the configuration and operation of Timer 0. However, both timers operate identically, and Timer 1 is configured in the same manner as described for Timer 0.

The TH0 register holds the eight MSBs of the 13-bit counter/timer. TL0 holds the five LSBs in bit positions TL0.4–TL0.0. The three upper bits of TL0 (TL0.7–TL0.5) are indeterminate and should be masked out or ignored when reading. As the 13-bit timer register increments and overflows from 0x1FFF (all ones) to 0x0000, the timer overflow flag TF0 (TCON.5) is set and an interrupt will occur if Timer 0 interrupts are enabled.

The C/T0 bit (TMOD.2) selects the counter/timer's clock source. When C/T0 is set to logic 1, high-to-low transitions at the selected Timer 0 input pin (T0) increment the timer register (Refer to Section “27.3. Priority Crossbar Decoder” on page 355 for information on selecting and configuring external I/O pins). Clearing C/T selects the clock defined by the T0M bit (CKCON.3). When T0M is set, Timer 0 is clocked by the system clock. When T0M is cleared, Timer 0 is clocked by the source selected by the Clock Scale bits in CKCON (see SFR Definition 32.1).

Setting the TR0 bit (TCON.4) enables the timer when either GATE0 (TMOD.3) is logic 0 or the input signal $\overline{\text{INT0}}$ is active as defined by bit IN0PL in register IT01CF (see SFR Definition 17.7). Setting GATE0 to 1 allows the timer to be controlled by the external input signal $\overline{\text{INT0}}$ (see Section “17.5. Interrupt Register Descriptions” on page 235), facilitating pulse width measurements

Table 32.1. Timer 0 Running Modes

TR0	GATE0	$\overline{\text{INT0}}$	Counter/Timer
0	X	X	Disabled
1	0	X	Enabled
1	1	0	Disabled
1	1	1	Enabled
Note: X = Don't Care			

Setting TR0 does not force the timer to reset. The timer registers should be loaded with the desired initial value before the timer is enabled.

TL1 and TH1 form the 13-bit register for Timer 1 in the same manner as described above for TL0 and TH0. Timer 1 is configured and controlled using the relevant TCON and TMOD bits just as with Timer 0. The input signal $\overline{\text{INT1}}$ is used with Timer 1; the $\overline{\text{INT1}}$ polarity is defined by bit IN1PL in register IT01CF (see SFR Definition 17.7).

Table 33.2. PCA0CPM and PCA0PWM Bit Settings for PCA Capture/Compare Modules

Operational Mode	PCA0CPMn								PCA0PWM				
Software Timer	X	C	0	0	1	0	0	A	0	X	B	XXX	XX
High Speed Output	X	C	0	0	1	1	0	A	0	X	B	XXX	XX
Frequency Output	X	C	0	0	0	1	1	A	0	X	B	XXX	XX
8-Bit Pulse Width Modulator (Note 7)	0	C	0	0	E	0	1	A	0	X	B	XXX	00
9-Bit Pulse Width Modulator (Note 7)	0	C	0	0	E	0	1	A	D	X	B	XXX	01
10-Bit Pulse Width Modulator (Note 7)	0	C	0	0	E	0	1	A	D	X	B	XXX	10
11-Bit Pulse Width Modulator (Note 7)	0	C	0	0	E	0	1	A	D	X	B	XXX	11
16-Bit Pulse Width Modulator	1	C	0	0	E	0	1	A	0	X	B	XXX	XX

Notes:
1. X = Don't Care (no functional difference for individual module if 1 or 0).
2. A = Enable interrupts for this module (PCA interrupt triggered on CCFn set to 1).
3. B = Enable 8th, 9th, 10th or 11th bit overflow interrupt (Depends on setting of CLSEL[1:0]).
4. C = When set to 0, the digital comparator is off. For high speed and frequency output modes, the associated pin will not toggle. In any of the PWM modes, this generates a 0% duty cycle (output = 0).
5. D = Selects whether the Capture/Compare register (0) or the Auto-Reload register (1) for the associated channel is accessed via addresses PCA0CPHn and PCA0CPLn.
6. E = When set, a match event will cause the CCFn flag for the associated channel to be set.
7. All modules set to 8, 9, 10 or 11-bit PWM mode use the same cycle length setting.

33.3.1. Edge-triggered Capture Mode

In this mode, a valid transition on the CEXn pin causes the PCA to capture the value of the PCA counter/timer and load it into the corresponding module's 16-bit capture/compare register (PCA0CPLn and PCA0CPHn). The CAPPn and CAPNn bits in the PCA0CPMn register are used to select the type of transition that triggers the capture: low-to-high transition (positive edge), high-to-low transition (negative edge), or either transition (positive or negative edge). When a capture occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. If both CAPPn and CAPNn bits are set to logic 1, then the state of the Port pin associated with CEXn can be read directly to determine whether a rising-edge or falling-edge caused the capture.

C2 Register Definition 34.4. FPCTL: C2 Flash Programming Control

Bit	7	6	5	4	3	2	1	0
Name	FPCTL[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

C2 Address: 0x02

Bit	Name	Function
7:0	FPCTL[7:0]	**Flash Programming Control Register.** This register is used to enable Flash programming via the C2 interface. To enable C2 Flash programming, the following codes must be written in order: 0x02, 0x01. Note that once C2 Flash programming is enabled, a system reset must be issued to resume normal operation.

C2 Register Definition 34.5. FPDAT: C2 Flash Programming Data

Bit	7	6	5	4	3	2	1	0
Name	FPDAT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

C2 Address: 0xB4

Bit	Name	Function	
7:0	FPDAT[7:0]	**C2 Flash Programming Data Register.** This register is used to pass Flash commands, addresses, and data during C2 Flash accesses. Valid commands are listed below.	
		Code	**Command**
		0x06	Flash Block Read
		0x07	Flash Block Write
		0x08	Flash Page Erase
		0x03	Device Erase

Document Change List

Revision 0.1 to Revision 0.2

- Added new content to DC0 chapter.
- Reordered chapters.
- Corrections to SFR tables.
- Updated Electrical Specifications.

Revision 0.2 to Revision 0.3

- Added new content to DMA0, CRC1, ENC0, SPI1, and Pulse Counter chapters.
- Added TQFP-80 package variant.
- Added package drawings and landing diagram for TQFP-80 package.
- Added via placement recommendations for DQFN-76 package.
- Updated electrical specifications.
- Corrections to SFR tables.
- Fixed inconsistencies in SFR names.
- Fixed inconsistencies in acronyms and terminology.

Revision 0.3 to Revision 0.5

- Updated maximum IBAT current using precision oscillator in Table 4.4.
- Updated sleep currents in Table 4.4.
- Added Note 1 to Table 4.6.
- Deleted SFR Page Stack Example in Special Function Registers chapter.
- Change description of SFRPGEN bit in SFRPGCN SFR definition.
- Added paragraph to Flash chapter to explain lock byte behavior on 128 kB devices.
- Corrected SFRPAGE in SPI1 SFR definitions 32.1/2/3.

Revision 0.5 to Revision 1.0

- Changed revision in ordering information from A to B.
- Fixed inconsistencies in VIORF pin definitions.
- Added note about IFBANK usage.
- Updated Table 4.4 Digital Supply Current—Sleep Mode (LCD disabled, RTC disabled) 3.6 V, 25 °C maximum to 0.23 µA.
- Fixed inconsistencies in description of reset behavior.
- Added encryption/decryption times to SFR Definition 14.1.
- Fixed inconsistencies in SFR Definition 14.2.
- Fixed inconsistencies in Port P2 through P7 SFR Definitions.
- All TBD specifications have been determined.