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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, LCD, POR, PWM, WDT
Number of I/O	57
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.8V
Data Converters	A/D 16x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f968-b-gq

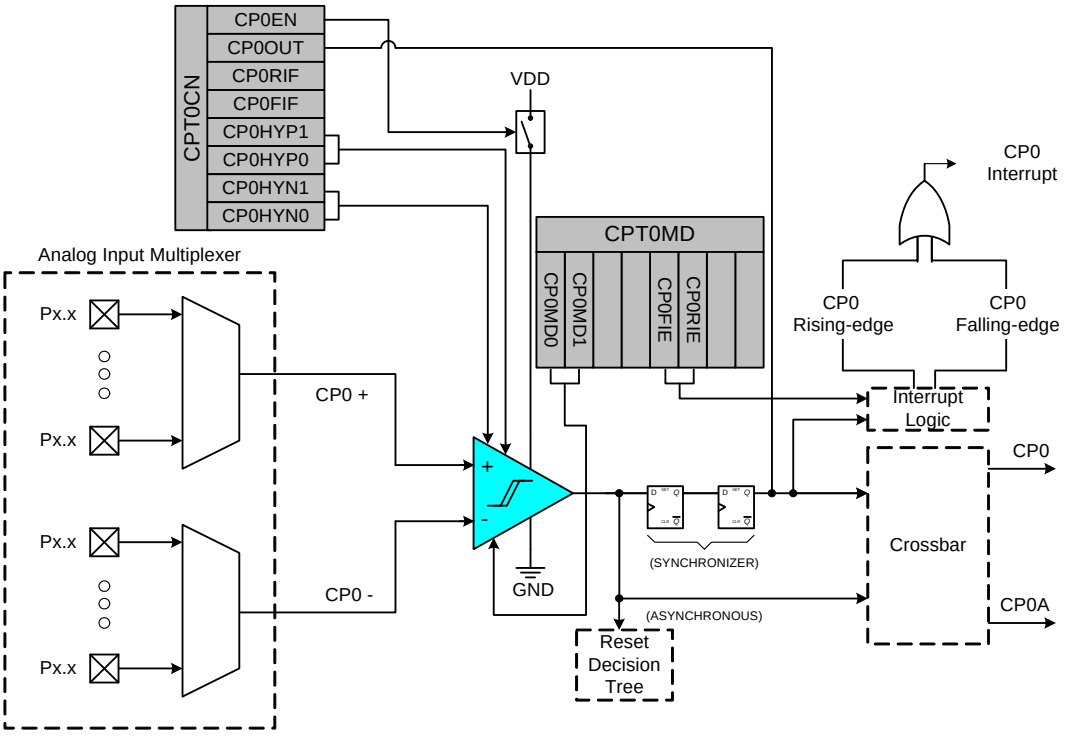

Figure 1.15. Comparator 0 Functional Block Diagram

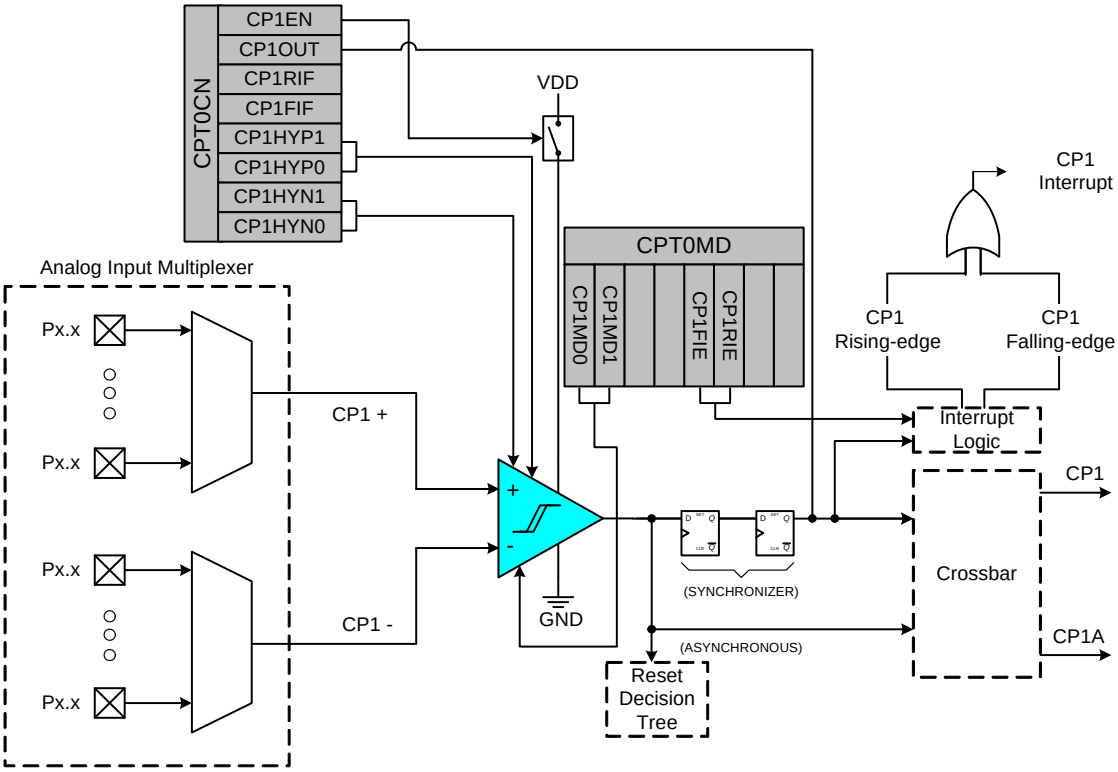

Figure 1.16. Comparator 1 Functional Block Diagram

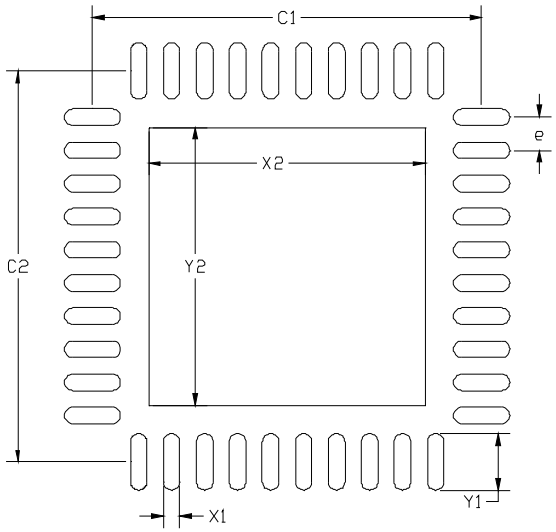

Figure 3.8. QFN-40 Landing Diagram

Table 3.6. QFN-40 Landing Diagram Dimensions

Dimension	Min	Max	Dimension	Min	Max
C1	5.80	5.90	X2	4.10	4.20
C2	5.80	5.90	Y1	0.75	0.85
e	0.50 BSC		Y2	4.10	4.20
X1	0.15	0.25			

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimension and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-SM-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
9. A 4x4 array of 0.80 mm square openings on a 1.05 mm pitch should be used for the center ground pad.

Card Assembly

10. A No-Clean, Type-3 solder paste is recommended.
11. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

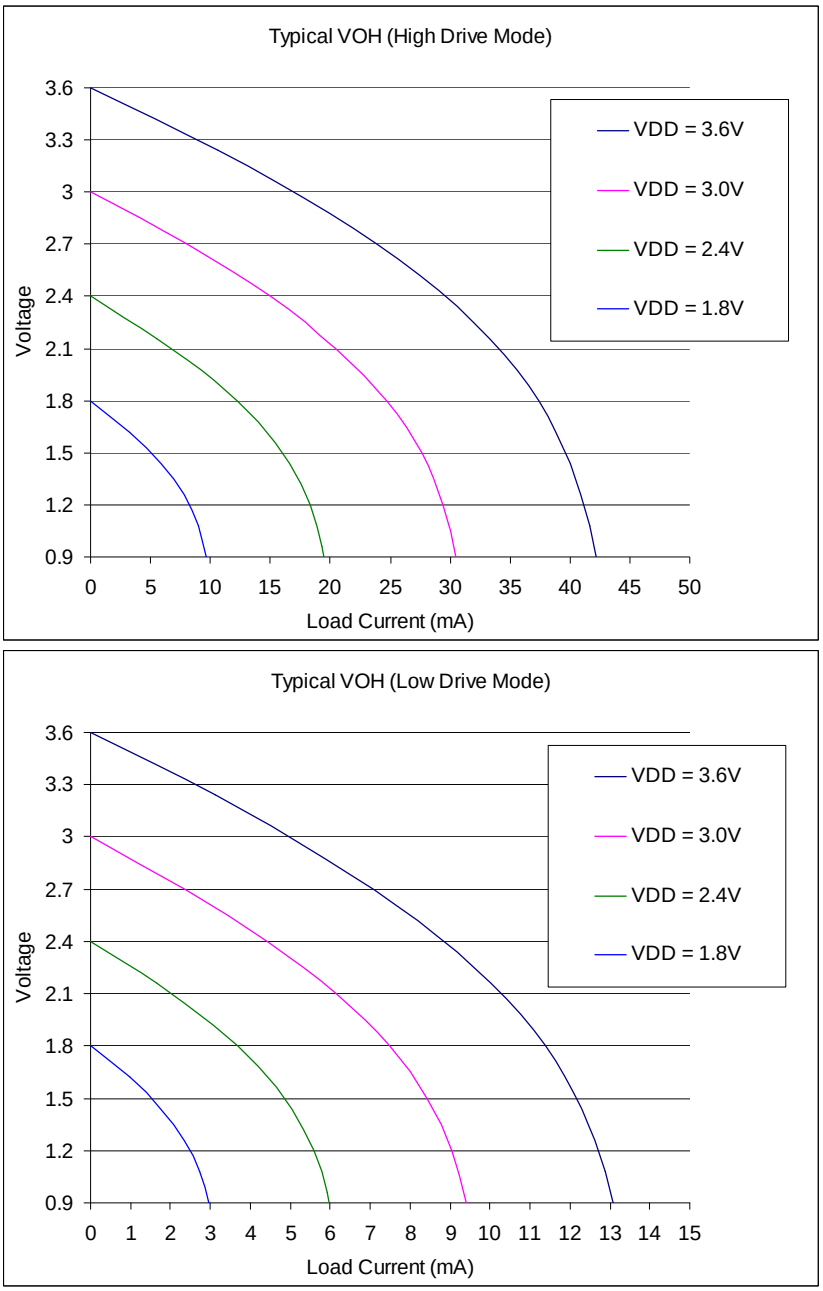

Figure 4.2. Typical VOH Curves, 1.8–3.6 V

SFR Definition 6.2. IREF0CF: Current Reference Configuration

Bit	7	6	5	4	3	2	1	0
Name	PWMEN					PWMSS[2:0]		
Type	R/W	R/W	R/W	R/W	R/W	R/W		
Reset	0	0	0	0	0	0	0	0

SFR Page = 0xF; SFR Address = 0xB9

Bit	Name	Function
7	PWMEN	**PWM Enhanced Mode Enable.** Enables the PWM Enhanced Mode. 0: PWM Enhanced Mode disabled. 1: PWM Enhanced Mode enabled.
6:3	Unused	Read = 0000b, Write = don't care.
2:0	PWMSS[2:0]	**PWM Source Select.** Selects the PCA channel to use for the fine-tuning control signal. 000: CEX0 selected as fine-tuning control signal. 001: CEX1 selected as fine-tuning control signal. 010: CEX2 selected as fine-tuning control signal. 011: CEX3 selected as fine-tuning control signal. 100: CEX4 selected as fine-tuning control signal. 101: CEX5 selected as fine tuning control signal. All Other Values: Reserved.

6.2. IREF0 Specifications

See Table 4.15 on page 73 for a detailed listing of IREF0 specifications.

10.2. Configuring the External Memory Interface

Configuring the External Memory Interface consists of five steps:

1. Configure the Output Modes of the associated port pins as either push-pull or open-drain (push-pull is most common). The Input Mode of the associated port pins should be set to digital (reset value).
2. Configure Port latches to “park” the EMIF pins in a dormant state (usually by setting them to logic 1).
3. Select Multiplexed mode or Non-multiplexed mode.
4. Select the memory mode (on-chip only, split mode without bank select, split mode with bank select, or off-chip only).
5. Set up timing to interface with off-chip memory or peripherals.

Each of these five steps is explained in detail in the following sections. The Port selection, Multiplexed mode selection, and Mode bits are located in the EMI0CF register shown in SFR Definition .

10.3. Port Configuration

The External Memory Interface appears on Ports 3, 4, 5, and 6 when it is used for off-chip memory access. The external memory interface and the LCD cannot be used simultaneously. When using EMIF, all pins on Port 3-6 may only be used for EMIF purposes or as general purpose I/O. The EMIF pinout is shown in Table 10.1 on page 131.

The External Memory Interface claims the associated Port pins for memory operations ONLY during the execution of an off-chip MOVX instruction. Once the MOVX instruction has completed, control of the Port pins reverts to the Port latches or to the Crossbar settings for those pins. See Section “27. Port Input/Output” on page 351 for more information about the Crossbar and Port operation and configuration. **The Port latches should be explicitly configured to “park” the External Memory Interface pins in a dormant state, most commonly by setting them to a logic 1**.

During the execution of the MOVX instruction, the External Memory Interface will explicitly disable the drivers on all Port pins that are acting as Inputs (Data[7:0] during a READ operation, for example). The Output mode of the Port pins (whether the pin is configured as Open-Drain or Push-Pull) is unaffected by the External Memory Interface operation, and remains controlled by the PnMDOUT registers. In most cases, the output modes of all EMIF pins should be configured for push-pull mode.

The C8051F960/2/4/6/8 devices support both the multiplexed and non-multiplexed modes. Accessing off-chip memory is not supported by the C8051F961/3/5/7/9 devices.

SFR Definition 11.1. DMA0EN: DMA0 Channel Enable

Bit	7	6	5	4	3	2	1	0
Name		CH6_EN	CH5_EN	CH4_EN	CH3_EN	CH2_EN	CH1_EN	CH0_EN
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x2; SFR Address = 0xD2

Bit	Name	Function
7	Unused	Read = 0b, Write = Don't Care
6	CH6_EN	**Channel 6 Enable.** 0: Disable DMA0 channel 6. 1: Enable DMA0 channel 6.
5	CH5_EN	**Channel 5 Enable.** 0: Disable DMA0 channel 5. 1: Enable DMA0 channel 5.
4	CH4_EN	**Channel 4 Enable.** 0: Disable DMA0 channel 4. 1: Enable DMA0 channel 4.
3	CH3_EN	**Channel 3 Enable.** 0: Disable DMA0 channel 3. 1: Enable DMA0 channel 3.
2	CH2_EN	**Channel 2 Enable.** 0: Disable DMA0 channel 2. 1: Enable DMA0 channel 2.
1	CH1_EN	**Channel 1 Enable.** 0: Disable DMA0 channel 1. 1: Enable DMA0 channel 1.
0	CH0_EN	**Channel 0 Enable.** 0: Disable DMA0 channel 0. 1: Enable DMA0 channel 0.

13.2. Endianness

The CRC1 module is optimized to process big endian data. Data written to the CRC1IN SFR should be in the normal bit order with the most significant bit stored in bit 7 and the least significant bit stored in bit 0. The input data is shifted left into the CRC engine. The CRC1 module will process one byte at a time and update the results for each byte. When used with the DMA, the first byte to be written should be stored in the lowest address.

Some communications systems may transmit data least significant bit first and may require calculation of a CRC in the transmission bit order. In this case, the bits must be flipped, using the CRC0FLIP SFR, before writing to the CRC1IN SFR. The final 16-bit result may be flipped using the flip bit in the CRC1CN SFR. Note that the polynomial is always written in big endian bit order.

14.4. AES Block Cipher Data Flow

The AES0 module data flow for AES Block Cipher encryption and decryption shown in Figure 14.3. The data flow is the same for encryption and decryption. The AES0DCF sfr is always configured to route the AES core output to AES0YOUT. The XOR on the input and output paths are not used.

For an encryption operation, the core is configured for an encryption cipher, the encryption key is written to AES0KIN, the plaintext is written to the AES0BIN sfr. and the ciphertext is read from AES0YOUT.

For a decryption operation, the core is configured for an decryption cipher, the decryption key is written to AES0KIN, the ciphertext is written to the AES0BIN sfr. and the plaintext is read from AES0YOUT.

The key size is set to the desired key size.

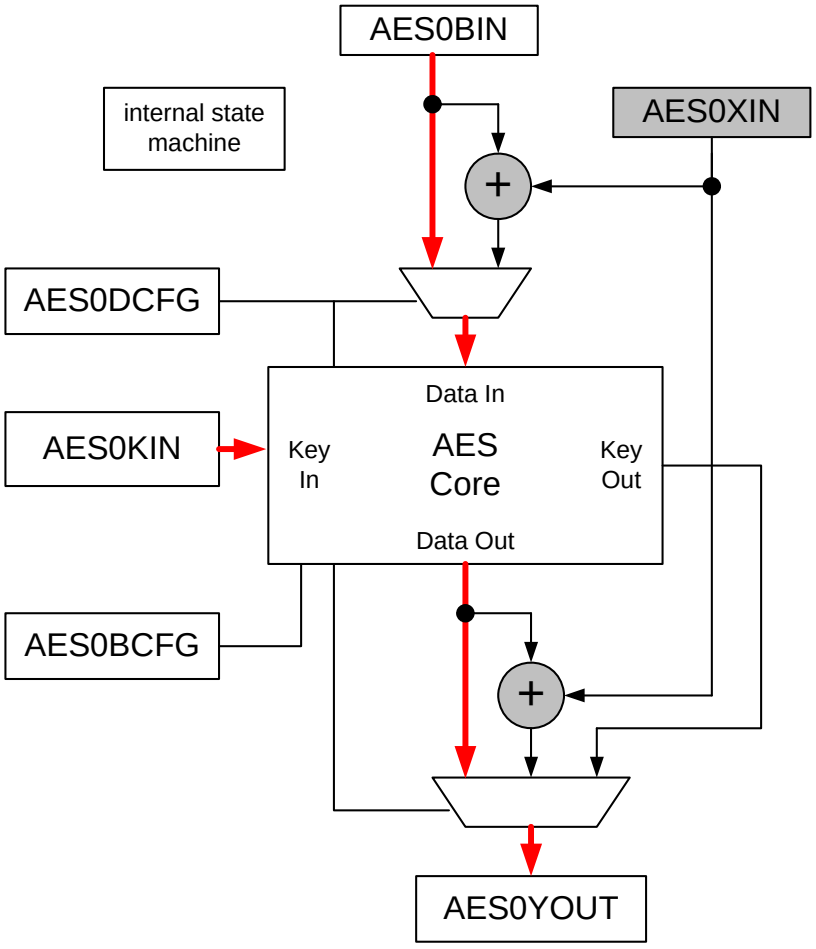

Figure 14.3. AES Block Cipher Data Flow

Table 16.1. SFR Map (0xC0–0xFF)

Addr.	Page	0(8)	1(9)	2(A)	3(B)	4(C)	5(D)	6(E)	7(F)
0xF8	0x0	SPI0CN	PCA0L	PCA0H	PCA0CPL0	PCA0CPH0	PCA0CPL4	PCA0CPH4	VDM0CN
	0x2	SPI1CN	PC0DCL	PC0DCH	PC0INT0	PC0INT1	DC0RDY		
	0xF		P4MDOUT	P5MDOUT	P6MDOUT	P7MDOUT	CLKMODE	PCLKEN	
0xF0	0x0		P0MDIN	P1MDIN	P2MDIN	SMB0ADR	SMB0ADM	EIP1	EIP2
	0x2		PC0CMP1L	PC0CMP1M	PC0CMP1H	PC0HIST	AES0YOUT		
	0xF		P3MDIN	P4MDIN	P5MDIN	P6MDIN	PCLKACT		
0xE8	0x0	ADC0CN	PCA0CPL1	PCA0CPH1	PCA0CPL2	PCA0CPH2	PCA0CPL3	PCA0CPH3	RSTSRC
	0x2		AES0BCFG	AES0DCFG	AES0BIN	AES0XIN	AES0KIN		
	0xF		DEVICEID	REVID					
0xE0	0x0	ACC	XBR0	XBR1	XBR2	IT01CF		EIE1	EIE2
	0x2		PC0CMP0L	PC0CMP0M	PC0CMP0H	PC0TH			
	0xF		XBR0	XBR1	XBR2	IT01CF			
0xD8	0x0	PCA0CN	PCA0MD	PCA0CPM0	PCA0CPM1	PCA0CPM2	PCA0CPM3	PCA0CPM4	PCA0PWM
	0x2		PC0MD	PC0CTR0L	PC0TRML	PC0CTR0H	PC0CTR1L	PC0TRMH	PC0CTR1H
	0xF		P4	P5	P6	P7			
0xD0	0x0	PSW	REF0CN	PCA0CPL5	PCA0CPH5	P0SKIP	P1SKIP	P2SKIP	P0MAT
	0x2		DMA0SEL	DMA0EN	DMA0INT	DMA0MINT	DMA0BUSY	DMA0NMD	PC0PCF
	0xF								
0xC8	0x0	TMR2CN	REG0CN	TMR2RLL	TMR2RLH	TMR2L	TMR2H	PCA0CPM5	P1MAT
	0x2		DMA0NCF	DMA0NBAL	DMA0NBAH	DMA0NAOL	DMA0NAOH	DMA0NSZL	DMA0NSZH
	0xF								
0xC0	0x0	SMB0CN	SMB0CF	SMB0DAT	ADC0GTL	ADC0GTH	ADC0LTL	ADC0LTH	P0MASK
	0x2		PC0STAT	ENC0L	ENC0M	ENC0H	ENC0CN	VREGINSDL	VREGINSDH
	0xF								

of an inadvertent write to the PCON register. If this behavior is not desired, the WDT may be disabled by software prior to entering the idle mode if the WDT was initially configured to allow this operation. This provides the opportunity for additional power savings, allowing the system to remain in the Idle mode indefinitely, waiting for an external stimulus to wake up the system. Refer to Section “22.6. PCA Watchdog Timer Reset” on page 283 for more information on the use and configuration of the WDT.

19.3. Stop Mode

Setting the Stop Mode Select bit (PCON.1) causes the CIP-51 to enter Stop mode as soon as the instruction that sets the bit completes execution. In Stop mode the precision internal oscillator and CPU are stopped; the state of the low power oscillator and the external oscillator circuit is not affected. Each analog peripheral (including the external oscillator circuit) may be shut down individually prior to entering Stop Mode. Stop mode can only be terminated by an internal or external reset. On reset, the CIP-51 performs the normal reset sequence and begins program execution at address 0x0000.

If enabled, the Missing Clock Detector will cause an internal reset and thereby terminate the Stop mode. The Missing Clock Detector should be disabled if the CPU is to be put to in STOP mode for longer than the MCD timeout.

Stop Mode is a legacy 8051 power mode; it will not result in optimal power savings. Sleep, Suspend, or Low Power Idle mode will provide more power savings if the MCU needs to be inactive for a long period of time.

19.4. Low Power Idle Mode

Low Power Idle Mode uses clock gating to reduce the supply current when the device is placed in Idle mode. This mode is enabled by configuring the clock tree gates using the PCLKEN register, setting the LPMEN bit in the CLKMODE register, and placing the device in Idle mode. The clock is automatically gated from the CPU upon entry into Idle mode when the LPMEN bit is set. This mode provides substantial power savings over the standard Idle Mode especially at high system clock frequencies.

The clock gating logic may also be used to reduce power when executing code. Low Power Active Mode is enabled by configuring the PCLKACT and PCLKEN registers, then setting the LPMEN bit. The PCLKACT register provides the ability to override the PCLKEN setting to force a clock to certain peripherals in Low Power Active mode. If the PCLKACT register is left at its default value, then PCLKEN determines which perpherals will be clocked in this mode. The CPU is always clocked in Low Power Active Mode.

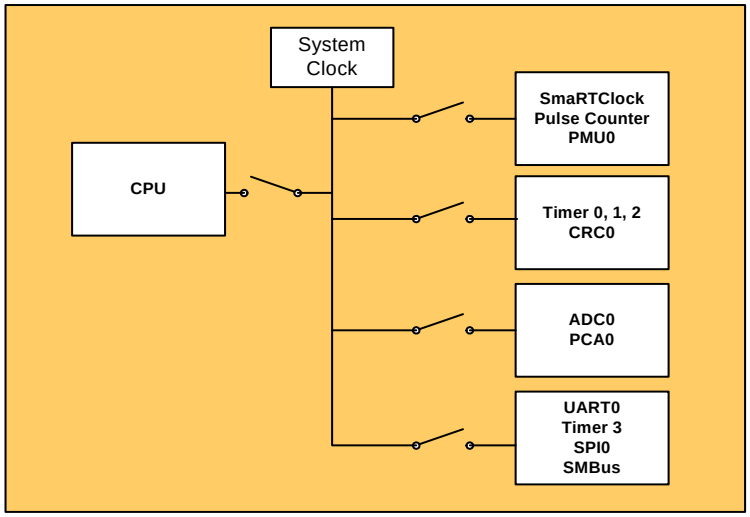

Figure 19.2. Clock Tree Distribution

23.4. Special Function Registers for Selecting and Configuring the System Clock

The clocking sources on C8051F96x devices are enabled and configured using the OSCICN, OSCICL, OSCXCN and the SmaRTClock internal registers. See Section “24. SmaRTClock (Real Time Clock)” on page 295 for SmaRTClock register descriptions. The system clock source for the MCU can be selected using the CLKSEL register. To minimize active mode current, the oneshot timer which sets Flash read time should by bypassed when the system clock is greater than 10 MHz. See the FLSCL register description for details.

The clock selected as the system clock can be divided by 1, 2, 4, 8, 16, 32, 64, or 128. When switching between two clock divide values, the transition may take up to 128 cycles of the undivided clock source. The CLKRDY flag can be polled to determine when the new clock divide value has been applied. The clock divider must be set to "divide by 1" when entering Suspend or Sleep Mode.

The system clock source may also be switched on-the-fly. The switchover takes effect after one clock period of the slower oscillator.

SFR Definition 23.1. CLKSEL: Clock Select

Bit	7	6	5	4	3	2	1	0
Name	CLKRDY	CLKDIV[2:0]				CLKSEL[2:0]		
Type	R	R/W			R/W	R/W		
Reset	0	0	0	1	0	0	1	0

SFR Page = All Pages; SFR Address = 0xA9

Bit	Name	Function
7	CLKRDY	**System Clock Divider Clock Ready Flag.** 0: The selected clock divide setting has not been applied to the system clock. 1: The selected clock divide setting has been applied to the system clock.
6:4	CLKDIV[2:0]	**System Clock Divider Bits.** Selects the clock division to be applied to the undivided system clock source. 000: System clock is divided by 1. 001: System clock is divided by 2. 010: System clock is divided by 4. 011: System clock is divided by 8. 100: System clock is divided by 16. 101: System clock is divided by 32. 110: System clock is divided by 64. 111: System clock is divided by 128.
3	Unused	Read = 0b. Must Write 0b.
2:0	CLKSEL[2:0]	**System Clock Select.** Selects the oscillator to be used as the undivided system clock source. 000: Precision Internal Oscillator. 001: External Oscillator. 010: Low Power Oscillator divided by 8. 011: SmaRTClock Oscillator. 100: Low Power Oscillator. All other values reserved.

SFR Definition 26.14. LCD0CHPCF: LCD0 Charge Pump Configuration

Bit	7	6	5	4	3	2	1	0
Name								
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	1	0	0	0	0	0

SFR Page = 0x2; SFR Address = 0xAD

Bit	Name	Function
7:0	Reserved	Must write 0x60.

SFR Definition 26.15. LCD0CHPMD: LCD0 Charge Pump Mode

Bit	7	6	5	4	3	2	1	0
Name								
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	0	1	0	0	1

SFR Page = 0x2; SFR Address = 0xAE

Bit	Name	Function
7:0	Reserved	Must write 0xE9.

SFR Definition 26.16. LCD0BUFCN: LCD0 Buffer Control

Bit	7	6	5	4	3	2	1	0
Name								
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	1	0	0	0	1	0	0

SFR Page = 0xF; SFR Address = 0x9C

Bit	Name	Function
7:0	Reserved	Must write 0x44.

All transactions are initiated by a master, with one or more addressed slave devices as the target. The master generates the START condition and then transmits the slave address and direction bit. If the transaction is a WRITE operation from the master to the slave, the master transmits the data a byte at a time waiting for an ACK from the slave at the end of each byte. For READ operations, the slave transmits the data waiting for an ACK from the master at the end of each byte. At the end of the data transfer, the master generates a STOP condition to terminate the transaction and free the bus. Figure 28.3 illustrates a typical SMBus transaction.

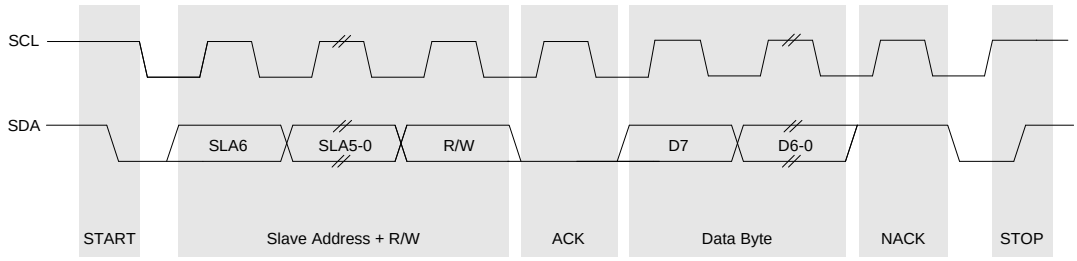

Figure 28.3. SMBus Transaction

28.3.1. Transmitter Vs. Receiver

On the SMBus communications interface, a device is the “transmitter” when it is sending an address or data byte to another device on the bus. A device is a “receiver” when an address or data byte is being sent to it from another device on the bus. The transmitter controls the SDA line during the address or data byte. After each byte of address or data information is sent by the transmitter, the receiver sends an ACK or NACK bit during the ACK phase of the transfer, during which time the receiver controls the SDA line.

28.3.2. Arbitration

A master may start a transfer only if the bus is free. The bus is free after a STOP condition or after the SCL and SDA lines remain high for a specified time (see Section “28.3.5. SCL High (SMBus Free) Timeout” on page 384). In the event that two or more devices attempt to begin a transfer at the same time, an arbitration scheme is employed to force one master to give up the bus. The master devices continue transmitting until one attempts a HIGH while the other transmits a LOW. Since the bus is open-drain, the bus will be pulled LOW. The master attempting the HIGH will detect a LOW SDA and lose the arbitration. The winning master continues its transmission without interruption; the losing master becomes a slave and receives the rest of the transfer if addressed. This arbitration scheme is non-destructive: one device always wins, and no data is lost.

28.3.3. Clock Low Extension

SMBus provides a clock synchronization mechanism, similar to I^2C, which allows devices with different speed capabilities to coexist on the bus. A clock-low extension is used during a transfer in order to allow slower slave devices to communicate with faster masters. The slave may temporarily hold the SCL line LOW to extend the clock low period, effectively decreasing the serial clock frequency.

28.3.4. SCL Low Timeout

If the SCL line is held low by a slave device on the bus, no further communication is possible. Furthermore, the master cannot force the SCL line high to correct the error condition. To solve this problem, the SMBus protocol specifies that devices participating in a transfer must detect any clock cycle held low longer than 25 ms as a “timeout” condition. Devices that have detected the timeout condition must reset the communication no later than 10 ms after detecting the timeout condition.

When the SMBTOE bit in SMB0CF is set, Timer 3 is used to detect SCL low timeouts. Timer 3 is forced to reload when SCL is high, and allowed to count when SCL is low. With Timer 3 enabled and configured to

Table 28.3. Sources for Hardware Changes to SMB0CN

Bit	Set by Hardware When:	Cleared by Hardware When:
MASTER	• A START is generated.	• A STOP is generated. • Arbitration is lost.
TXMODE	• START is generated. • SMB0DAT is written before the start of an SMBus frame.	• A START is detected. • Arbitration is lost. • SMB0DAT is not written before the start of an SMBus frame.
STA	• A START followed by an address byte is received.	• Must be cleared by software.
STO	• A STOP is detected while addressed as a slave. • Arbitration is lost due to a detected STOP.	• A pending STOP is generated.
ACKRQ	• A byte has been received and an ACK response value is needed (only when hardware ACK is not enabled).	• After each ACK cycle.
ARBLOST	• A repeated START is detected as a MASTER when STA is low (unwanted repeated START). • SCL is sensed low while attempting to generate a STOP or repeated START condition. • SDA is sensed low while transmitting a 1 (excluding ACK bits).	• Each time SI is cleared.
ACK	• The incoming ACK value is low (ACKNOWLEDGE).	• The incoming ACK value is high (NOT ACKNOWLEDGE).
SI	• A START has been generated. • Lost arbitration. • A byte has been transmitted and an ACK/NACK received. • A byte has been received. • A START or repeated START followed by a slave address + R/W has been received. • A STOP has been received.	• Must be cleared by software.

28.4.3. Hardware Slave Address Recognition

The SMBus hardware has the capability to automatically recognize incoming slave addresses and send an ACK without software intervention. Automatic slave address recognition is enabled by setting the EHACK bit in register SMB0ADM to 1. This will enable both automatic slave address recognition and automatic hardware ACK generation for received bytes (as a master or slave). More detail on automatic hardware ACK generation can be found in Section 28.4.2.2.

The registers used to define which address(es) are recognized by the hardware are the SMBus Slave Address register (SFR Definition 28.3) and the SMBus Slave Address Mask register (SFR Definition 28.4). A single address or range of addresses (including the General Call Address 0x00) can be specified using these two registers. The most-significant seven bits of the two registers are used to define which addresses will be ACKed. A 1 in bit positions of the slave address mask SLVM[6:0] enable a comparison between the received slave address and the hardware's slave address SLV[6:0] for those bits. A 0 in a bit of the slave address mask means that bit will be treated as a "don't care" for comparison purposes. In this case, either a 1 or a 0 value are acceptable on the incoming slave address. Additionally, if the GC bit in register SMB0ADR is set to 1, hardware will recognize the General Call Address (0x00). Table 28.4 shows some example parameter settings and the slave addresses that will be recognized by hardware under those conditions.

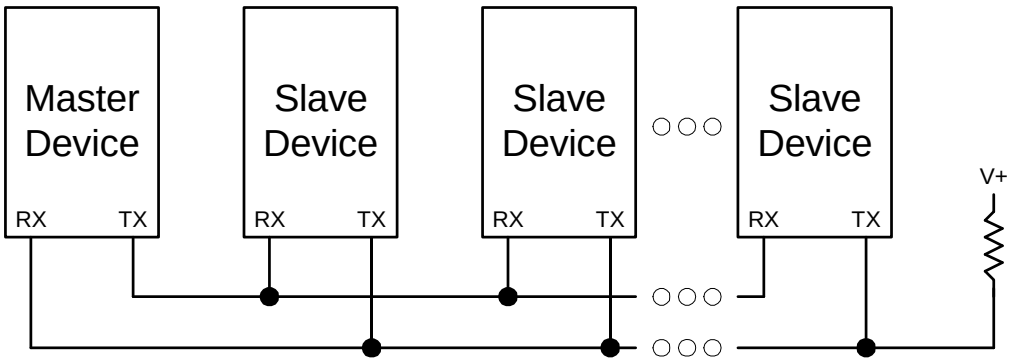

Figure 29.6. UART Multi-Processor Mode Interconnect Diagram

SFR Definition 30.3. SPI0CKR: SPI0 Clock Rate

Bit	7	6	5	4	3	2	1	0
Name	SCR[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xA2

Bit	Name	Function
7:0	SCR[7:0]	**SPI0 Clock Rate.** These bits determine the frequency of the SCK output when the SPI0 module is configured for master mode operation. The SCK clock frequency is a divided version of the system clock, and is given in the following equation, where *SYSCLK* is the system clock frequency and *SPI0CKR* is the 8-bit value held in the SPI0CKR register. $f_{SCK} = \frac{SYSCLK}{2 \times (SPI0CKR[7:0] + 1)}$ for 0 <= SPI0CKR <= 255 Example: If SYSCLK = 2 MHz and SPI0CKR = 0x04, $f_{SCK} = \frac{2000000}{2 \times (4 + 1)}$ $f_{SCK} = 200kHz$

SFR Definition 30.4. SPI0DAT: SPI0 Data

Bit	7	6	5	4	3	2	1	0
Name	SPI0DAT[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Page = 0x0; SFR Address = 0xA3

Bit	Name	Function
7:0	SPI0DAT[7:0]	**SPI0 Transmit and Receive Data.** The SPI0DAT register is used to transmit and receive SPI0 data. Writing data to SPI0DAT places the data into the transmit buffer and initiates a transfer when in Master Mode. A read of SPI0DAT returns the contents of the receive buffer.

31.3. SPI1 Slave Mode Operation

When SPI1 is enabled and not configured as a master, it will operate as a SPI slave. As a slave, bytes are shifted in through the MOSI pin and out through the MISO pin by a master device controlling the SCK signal. A bit counter in the SPI1 logic counts SCK edges. When 8 bits have been shifted through the shift register, the SPIF flag is set to logic 1, and the byte is copied into the receive buffer. Data is read from the receive buffer by reading SPI1DAT. A slave device cannot initiate transfers. Data to be transferred to the master device is pre-loaded into the shift register by writing to SPI1DAT. Writes to SPI1DAT are double-buffered, and are placed in the transmit buffer first. If the shift register is empty, the contents of the transmit buffer will immediately be transferred into the shift register. When the shift register already contains data, the SPI will load the shift register with the transmit buffer's contents after the last SCK edge of the next (or current) SPI transfer.

When configured as a slave, SPI1 can be configured for 4-wire or 3-wire operation. The default, 4-wire slave mode, is active when NSSMD1 (SPI1CN.3) = 0 and NSSMD0 (SPI1CN.2) = 1. In 4-wire mode, the NSS signal is routed to a port pin and configured as a digital input. SPI1 is enabled when NSS is logic 0, and disabled when NSS is logic 1. The bit counter is reset on a falling edge of NSS. Note that the NSS signal must be driven low at least 2 system clocks before the first active edge of SCK for each byte transfer. Figure 31.4 shows a connection diagram between two slave devices in 4-wire slave mode and a master device.

3-wire slave mode is active when NSSMD1 (SPI1CN.3) = 0 and NSSMD0 (SPI1CN.2) = 0. NSS is not used in this mode, and is not mapped to an external port pin through the crossbar. Since there is no way of uniquely addressing the device in 3-wire slave mode, SPI1 must be the only slave device present on the bus. It is important to note that in 3-wire slave mode there is no external means of resetting the bit counter that determines when a full byte has been received. The bit counter can only be reset by disabling and re-enabling SPI1 with the SPIEN bit. Figure 31.3 shows a connection diagram between a slave device in 3-wire slave mode and a master device.

31.4. SPI1 Interrupt Sources

When SPI1 interrupts are enabled, the following four flags will generate an interrupt when they are set to logic 1:

All of the following bits must be cleared by software.

- The SPI Interrupt Flag, SPIF (SPI1CN.7) is set to logic 1 at the end of each byte transfer. This flag can occur in all SPI1 modes.
- The Write Collision Flag, WCOL (SPI1CN.6) is set to logic 1 if a write to SPI1DAT is attempted when the transmit buffer has not been emptied to the SPI shift register. When this occurs, the write to SPI1DAT will be ignored, and the transmit buffer will not be written.This flag can occur in all SPI1 modes.
- The Mode Fault Flag MODF (SPI1CN.5) is set to logic 1 when SPI1 is configured as a master, and for multi-master mode and the NSS pin is pulled low. When a Mode Fault occurs, the MSTEN and SPIEN bits in SPI1CN are set to logic 0 to disable SPI1 and allow another master device to access the bus.
- The Receive Overrun Flag RXOVRN (SPI1CN.4) is set to logic 1 when configured as a slave, and a transfer is completed and the receive buffer still holds an unread byte from a previous transfer. The new byte is not transferred to the receive buffer, allowing the previously received data byte to be read. The data byte which caused the overrun is lost.

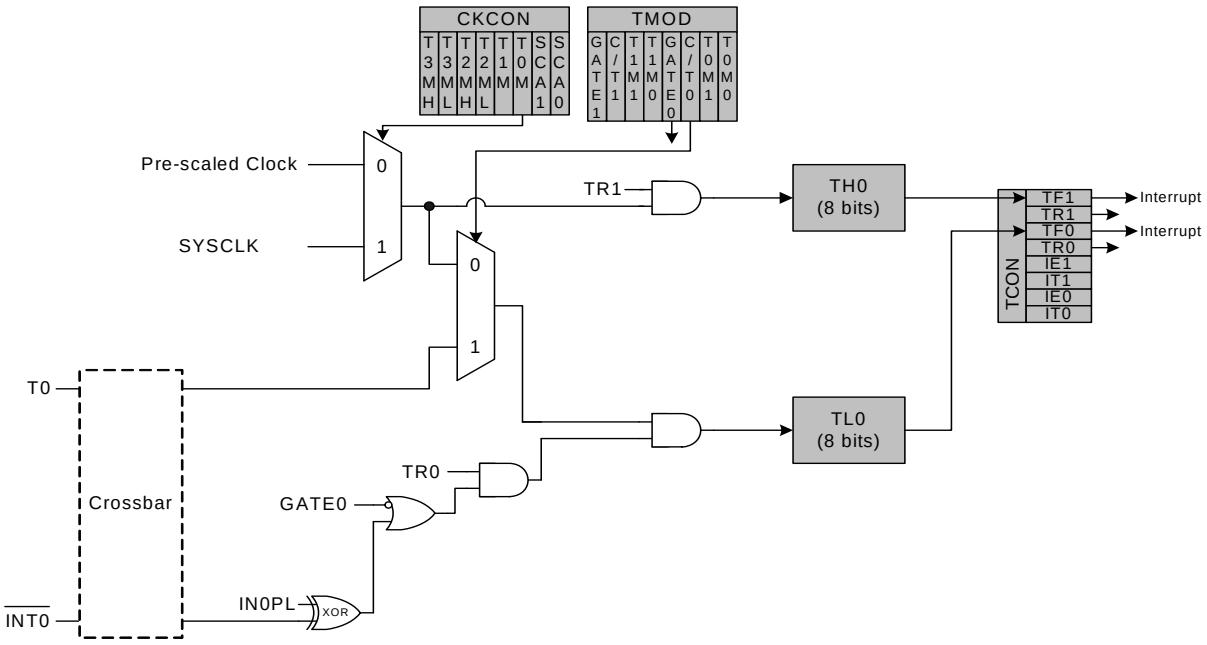

Figure 32.3. T0 Mode 3 Block Diagram

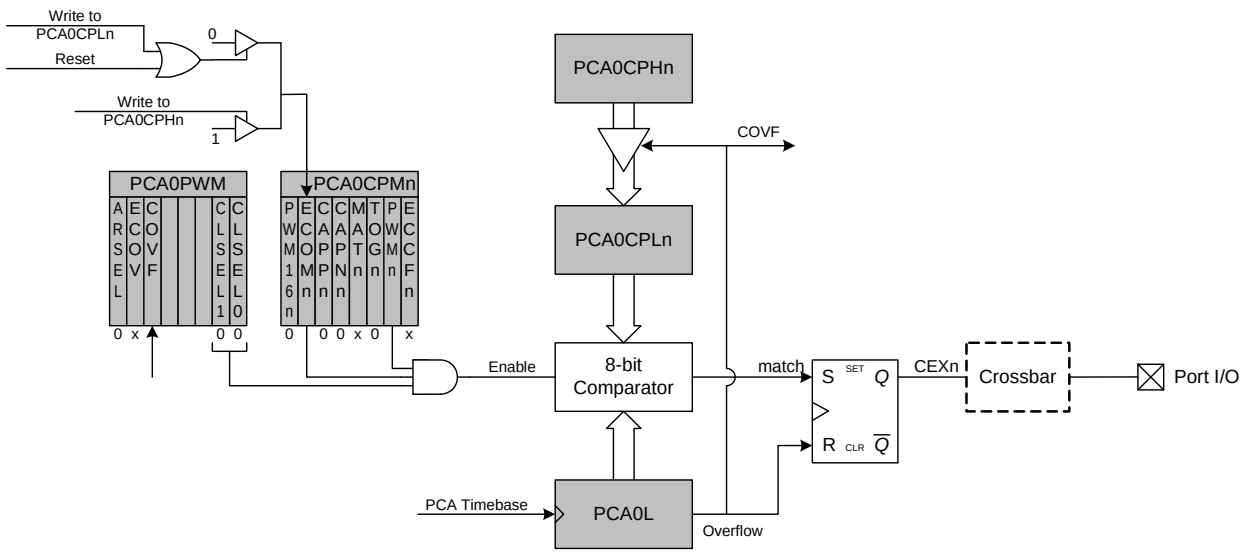

Figure 33.8. PCA 8-Bit PWM Mode Diagram

33.3.5.2. 9/10/11-bit Pulse Width Modulator Mode

The duty cycle of the PWM output signal in 9/10/11-bit PWM mode should be varied by writing to an "Auto-Reload" Register, which is dual-mapped into the PCA0CPHn and PCA0CPLn register locations. The data written to define the duty cycle should be right-justified in the registers. The auto-reload registers are accessed (read or written) when the bit ARSEL in PCA0PWM is set to 1. The capture/compare registers are accessed when ARSEL is set to 0.

When the least-significant N bits of the PCA0 counter match the value in the associated module's capture/compare register (PCA0CPn), the output on CEXn is asserted high. When the counter overflows from the Nth bit, CEXn is asserted low (see Figure 33.9). Upon an overflow from the Nth bit, the COVF flag is set, and the value stored in the module's auto-reload register is loaded into the capture/compare register. The value of N is determined by the CLSEL bits in register PCA0PWM.

The 9, 10 or 11-bit PWM mode is selected by setting the ECOMn and PWMn bits in the PCA0CPMn register, and setting the CLSEL bits in register PCA0PWM to the desired cycle length (other than 8-bits). If the MATn bit is set to 1, the CCFn flag for the module will be set each time a comparator match (rising edge) occurs. The COVF flag in PCA0PWM can be used to detect the overflow (falling edge), which will occur every 512 (9-bit), 1024 (10-bit) or 2048 (11-bit) PCA clock cycles. The duty cycle for 9/10/11-Bit PWM Mode is given in Equation 33.3, where N is the number of bits in the PWM cycle.

Important Note About PCA0CPHn and PCA0CPLn Registers: When writing a 16-bit value to the PCA0CPn registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

$$\text{Duty Cycle} = \frac{(2^N - PCA0CPn)}{2^N}$$

Equation 33.3. 9, 10, and 11-Bit PWM Duty Cycle

A 0% duty cycle may be generated by clearing the ECOMn bit to 0.