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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LVR, POR, PWM, WDT
Number of I/O	14
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.5V ~ 5.5V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/m058sfan

TABLE OF CONTENTS

1 GENERAL DESCRIPTION

The NuMicro™ M058S is a 32-bit microcontroller with embedded ARM® Cortex®-M0 core for industrial control and applications which need rich communication interfaces. The Cortex®-M0 is ARM embedded processor with 32-bit performance and cost-effective microcontroller.

The NuMicro™ M058S can run up to 50 MHz. Thus it can afford to support a variety of industrial control and applications which need high CPU performance. The NuMicro™ M058S has 32 KB flash, 4 KB data flash, 4 KB flash for the ISP, and 4 KB SRAM.

Many system level peripheral functions, such as I/O Port, Timer, UART, SPI, I^2C, PWM, ADC, Watchdog Timer, and Brown-Out Detector, have been incorporated into the NuMicro™ M058S in order to reduce component count, board space and system cost. These useful functions make the NuMicro™ M058S powerful for a wide range of applications.

Additionally, the NuMicro™ M058S is equipped with IAP (In-Application Programming), ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product.

Pin Number				Symbol	Alternate Function			Type[1]	Description
TSSOP 20	QFN 33	LQFP 48	LQFP 64		1	2	3		
7	7	10	13	P3.4	T0	SDA0		I/O	UART function use. The SDA0/SCL0 pins are for I²C0 function use. CKO: HCLK clock output The STADC pin is for ADC external trigger input. The T0/T1 pins are for Timer0/1 external event counter input. The T0EX/T1EX pins are for external capture/reset trigger input of Timer0/1.
8	8	11	14	P3.5	T1	SCL0	CKO[2]	I/O	
	9	13	16	P3.6		CKO		I/O	
	NC	14	17	P3.7				I/O	
	NC	24	32	P4.0	PWM0[2]		T2EX	I/O	**PORT4:** General purpose I/O port, which can be configured by software in four modes. Its multifunction pins are for PWM0-3, SCL1, SDA1, ICE_CLK and ICE_DAT. The ICE_CLK/ICE_DAT pins are for JTAG-ICE function use. PWM0-3 can be used from P2.0-P2.3 or P4.0-P4.3. The T2EX/T3EX pins are for external capture/reset trigger input of Timer2/3.
	NC	36	48	P4.1	PWM1[2]		T3EX	I/O	
	NC	48	64	P4.2	PWM2[2]			I/O	
	NC	12	15	P4.3	PWM3[2]			I/O	
	NC	28	36	P4.4		SCL1		I/O	
	NC	29	37	P4.5		SDA1		I/O	
14	19	30	38	P4.6	ICE_CLK			I/O	
15	20	31	39	P4.7	ICE_DAT			I/O	
	NC	NC	7	P5.1	T1EX			I/O	**PORT5:** General purpose I/O port, which can be configured by software in four modes. Its multifunction pins are for T0EX, T1EX, SDA0 and SCL0. The T0EX/T1EX pins are for external capture/reset trigger input of Timer0/1. The SDA0/SCL0 pins are for I²C0 function use.
	NC	NC	8	P5.2	SDA0			I/O	
	NC	NC	9	P5.3	SCL0			I/O	
	NC	NC	23	P5.4				I/O	
	NC	NC	24	P5.5				I/O	
	NC	NC	25	P5.6				I/O	
	NC	NC	26	P5.7				I/O	
	NC	NC	40	P6.0				I/O	**PORT6:** General purpose I/O

Pin Number				Symbol	Alternate Function			Type[1]	Description
TSSOP 20	QFN 33	LQFP 48	LQFP 64		1	2	3		
	NC	NC	41	P6.1				I/O	port, which can be configured by software in four modes.
	NC	NC	42	P6.2				I/O	
	NC	NC	43	P6.3				I/O	
	NC	NC	57	P6.6				I/O	
	NC	NC	58	P6.7				I/O	
9	10	15	18	P7.0	XTAL2			I/O, O	PORT7: General purpose I/O port, which can be configured by software in four modes. Its multifunction pins are for XTAL
10	11	16	19	P7.1	XTAL1			I/O, I(ST)	XTAL: External 4~24 MHz (high speed) crystal pin.

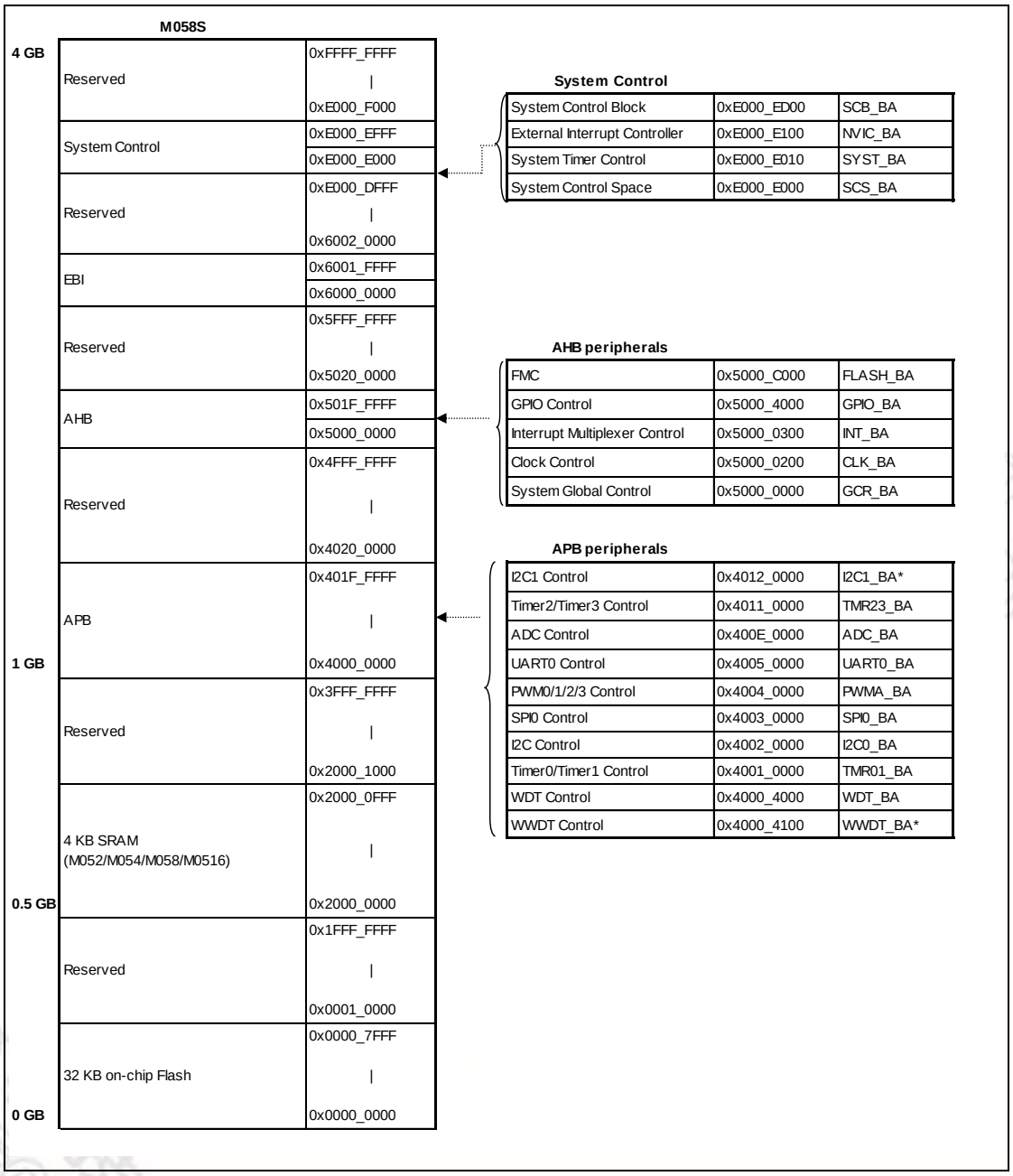
Note 1: I/O type description. I: Input, O: Output, I/O: Quasi-bidirectional, D: Open-drain, P: Power pins, ST: Schmitt trigger.

Note 2: The PWM0 ~ PWM3, RXD, TXD, RXD1, TXD1, SCL1, SDA1 and CKO can be assigned to different pins. However, a pin function can only be assigned to a pin at the same time, i.e. software cannot assign RXD to P0.3 and P3.0 at the same time.

0xE000_ED00 – 0xE000_ED8F	SCB_BA	System Control Block Registers

Table 6.2-1 Address Space Assignments for On-Chip Modules

6.2.5 Whole System Memory Mapping



6.2.6 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick. SysTick provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_CVR) to 0, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_RVR) on the next clock edge, then decrement on subsequent clocks. When the counter transitions to 0, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_CVR value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_RVR value rather than an arbitrary value when it is enabled.

If the SYST_RVR is 0, the timer will be maintained with a current value of 0 after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the documents “ARM® Cortex®-M0 Technical Reference Manual” and “ARM® v6-M Architecture Reference Manual”.

6.2.7.1 Exception Model and System Interrupt Map

The following table lists the exception model supported by NuMicro™ M058S series. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0” and the lowest priority is denoted as “3”. The default priority of all the user-configurable interrupts is “0”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable
SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 6.2-2 Exception Model

Exception Number	Vector Address	Interrupt Number (Bit in Interrupt Registers)	Interrupt Name	Source Module	Interrupt description	Power-down Wakeup
1-15					System exceptions	
16	0x40	0	BOD_INT	Brown-out	Brown-out low voltage detected interrupt	Yes
17	0x44	1	WDT_INT	WDT	Watchdog Timer interrupt	Yes
18	0x48	2	EINT0	GPIO	External signal interrupt from P3.2 pin	Yes
19	0x4C	3	EINT1	GPIO	External signal interrupt from P3.3 pin	Yes
20	0x50	4	GP01_INT	GPIO	External signal interrupt from P0[7:0] / P1[7:0]	Yes
21	0x54	5	GP234_INT	GPIO	External interrupt from P2[7:0]/P3[7:0]/P4[7:0], except P32 and P33	Yes

entry as illustrated in previous section.

Vector Table Word Offset	Description
0	SP_main – The Main stack pointer
Vector Number	Exception Entry Pointer using that Vector Number

Table 6.2-4 Vector Figure Format

6.2.7.3 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip enters Power-down mode when Cortex®-M0 core executes the WFI instruction only if the PWR_DOWN_EN (PWRCON[7]) bit and PD_WAIT_CPU (PWRCON[8]) bit are both set to 1. After that, chip enters Power-down mode and waits for wake-up interrupt source triggered to exit Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT) and 22.1184 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. The following figures show the clock generator and the overview of the clock source control.

6.3.2 Clock Generator Block Diagram

The clock generator consists of 4 clock sources as listed below:

- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLL source can be selected from external 4~24 MHz external high speed crystal (HXT) or 22.1184 MHz internal high speed oscillator (HIRC)) (PLL FOUT)
- 22.1184 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

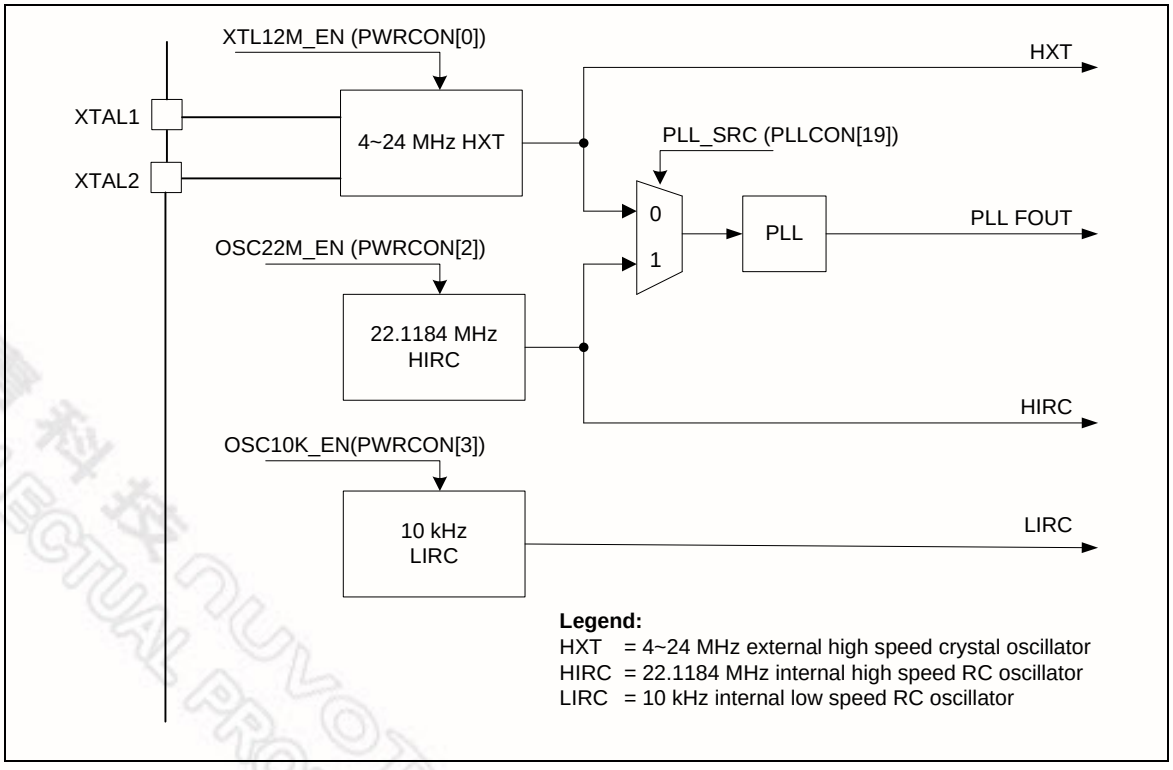


Figure 6.3-1 Clock Generator Block Diagram

6.3.4 Power-down Mode Clock

When chip enters Power-down mode, system clocks, some clock sources, and some peripheral clocks will be disabled. Some clock sources and peripherals clocks are still active in Power-down mode.

The clocks still kept active are listed below:

- Clock Generator
- 10 kHz internal low speed oscillator clock
- Peripherals Clock (when 10 kHz low speed oscillator is adopted as clock source)

6.3.5 Frequency Divider Output

This device is equipped with a power-of-2 frequency divider which is composed by 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to the CKO pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where Fin is input clock frequency to the clock divider.

The output formula is $\boldsymbol{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQDIV.FSEL[3:0].

When write 1 to DIVIDER_EN (FRQDIV[4]), the chained counter starts to count. When write 0 to DIVIDER_EN (FRQDIV[4]), the chained counter continuously runs till divided clock reaches low state and stay in low state.

If DIVIDER1(FRQDIV[5]) set to 1, the frequency divider clock (FRQDIV_CLK) will bypass power-of-2 frequency divider. The frequency divider clock will be output to CKO pin directly.

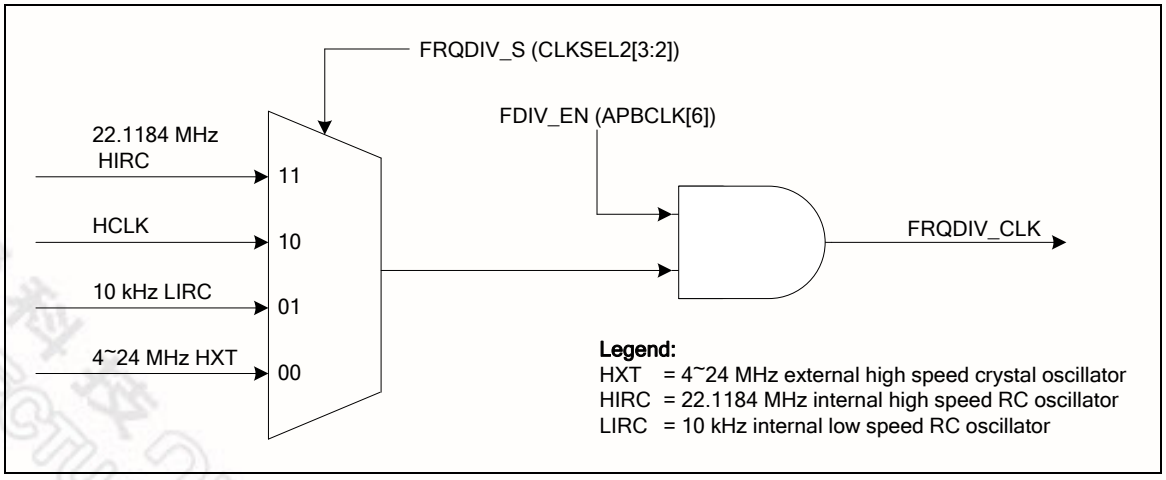


Figure 6.3-6 Clock Source of Frequency Divider

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

There are 58 General Purpose I/O pins shared with special feature functions in this MCU. The 58 pins are arranged in 9 ports named with P0, P1… to P7. Each port equips maximum 8 pins except P7[1:0]. Each one of the 58 pins is independent and has the corresponding register bits to control the pin mode function and data

The I/O type of each of I/O pins can be software configured individually as input, output, open-drain or quasi-bidirectional mode. The all pins of I/O type stay in quasi-bidirectional mode and port data register Px_DOUT[7:0] resets to 0x000_00FF. Each I/O pin equips a very weakly individual pull-up resistor which is about 110KΩ~300KΩ for V_{DD} which is from 5.0V to 2.5V.

6.5.2 Features

- Four I/O modes:
  - Input only with high impedance
  - Push-pull output
  - Open-drain output
- Quasi-bidirectional TTL/Schmitt trigger input mode selected by Px_MFP[23:16]
- I/O pin configured as interrupt source with edge/level setting
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the pin wake-up function
- Configurable default I/O mode of all pins after reset by CIOINI(CONFIG[10]) setting
  - CIOINI = 0, all GPIO pins in Input tri-state mode after chip reset
  - CIOINI = 1, all GPIO pins in Quasi-bidirectional mode after chip reset

6.12 Serial Peripheral Interface (SPI)

6.12.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full-duplex transfer. Devices communicate in Master/Slave mode with 4-wire bi-direction interface. The NuMicro™ M058S contains one set of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. SPI controller can be configured as a master or a slave device.

6.12.2 Features

- One set of SPI controllers
- Supports Master or Slave mode operation
- Configurable transfer bit length
- Provides transmit/receive can be transferred up to two times word transaction in one transfer
  - Provides FIFO buffers
- Supports MSB or LSB first transfer
- Supports byte reorder function
- Supports byte or word suspend mode
- Supports Slave 3-wire mode
- SPI bus clock rate can be configured to equal the system clock rate

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	V_{DD} –V_{SS}	-0.3	+7.0	V
Input Voltage	VIN	V_{SS}-0.3	V_{DD} +0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}			120	mA
Maximum Current sunk by a I/O pin			35	mA
Maximum Current sourced by a I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

7.2 DC Electrical Characteristics

(V_{DD} -V_{SS}=2.5~5.5V, TA = 25°C, F_{OSC} = 50 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operation voltage	V_{DD}	2.5		5.5	V	V_{DD} =2.5V ~ 5.5V up to 50 MHz
LDO Output Voltage	V_{LDO}	1.7	1.8	1.9	V	V_{DD} ≥ 2.5V
Band Gap Analog Input	V_{BG}	-5%	1.20	+5%	V	V_{DD} =2.5V ~ 5.5V
Analog Operating Voltage	AV_{DD}	V_{DD}		V_{DD}	V	
Operating Current Normal Run Mode @ 50 MHz	IDD1		20.6		mA	V_{DD} = 5.5V@ 50 MHz, enable all peripherals and PLL, XTAL=12 MHz
	IDD2		14.4		mA	V_{DD} =5.5V@ 50 MHz, disable all peripherals and enable PLL, XTAL=12 MHz
	IDD3		18.9		mA	V_{DD} = 3.3V@ 50 MHz, enable all peripherals and PLL, XTAL=12 MHz
	IDD4		12.8		mA	V_{DD} = 3.3V@ 50 MHz, disable all peripherals and enable PLL, XTAL=12 MHz
Operating Current Normal Run Mode @ 22 MHz	IDD5		6.2		mA	V_{DD} = 5.5V@ 22 MHz, enable all peripherals and IRC 22 MHz, disable PLL
	IDD6		3.4		mA	V_{DD} =5.5V@ 22 MHz, disable all peripherals and enable IRC 22 MHz, disable PLL
	IDD7		6.1		mA	V_{DD} = 3.3V@ 22 MHz, enable all peripherals and IRC 22 MHz, disable PLL
	IDD8		3.4		mA	V_{DD} = 3.3V@ 22 MHz, disable all peripherals and enable IRC 22 MHz, disable PLL
Operating Current Normal Run Mode @ 12 MHz	IDD9		5.3		mA	V_{DD} = 5.5V@ 12 MHz, enable all peripherals and disable PLL, XTAL=12 MHz
	IDD10		3.7		mA	V_{DD} = 5.5V@ 12 MHz, disable all peripherals and disable PLL, XTAL=12 MHz
	IDD11		4.0		mA	V_{DD} = 3.3V@ 12 MHz, enable all peripherals and disable PLL, XTAL=12 MHz
	IDD12		2.3		mA	V_{DD} = 3.3V@ 12 MHz, disable all peripherals and disable PLL, XTAL=12 MHz

7.3.3 Typical Crystal Application Circuits

CRYSTAL	C1	C2
4 MHz ~ 24 MHz	Optional (Depend on crystal specification)	

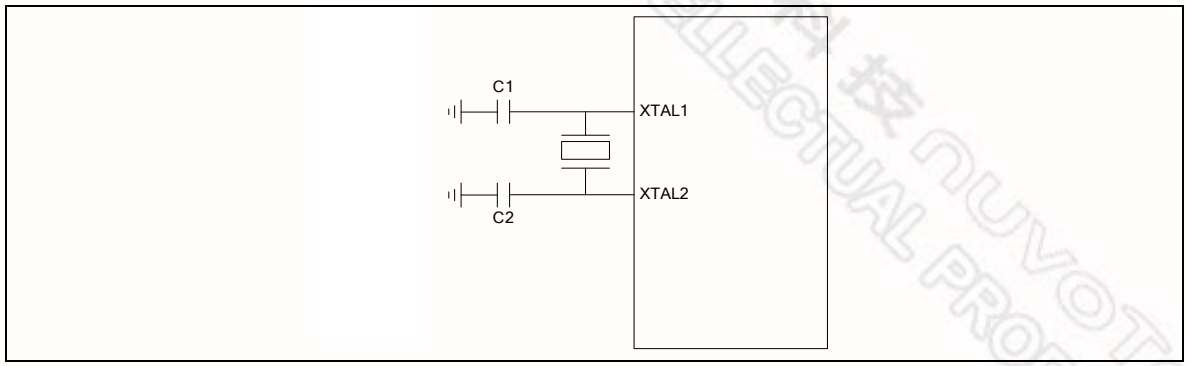


Figure 7.3-1 Typical Crystal Application Circuit

7.3.4 Internal 22.1184 MHz RC Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Center Frequency	-	-	22.1184		MHz
Calibrated Internal Oscillator Frequency	+25°C; V_{DD} =5V	-3	-	+3	%
	-40°C~+85°C; V_{DD}=2.5V~5.5V	-5	-	+5	%
Operating current	V_{DD} =5V	-	500	-	uA

7.3.5 Internal 10 kHz RC Oscillator

PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25°C; V_{DD} =5V	-30	-	+30	%
	-40°C~+85°C; V_{DD}=2.5V~5.5V	-50	-	+50	%
Operating current	V_{DD} =5V	-	5	-	uA

Notes:

1. Internal operation voltage comes from LDO.

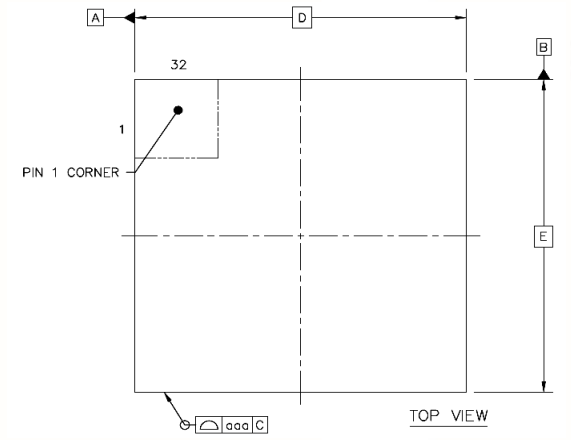
7.4.2 LDO Specification

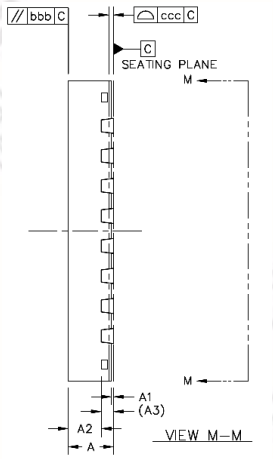
RAMETER	MIN	TYP	MAX	UNIT	NOTE
Input Voltage	2.5		5.5	V	V_{DD} input voltage
Output Voltage	-10%	1.8	+10%	V	LDO output voltage
Temperature	-40	25	85	℃	
C	-	1	-	uF	Resr=1ohm

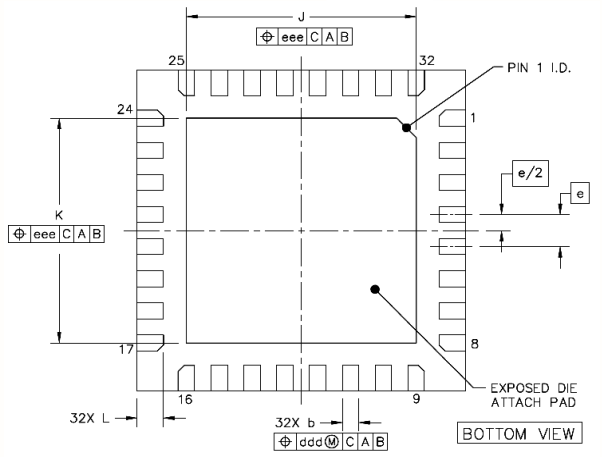
Note:

1. It is recommended a 100nF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. For ensuring power stability, a 1uF or higher capacitor must be connected between LDO pin and the closest V_{SS} pin of the device.

8.2 QFN-33 (5X5 mm^2, Thickness 0.8mm, Pitch 0.5 mm)







		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

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