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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	168MHz
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 29x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkv44f128vlh16

Kinetis Motor Suite

- Supports velocity and position control of BLDC and PMSM motors
- Implements Field Orient Control (FOC) using Back EMF to improve motor efficiency
- Utilizes SpinTAC control theory that improves overall system performance and reliability

Security and integrity modules

- Hardware CRC module to support fast cyclic redundancy checks
- External Watchdog Monitor (EWM)

NOTE

The 48-pin LQFP package for this product is not yet available. However, it is included in a Package Your Way program for Kinetis MCUs. Visit nxp.com/KPYW for more details.

Orderable part numbers summary[1]

NXP part number	CPU frequency (MHz)	Pin count	Total flash memory (KB)	SRAM (KB)	ADC		eFlexPWM		PWM Nano-Edge	Flex Timers			DAC	FlexCAN	
					ADCA	ADCB	PWMA PWMB	PWMX		FTM0	FTM3	FTM1		CAN0	CAN1
MKV46F256VLL16	168	100	256	32	18ch	20ch	1x8ch	1x4ch	Yes	1x8ch	1x8ch	1x2ch	1	1	1
MKV46F256VLH16	168	64	256	32	13ch	16ch	1x8ch	—	Yes	1x8ch	1x8ch	1x2ch	1	1	1
MKV46F128VLL16	168	100	128	24	18ch	20ch	1x8ch	1x4ch	Yes	1x8ch	1x8ch	1x2ch	1	1	1
MKV46F128VLH16	168	64	128	24	13ch	16ch	1x8ch	—	Yes	1x8ch	1x8ch	1x2ch	1	1	1
MKV44F256VLL16	168	100	256	32	18ch	20ch	1x8ch	1x4ch	Yes	—	—	—	1	1	1
MKV44F256VLH16	168	64	256	32	13ch	16ch	1x8ch	—	Yes	—	—	—	1	1	1
MKV44F128VLL16	168	100	128	24	18ch	20ch	1x8ch	1x4ch	Yes	—	—	—	1	1	1
MKV44F128VLH16	168	64	128	24	13ch	16ch	1x8ch	—	Yes	—	—	—	1	1	1
MKV44F128VLF16[2]	168	48	128	24	11ch	10ch	1x8ch	—	Yes	—	—	—	1	1	—
MKV44F64VLH16	168	64	64	16	13ch	16ch	1x8ch	—	Yes	—	—	—	1	1	1
MKV44F64VLF16[2]	168	48	64	16	11ch	10ch	1x8ch	—	Yes	—	—	—	1	1	—
MKV42F256VLL16	168	100	256	32	18ch	20ch	—	—	—	1x8ch	1x8ch	1x2ch	—	1	1
MKV42F256VLH16	168	64	256	32	13ch	16ch	—	—	—	1x8ch	1x8ch	1x2ch	—	1	1
MKV42F128VLL16	168	100	128	24	18ch	20ch	—	—	—	1x8ch	1x8ch	1x2ch	—	1	1

Table continues on the next page...

Orderable part numbers summary[1] (continued)

NXP part number	CPU frequency (MHz)	Pin count	Total flash memory (KB)	SRAM (KB)	ADC		eFlexPWM		PWM Nano-Edge	Flex Timers			DAC	FlexCAN	
					ADCA	ADCB	PWMA PWMB	PWMX		FTM0	FTM3	FTM1		CAN0	CAN1
MKV42F128VLH16	168	64	128	24	13ch	16ch	—	—	—	1x8ch	1x8ch	1x2ch	—	1	1
MKV42F128VLF16[2]	168	48	128	24	11ch	10ch	—	—	—	1x8ch	1x8ch	1x2ch	—	1	—
MKV42F64VLH16	168	64	64	16	13ch	16ch	—	—	—	1x8ch	1x8ch	1x2ch	—	1	1
MKV42F64VLF16[2]	168	48	64	16	11ch	10ch	—	—	—	1x8ch	1x8ch	1x2ch	—	1	—

1. To confirm current availability of ordererable part numbers, go to http://www.nxp.com and perform a part number search.
2. Package Your Way.

Related Resources

Type	Description	Resource
Selector Guide	The Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KV4XP100M168RM[1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	KV4XP100M168[1]
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	Kinetis_V_1N72K[1]
KMS User Guide	The KMS User Guide provides a comprehensive description of the features and functions of the Kinetis Motor Suite solution.	Kinetis Motor Suite User's Guide (KMS100UG)[1]
KMS API Reference Manual	The KMS API reference manual provides a comprehensive description of the API of the Kinetis Motor Suite function blocks.	Kinetis Motor Suite API Reference Manual (KMS100RM)[1]
Package drawing	Package dimensions are provided in package drawings.	• LQFP 100-pin: 98ASS23308W[1] • LQFP 64-pin: 98ASS23234W[1] • LQFP 48-pin: 98ASH00962A[1]

1. To find the associated resource, go to http://www.nxp.com and perform a search using this term.

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.8	V
I_{DD}	Digital supply current	—	120	mA
V_{IO}	Digital pin input voltage (except open drain pins)	–0.3	VDD + 0.3[1]	V
	Open drain pins (PTC6 and PTC7)	–0.3	5.5	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V

1. Maximum value of V_{IO} (except open drain pins) must be 3.8 V.

1.5 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 1 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

Table 1. Absolute Maximum Ratings (V_{SS} = 0 V, V_{SSA} = 0 V)

Symbol	Description	Notes[1]	Min	Max	Unit
V_{DD}	Supply Voltage Range		-0.3	4.0	V
V_{DDA}	Analog Supply Voltage Range		-0.3	4.0	V
V_{REFHx}	ADC High Voltage Reference		-0.3	4.0	V
V_{REFLx}	ADC Low Voltage Reference		-0.3	0.3	V
ΔV_{DD}	Voltage difference V_{DD} to V_{DDA}		-0.3	0.3	V
ΔV_{SS}	Voltage difference V_{SS} to V_{SSA}		-0.3	0.3	V
V_{IN}	Digital Input Voltage Range	Pin Groups 1, 2	-0.3	4.0	V
V_{OSC}	Oscillator Input Voltage Range	Pin Group 4	-0.4	4.0	V
V_{INA}	Analog Input Voltage Range	Pin Group 3	-0.3	4.0	V
I_{IC}	Input clamp current, per pin (V_{IN} < 0)		—	-20.0	mA
I_{OC}	Output clamp current, per pin (V_O < 0)[2]		—	-20.0	mA
V_{OUT}	Output Voltage Range (Normal Push-Pull mode)	Pin Group 1	-0.3	4.0	V
V_{OUTOD}	Output Voltage Range (Open Drain mode)	Pin Group 2	-0.3	5.5	V
V_{OUT_DAC}	DAC Output Voltage Range	Pin Group 5	-0.3	4.0	V
T_A	Ambient Temperature Industrial		-40	105	°C
T_{STG}	Storage Temperature Range (Extended Industrial)		-55	150	°C

1. Default Mode
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$, PORTC6, and PORTC7
   - Pin Group 3: ADC and Comparator Analog Inputs

- Pin Group 4: XTAL, EXTAL
- Pin Group 5: DAC analog output

2. Continuous clamp current per pin is -2.0 mA

2 General

Electromagnetic compatibility (EMC) performance depends on the environment in which the MCU resides. Board design and layout, circuit topology choices, location, characteristics of external components, and MCU software operation play a significant role in EMC performance.

See the following applications notes available on nxp.com for guidelines on optimizing EMC performance.

- *AN2321: Designing for Board Level Electromagnetic Compatibility*
- *AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers*
- *AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers*
- *AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications*
- *AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems*

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

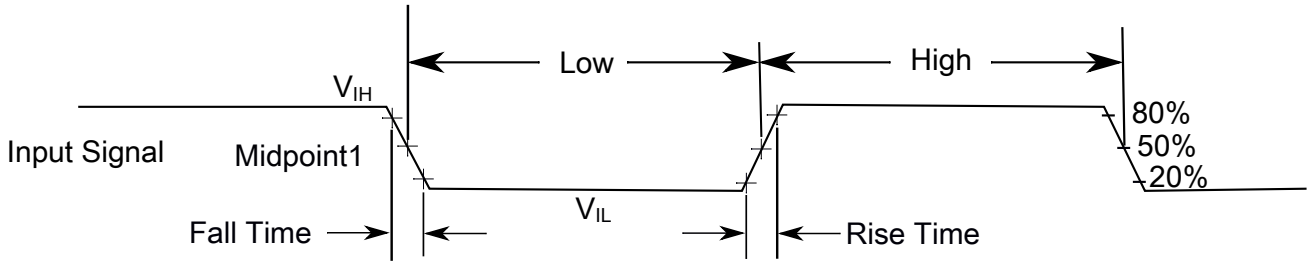


Figure 2. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume:

1. output pins
   - have C_L=30pF loads,
   - are slew rate disabled, and
   - are normal drive strength

2.2 Nonswitching electrical specifications

2.2.1 Recommended Operating Conditions

This section includes information about recommended operating conditions.

NOTE

Recommended V_{DD} ramp rate is between 1 ms and 200 ms.

Table 2. Recommended Operating Conditions (V_{REFLx}=0V, V_{SSA}=0V, V_{SS}=0V)

Symbol	Description	Notes[1]	Min	Typ	Max	Unit
V_{DD}	Supply Voltage Digital	2, 3	1.71		3.6	V
V_{DDA}	Supply voltage (analog)	2, 3	2.7	3.0	3.6	V
V_{REFHx}	ADC (Cyclic) Reference Voltage High		2.7		V_{DDA}	V
ΔVDD	Voltage difference V_{DD} to V_{DDA}		-0.1	0	0.1	V
ΔVSS	Voltage difference V_{SS} to V_{SSA}		-0.1	0	0.1	V
F_MCGOUT	Device Clock Frequency • using internal RC oscillator • using external clock source		0.04 0		168 168	MHz
V_{IH}	Input Voltage High (digital inputs)	Pin Groups 1, 2	0.7 x V_{DD}		3.6	V
V_{IL}	Input Voltage Low (digital inputs)	Pin Groups 1, 2			0.35 x V_{DD}	V
V_{IHOSC}	Oscillator Input Voltage High XTAL driven by an external clock source	Pin Group 4	2.0		V_{DD} + 0.3	V
V_{ILOSC}	Oscillator Input Voltage Low	Pin Group 4	-0.3		0.8	V
C_{out}	DAC Output Current Drive Strength	Pin Group 5			1	mA
T_A	Ambient Operating Temperature		-40		105	°C

1. Default Mode
   - Pin Group 1: GPIO, TDI, TDO, TMS, TCK
   - Pin Group 2: $\overline{\text{RESET}}$
   - Pin Group 3: ADC and Comparator Analog Inputs
   - Pin Group 4: XTAL, EXTAL
   - Pin Group 5: DAC analog output
   - Pin Group 6: PTB0, PTB1, PTD4, PTD5, PTD6, PTD7, PTC3, and PTC4. have high output current capability
   - Pin Group 7: PTC6 and PTC7 are true open drain pins and have no P-chanl transistor. A external pull-up resistor is required when these pins are outputs.

Table 6. Power consumption operating behaviors (All IDDs are Target values) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• @ –40 to 25°C	—	2.7	3.3	µA	
	• @ 70°C	—	6.6	12.2	µA	
	• @ 105°C	—	25.9	50.5	µA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	• @ –40 to 25°C	—	740	1200	nA	
	• @ 70°C	—	2.5	10.6	µA	
	• @ 105°C	—	11.1	26.5	µA	
I_{DD_VLLS0B}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled					
	• @ –40 to 25°C	—	420	832	nA	
	• @ 70°C	—	1.9	9.4	µA	
	• @ 105°C	—	10.8	26.3	µA	
I_{DD_VLLS0A}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled					
	• @ –40 to 25°C	—	200	599	nA	
	• @ 70°C	—	1.8	10.5	µA	
	• @ 105°C	—	10.8	26.3	µA	

Table 7. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{IREFSTEN4MHz}$	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	µA
$I_{IREFSTEN32KHz}$	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	µA
$I_{EREFSTEN4MHz}$	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	uA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.							nA
	VLLS1							
	VLLS3	440	490	540	560	570	580	
	VLPS	440	490	540	560	570	580	
	STOP	510	560	560	560	610	680	

Table continues on the next page...

Table 7. Low power mode peripheral adders — typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
		510	560	560	560	610	680	
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	µA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							µA
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	
	OSCERCLK (4 MHz external crystal)	214	234	246	254	260	268	
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx or VLLSx mode.	45	45	45	45	45	45	µA

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode, and BLPE for VLPR mode
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

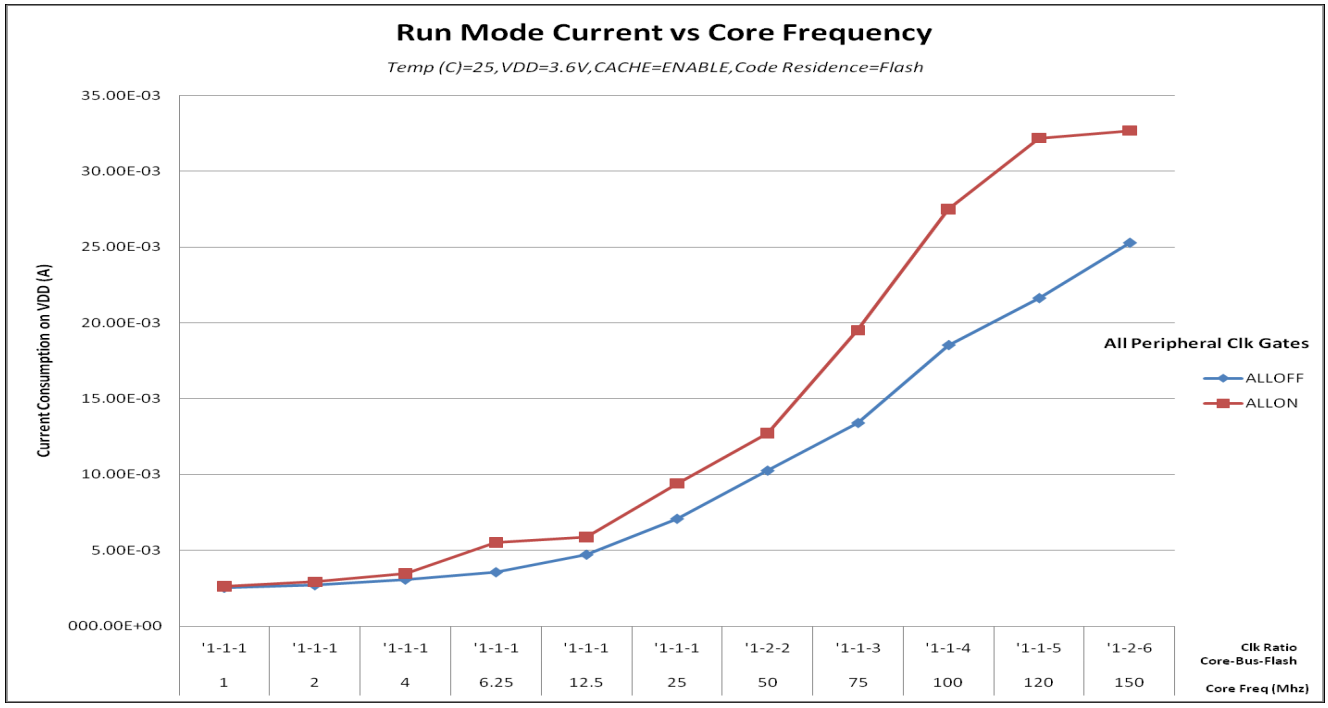


Figure 3. Run mode supply current vs. core frequency

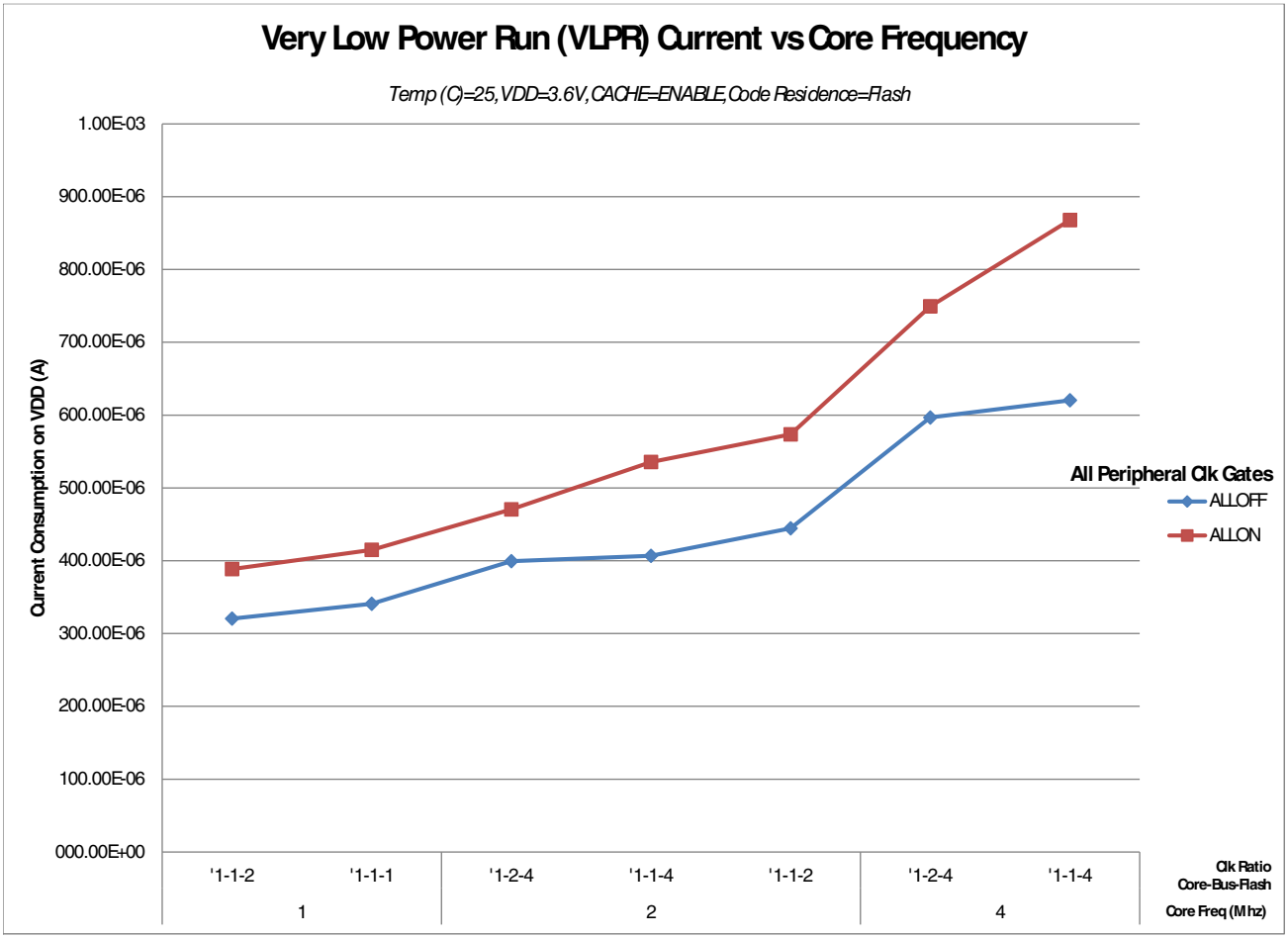


Figure 4. VLPR mode current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

NOTE

EMC measurements to IC-level IEC standards are available from NXP on request.

Table 8. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	20	dBµV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	18	dBµV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	14	dBµV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	8	dBµV	
V_{RE_IEC}	IEC level	0.15–1000	L	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = 10 MHz (crystal), f_{SYS} = 75 MHz, f_{BUS} = 25 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.nxp.com.
2. Perform a keyword search for “EMC design.”

2.2.8 Capacitance attributes

Table 9. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

2.3 Switching specifications

2.3.1 Typical device clock specifications

Table 10. Typical device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
High Speed RUN mode					
f_{SYS}	System and core clock	—	168	MHz	
f_{BUS}	Bus and Flash clock	—	24	MHz	
f_{FPCK}	Fast peripheral clock	—	84	MHz	
f_{NANO}	Nano-edge clock	—	168	MHz	
Normal run mode					
f_{SYS}	System and core clock	—	100	MHz	
f_{BUS}	Bus and Flash clock	—	25	MHz	

Table continues on the next page...

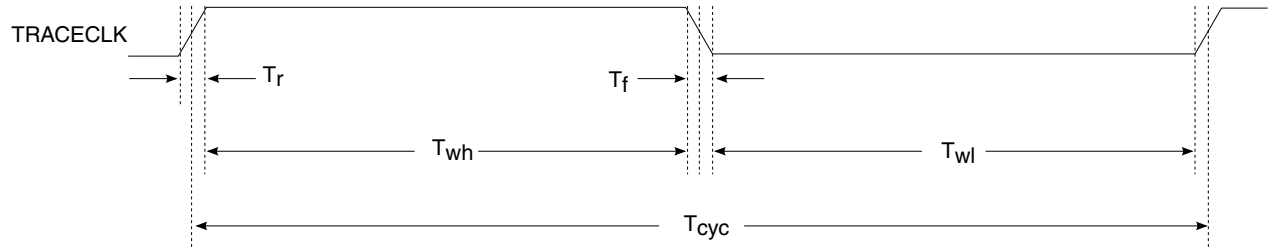


Figure 7. TRACE_CLKOUT specifications

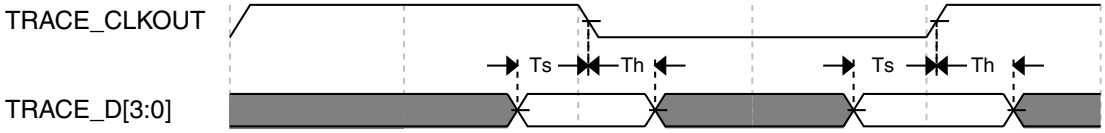


Figure 8. Trace data specifications

3.1.3 JTAG electricals

Table 16. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	25	
	• Serial Wire Debug	0	50	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	20	—	ns
	• Serial Wire Debug	10	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2.0	—	ns
J7	TCLK low to boundary scan output data valid	—	28	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns

Table continues on the next page...

Table 18. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• f_{vco} = 48 MHz	—	1350	—	ps	
	• f_{vco} = 120 MHz	—	600	—	ps	
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll\_ref})$	s	9

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a NXP developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.3.2 Oscillator electrical specifications

3.3.2.1 Oscillator DC electrical specifications

Table 19. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	µA	
	• 8 MHz	—	300	—	µA	
	• 16 MHz	—	950	—	µA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 4 MHz	—	400	—	µA	

Table continues on the next page...

Table 19. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• 8 MHz	—	500	—	µA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x,C_y can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

Table 25. 12-bit ADC electrical specifications (continued)

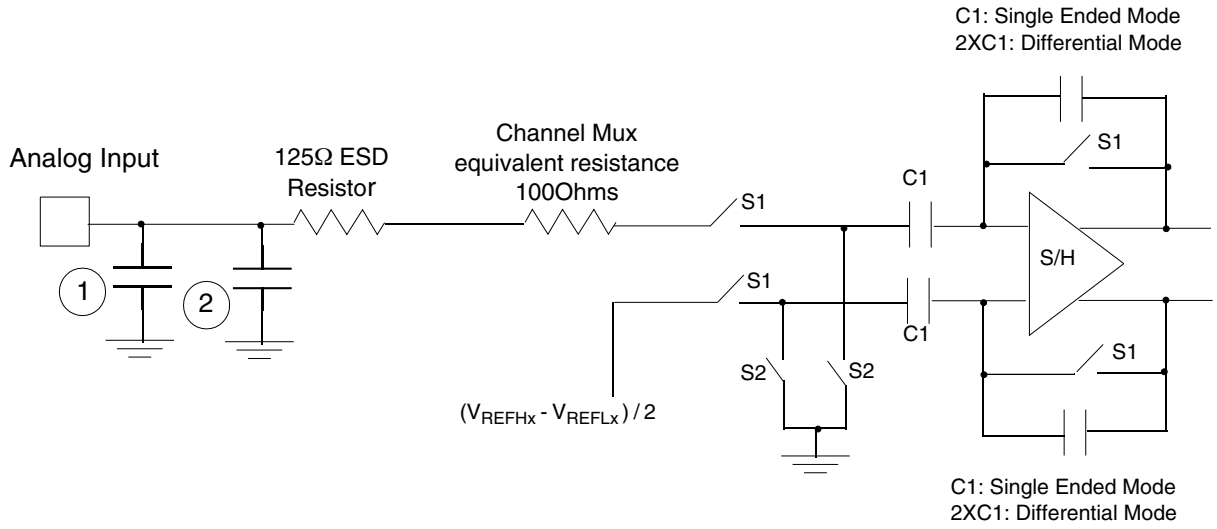
Characteristic	Symbol	Min	Typ	Max	Unit
Monotonicity					
Offset[6] • 1x gain mode • 2x gain mode • 4x gain mode	V_{OFFSET}			 +/- 25 +/- 20 +50, -10	LSB[4]
Gain Error	E_{GAIN}		0.0002	—	%
AC Specifications[7]					
Signal to Noise Ratio	SNR		59		dB
Total Harmonic Distortion	THD		64		dB
Spurious Free Dynamic Range	SFDR		65		dB
Signal to Noise plus Distortion	SINAD		59		dB
Effective Number of Bits	ENOB		9.1		bits
ADC Inputs					
Input Leakage Current	I_{IN}		0	+/-2	µA
Input Injection Current [8]	I_{INJ}			+/-3	mA
Input Capacitance Sampling Capacitor	C_{ADI}		4.8		pF

1. If the ADC's reference is from V_{DDA}: When V_{DDA} is below 2.7 V, then the ADC functions, but the ADC specifications are not guaranteed.
2. When the input is at the V_{refl} level, then the resulting output will be all zeros (hex 000), plus any error contribution due to offset and gain error. When the input is at the V_{refh} level, then the output will be all ones (hex FFF), minus any error contribution due to offset and gain error.
3. ADC clock duty cycle min/max is 45/55% .
4. D_{NL} and I_{NL} conversion accuracy is not guaranteed from V_{REFL} to V_{REFL} + 0025 and V_{REFH} to V_{REFH}-0025.
5. LSB = Least Significant Bit = 0.806 mV at 3.3 V VDDA, x1 Gain Setting
6. Offset over the conversion range of 0025 to 4070, with internal/external reference.
7. Measured when converting a 1 kHz input Full Scale sine wave.
8. The current that can be *injected into* or *sourced from* an unselected ADC input, without affecting the performance of the ADC.

3.6.1.1 Equivalent circuit for ADC inputs

The following figure shows the ADC input circuit during sample and hold. S1 and S2 are always opened/closed at non-overlapping phases, and both S1 and S2 operate at the ADC clock frequency. The following equation gives equivalent input impedance when the input is selected.

$$\frac{1}{(\text{ADC ClockRate}) \times 1.4 \times 10^{-12}} + 100\,ohm + 125\,ohm$$



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling = 1.8pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing = 2.04pF
3. Sampling capacitor at the sample and hold circuit. Capacitor C1 (4.8pF) is normally disconnected from the input, and is only connected to the input at sampling time.
4. S1 and S2 switch phases are non-overlapping and operate at the ADC clock frequency

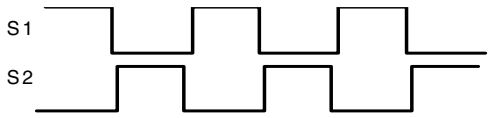


Figure 13. Equivalent circuit for A/D loading

3.6.2 CMP and 6-bit DAC electrical specifications

Table 26. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, high-speed mode (EN = 1, PMODE = 1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN = 1, PMODE = 0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS}	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				

Table continues on the next page...

Table 28. 12-bit DAC operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	µs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) • High-speed mode • Low speed mode	—	1	5	µs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} −100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	4
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	5
E_G	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, V_{DDA} ≥ 2.4 V	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	µV/C	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance (load = 3 kΩ)	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h • High power (SP_{HP}) • Low power (SP_{LP})	 1.2 0.05	 1.7 0.12	 — —	V/µs	
BW	3dB bandwidth • High power (SP_{HP}) • Low power (SP_{LP})	 550 40	 — —	 — —	kHz	

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to V_{DACR} −100 mV
3. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV
4. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV with V_{DDA} > 2.4 V
5. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} − 100 mV
6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

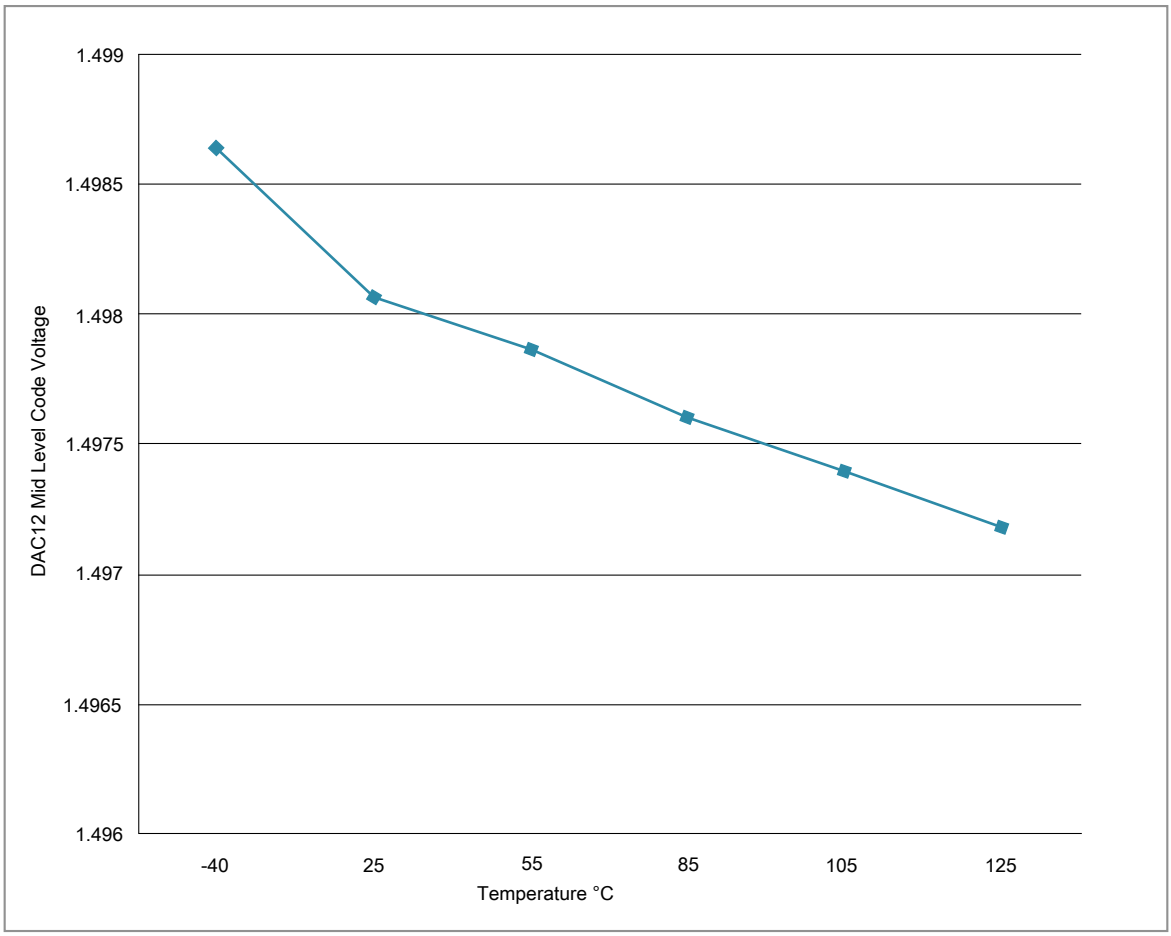


Figure 17. Offset at half scale vs. temperature

3.7 Timers

See General switching specifications.

3.8 Enhanced NanoEdge PWM characteristics

Table 29. NanoEdge PWM timing parameters - 100 Mhz operating frequency

Characteristic	Symbol	Min.	Typ.	Max.	Unit
PWM clock frequency			100		MHz
NanoEdge Placement (NEP) Step Size[1, 2]	pwmp		312		ps

Table continues on the next page...

Table 29. NanoEdge PWM timing parameters - 100 Mhz operating frequency (continued)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Delay for fault input activating to PWM output deactivated		1			ns
Power-up Time[3]	t_{pu}		25		µs

1. Reference 100 MHz in NanoEdge Placement mode.
2. Temperature and voltage variations do not affect NanoEdge Placement step size.
3. Powerdown to NanoEdge mode transition.

Table 30. NanoEdge PWM timing parameters - 84 Mhz operating frequency

Characteristic	Symbol	Min.	Typ.	Max.	Unit
PWM clock frequency			84		MHz
NanoEdge Placement (NEP) Step Size[1], [2]	pwmp		372		ps
Delay for fault input activating to PWM output deactivated		1			ns
Power-up Time[3]	t_{pu}		30		µs

1. Reference 84 MHz in NanoEdge Placement mode.
2. Temperature and voltage variations do not affect NanoEdge Placement step size.
3. Powerdown to NanoEdge mode transition.

3.9 Communication interfaces

3.9.1 SPI (DSPI) switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

NOTE

Fast pads:

- SIN: PTE19
- SOUT: PTE18
- SCK: PTE17
- PCS: PTE16

Open drain pads:

Table 38. Master mode DSPI timing fast pads (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	4 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) - 4	($t_{SCK/2)}$ + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 4	—	ns	2
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 4	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-7.8	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	17	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

Table 39. Master mode DSPI timing open drain pads (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	18.75	MHz	
DS1	DSPI_SCK output cycle time	4 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) - 4	($t_{SCK/2)}$ + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 4	—	ns	2
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 4	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	26	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-7.8	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	24	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

Table 42. Slave mode DSPI timing for open drain pads (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	9.375	MHz
DS9	DSPI_SCK input cycle time	8 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) - 4	($t_{SCK/2}$) + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	43.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.5	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	38	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	38	ns

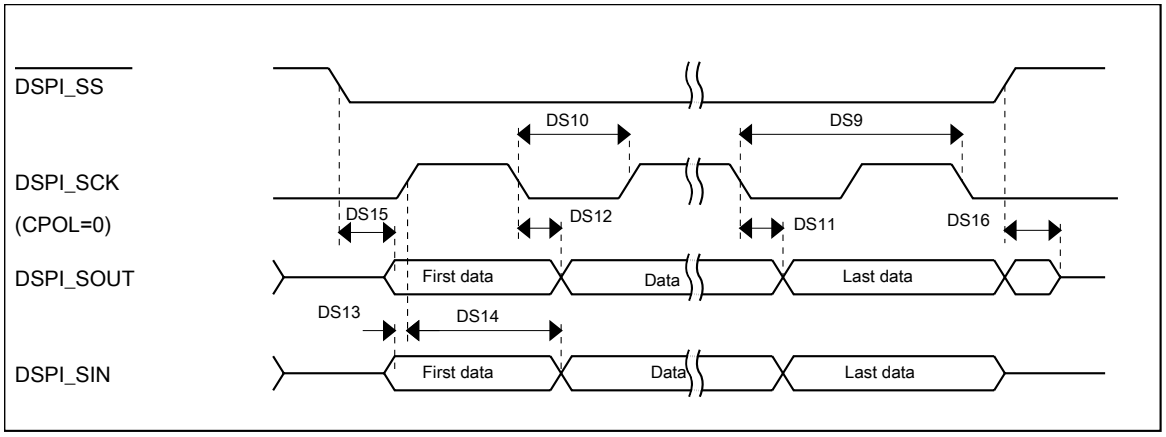


Figure 21. DSPI classic SPI timing — slave mode

3.9.3 I²C

See General switching specifications.

3.9.4 UART

See General switching specifications.

3.10 Kinetis Motor Suite (KMS)