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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	-
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Speed	-
Connectivity	-
Peripherals	-
Number of I/O	-
Program Memory Size	-
Program Memory Type	-
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkv44f128vll16

Kinetis Motor Suite

- Supports velocity and position control of BLDC and PMSM motors
- Implements Field Orient Control (FOC) using Back EMF to improve motor efficiency
- Utilizes SpinTAC control theory that improves overall system performance and reliability

Security and integrity modules

- Hardware CRC module to support fast cyclic redundancy checks
- External Watchdog Monitor (EWM)

NOTE

The 48-pin LQFP package for this product is not yet available. However, it is included in a Package Your Way program for Kinetis MCUs. Visit nxp.com/KPYW for more details.

Orderable part numbers summary[1]

NXP part number	CPU frequency (MHz)	Pin count	Total flash memory (KB)	SRAM (KB)	ADC		eFlexPWM		PWM Nano-Edge	Flex Timers			DAC	FlexCAN	
					ADCA	ADCB	PWMA PWMB	PWMX		FTM0	FTM3	FTM1		CAN0	CAN1
MKV46F256VLL16	168	100	256	32	18ch	20ch	1x8ch	1x4ch	Yes	1x8ch	1x8ch	1x2ch	1	1	1
MKV46F256VLH16	168	64	256	32	13ch	16ch	1x8ch	—	Yes	1x8ch	1x8ch	1x2ch	1	1	1
MKV46F128VLL16	168	100	128	24	18ch	20ch	1x8ch	1x4ch	Yes	1x8ch	1x8ch	1x2ch	1	1	1
MKV46F128VLH16	168	64	128	24	13ch	16ch	1x8ch	—	Yes	1x8ch	1x8ch	1x2ch	1	1	1
MKV44F256VLL16	168	100	256	32	18ch	20ch	1x8ch	1x4ch	Yes	—	—	—	1	1	1
MKV44F256VLH16	168	64	256	32	13ch	16ch	1x8ch	—	Yes	—	—	—	1	1	1
MKV44F128VLL16	168	100	128	24	18ch	20ch	1x8ch	1x4ch	Yes	—	—	—	1	1	1
MKV44F128VLH16	168	64	128	24	13ch	16ch	1x8ch	—	Yes	—	—	—	1	1	1
MKV44F128VLF16[2]	168	48	128	24	11ch	10ch	1x8ch	—	Yes	—	—	—	1	1	—
MKV44F64VLH16	168	64	64	16	13ch	16ch	1x8ch	—	Yes	—	—	—	1	1	1
MKV44F64VLF16[2]	168	48	64	16	11ch	10ch	1x8ch	—	Yes	—	—	—	1	1	—
MKV42F256VLL16	168	100	256	32	18ch	20ch	—	—	—	1x8ch	1x8ch	1x2ch	—	1	1
MKV42F256VLH16	168	64	256	32	13ch	16ch	—	—	—	1x8ch	1x8ch	1x2ch	—	1	1
MKV42F128VLL16	168	100	128	24	18ch	20ch	—	—	—	1x8ch	1x8ch	1x2ch	—	1	1

Table continues on the next page...

- Pin Group 4: XTAL, EXTAL
- Pin Group 5: DAC analog output

2. Continuous clamp current per pin is -2.0 mA

2 General

Electromagnetic compatibility (EMC) performance depends on the environment in which the MCU resides. Board design and layout, circuit topology choices, location, characteristics of external components, and MCU software operation play a significant role in EMC performance.

See the following applications notes available on nxp.com for guidelines on optimizing EMC performance.

- *AN2321: Designing for Board Level Electromagnetic Compatibility*
- *AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers*
- *AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers*
- *AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications*
- *AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems*

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

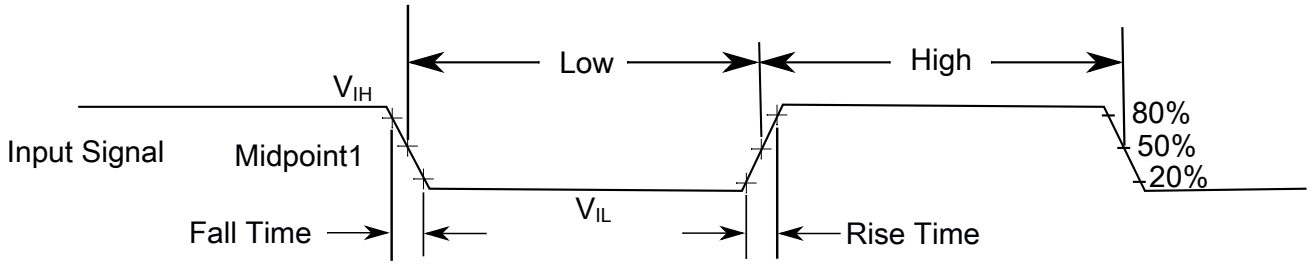

Figure 2. Input signal measurement reference

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	µs	
	• VLLS0 → RUN	—	—	173	µs	
	• VLLS1 → RUN	—	—	172	µs	
	• VLLS2 → RUN	—	—	96	µs	
	• VLLS3 → RUN	—	—	96	µs	
	• VLPS → RUN	—	—	5.4	µs	
	• STOP → RUN	—	—	5.4	µs	

2.2.5 Power consumption operating behaviors

NOTE

The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean+3σ)

Table 6. Power consumption operating behaviors (All IDDs are Target values)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash, excludes IDDA					Core frequency of 25 MHz.
	• @ 1.8V	—	6.8	17.2	mA	
	• @ 3.0V	—	6.9	17.4	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash, excludes IDDA					Core frequency of 50 MHz.
	• @ 1.8V • @ 3.0V	—	9.9	19.7	mA	

Table continues on the next page...

Table 6. Power consumption operating behaviors (All IDDs are Target values) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
		—	10.0	19.8	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash, excludes IDDA					Core frequency of 100 MHz.
	• @ 1.8V	—	17.0	25.9	mA	
	• @ 3.0V	—	17.2	26.1	mA	
I_{DD_HSRUN}	Run mode current — all peripheral clocks disabled, code executing from flash, excludes IDDA					Core frequency of 168 MHz.
	• @ 1.8V	—	26.3	45.3	mA	
	• @ 3.0V	—	26.5	45.5	mA	
I_{DD_HSRUN}	Run mode current — all peripheral clocks enabled, code executing from flash,excludes IDDA					Core frequency of 168 MHz. Nanoedge module at 84 MHz.
	• @ 3.0V					
	• @ 25°C	—	34.0	45.5	mA	
	• @ 105°C	—	39.0	53.2	mA	
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	8.9	—	mA	
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks disabled	—	0.58	—	mA	Core frequency of 4 Mhz.
I_{DD_VLPR}	Very-low-power run mode current at 3.0 V — all peripheral clocks enabled	—	0.83	—	mA	Core frequency of 4 Mhz.
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled	—	0.34	—	mA	Bus frequency of 2 MHz.
I_{DD_STOP}	Stop mode current at 3.0 V					
	• @ –40 to 25°C	—	0.43	2.03	mA	
	• @ 70°C	—	1.16	4.27	mA	
	• @ 105°C	—	3.05	10.13	mA	
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V					
	• @ –40 to 25°C	—	58	218	µA	
	• @ 70°C	—	280	1340	µA	
	• @ 105°C	—	924	2870	µA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V					
	• @ –40 to 25°C	—	2.8	5.3	µA	
	• @ 70°C	—	9.6	35.1	µA	
	• @ 105°C	—	37.4	134.8	µA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V					

Table continues on the next page...

Table 7. Low power mode peripheral adders — typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
		510	560	560	560	610	680	
I_{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	µA
I_{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							µA
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	
	OSCERCLK (4 MHz external crystal)	214	234	246	254	260	268	
I_{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx or VLLSx mode.	45	45	45	45	45	45	µA

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode, and BLPE for VLPR mode
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

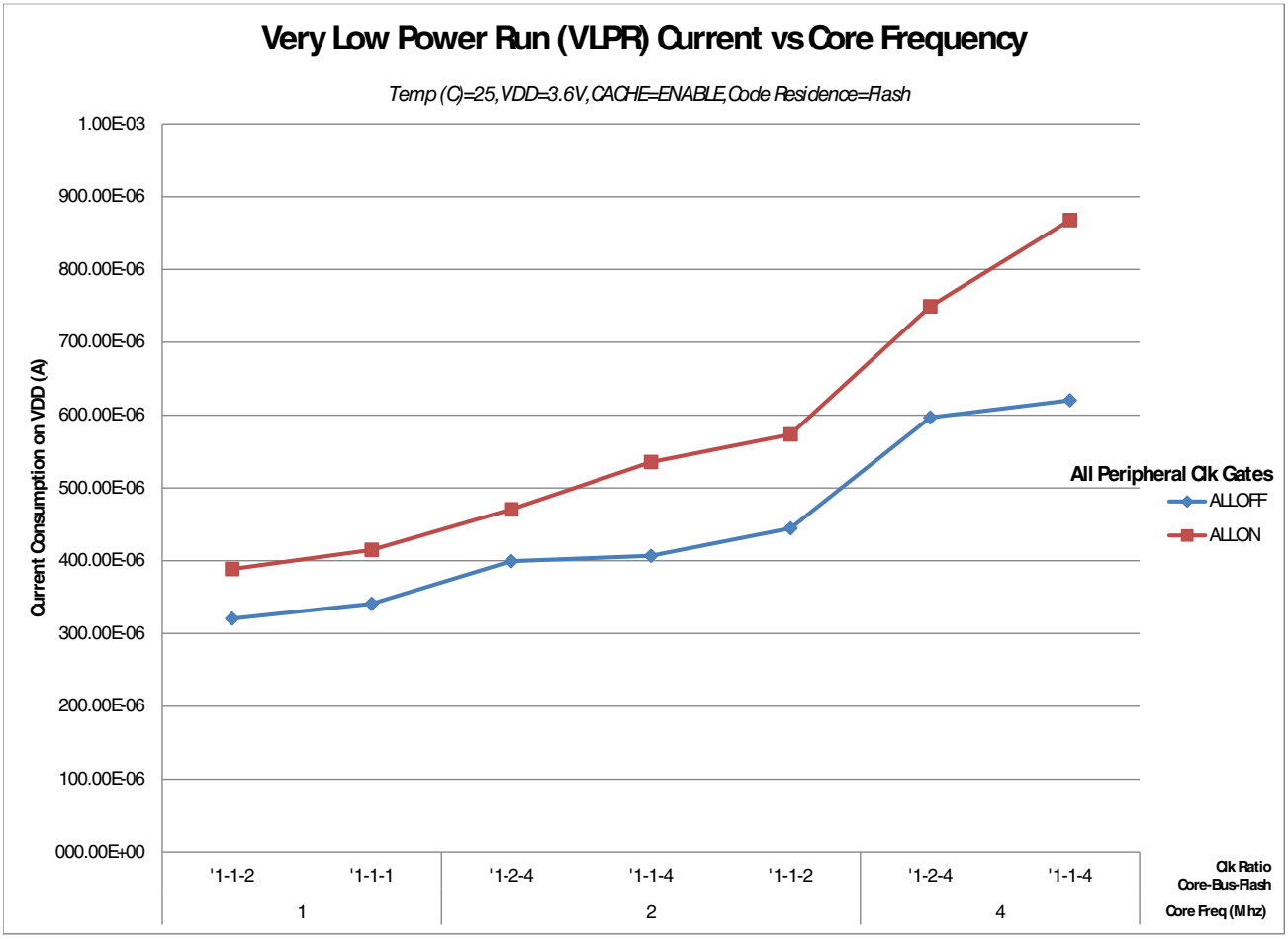

Figure 4. VLPR mode current vs. core frequency

2.2.6 EMC radiated emissions operating behaviors

NOTE

EMC measurements to IC-level IEC standards are available from NXP on request.

Table 8. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	20	dBµV	1, 2
V_{RE2}	Radiated emissions voltage, band 2	50–150	18	dBµV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	14	dBµV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	8	dBµV	
V_{RE_IEC}	IEC level	0.15–1000	L	—	2, 3

Table 10. Typical device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
f_{FPCK}	Fast peripheral clock	—	100	MHz	
f_{NANO}	Nano-edge clock	—	200	MHz	
Low Speed RUN mode					
f_{SYS}	System and core clock	—	50	MHz	
f_{BUS}	Bus and Flash clock	—	25	MHz	
f_{FPCK}	Fast peripheral clock	—	100	MHz	
f_{NANO}	Nano-edge clock	—	200	MHz	

NOTE

When NaneEdge circuit is enabled, the following clock set must be followed:

1. NanoEdge clock source must be from the PLL output
2. NanoEdge clock must be 2x the fast peripheral clock
3. NanoEdge clock must in the range of 164 Mhz ~232 Mhz

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and I^2C signals.

Table 11. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
	External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
	GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
	Port rise and fall time Fast slew rate 1.71≤ VDD ≤ 2.7 V 2.7 ≤ VDD ≤ 3.6 V	 — —	 8 7	 ns ns	3
	Port rise and fall time Slow slew rate 1.71≤ VDD ≤ 2.7 V 2.7 ≤ VDD ≤ 3.6 V	 — —	 25 15	 ns ns	

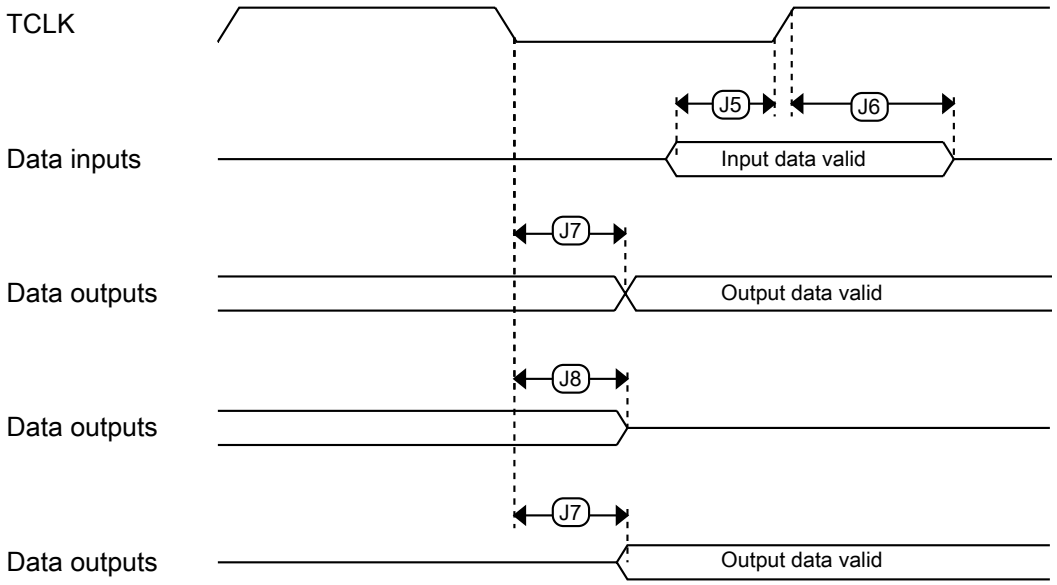

Figure 10. Boundary scan (JTAG) timing

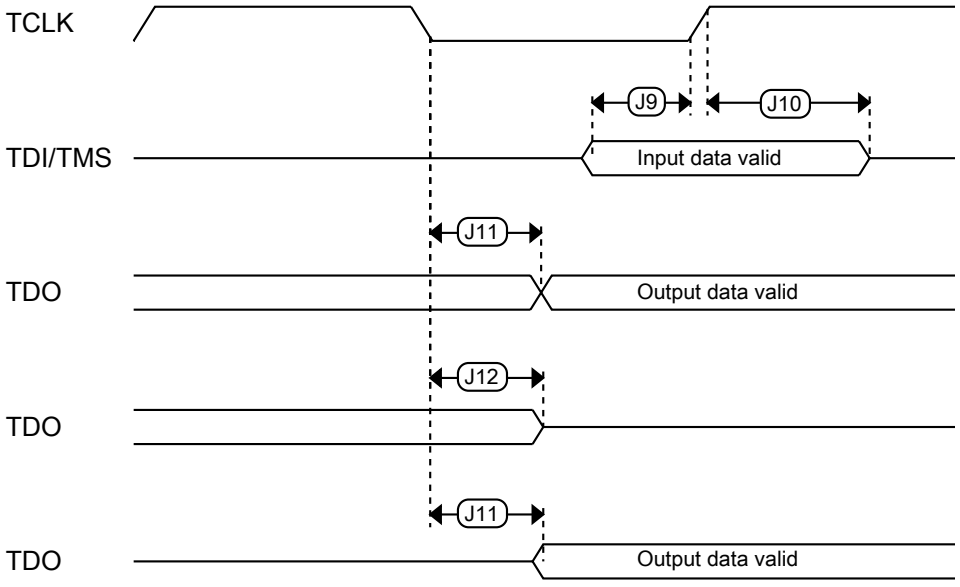

Figure 11. Test Access Port timing

Table 18. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• f_{vco} = 48 MHz	—	1350	—	ps	
	• f_{vco} = 120 MHz	—	600	—	ps	
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll\_ref})$	s	9

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a NXP developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.3.2 Oscillator electrical specifications

3.3.2.1 Oscillator DC electrical specifications

Table 19. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	µA	
	• 8 MHz	—	300	—	µA	
	• 16 MHz	—	950	—	µA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 4 MHz	—	400	—	µA	

Table continues on the next page...

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

3.6.1 12-bit cyclic Analog-to-Digital Converter (ADC) parameters

NOTE

The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean+3σ).

Table 25. 12-bit ADC electrical specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Recommended Operating Conditions					
Supply Voltage[1]	V_{DDA}	2.7	3.3	3.6	V
V_{refh} Supply Voltage[2]	Vrefhx	2.7		V_{DDA}	V
ADC Conversion Clock[3]	f_{ADCCLK}	0.6		25	MHz
Conversion Range	R_{AD}	V_{REFL}		V_{REFH}	V
Input Voltage Range External Reference Internal Reference	V_{ADIN}	 V_{REFL} V_{SSA}		 V_{REFH} V_{DDA}	V
Timing and Power					
Conversion Time	t_{ADC}		6		ADC Clock Cycles
ADC Power-Up Time (from adc_pdn)	t_{ADPU}		13		ADC Clock Cycles
ADC RUN Current (per ADC block) • at 600 kHz ADC Clock, LP mode • ≤ 8.33 MHz ADC Clock, 00 mode • ≤ 12.5 MHz ADC Clock, 01 mode • ≤ 16.67 MHz ADC Clock, 10 mode • ≤ 20 MHz ADC Clock, 11 mode • ≤ 25 MHz ADC Clock	I_{ADRUN}		 1 5.7 10.5 17.7 22.6 27.5		mA
ADC Powerdown Current (adc_pdn enabled)	$I_{ADPWRDWN}$		0.02		µA
V_{REFH} Current	I_{VREFH}		0.001		µA
Accuracy (DC or Absolute)					
Integral non-Linearity[4]	INL		+/- 3	+/- 5	LSB[5]
Differential non-Linearity[4]	DNL		+/- 0.6	+/- 0.9	LSB[5]

Table continues on the next page...

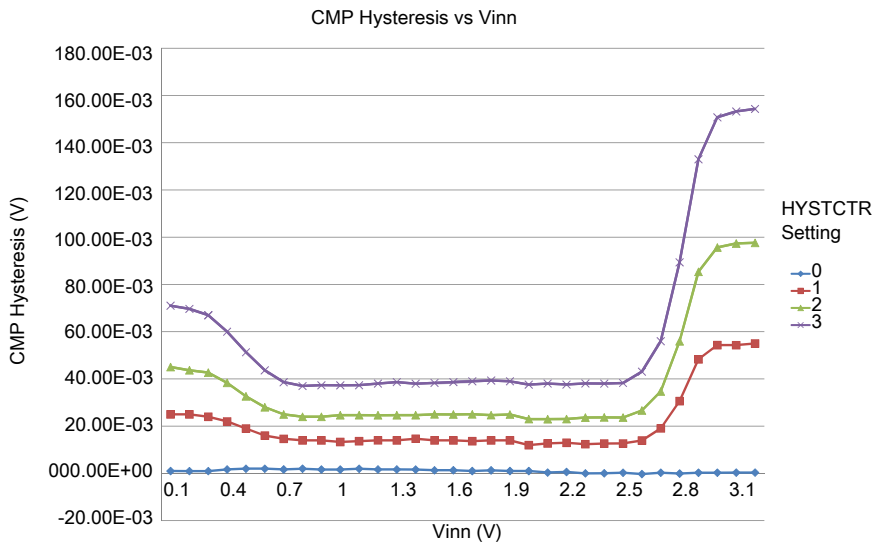

Figure 15. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 1)

3.6.3 12-bit DAC electrical characteristics

3.6.3.1 12-bit DAC operating requirements

Table 27. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REFH}.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

3.6.3.2 12-bit DAC operating behaviors

Table 28. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	330	µA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	1200	µA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	µs	1

Table continues on the next page...

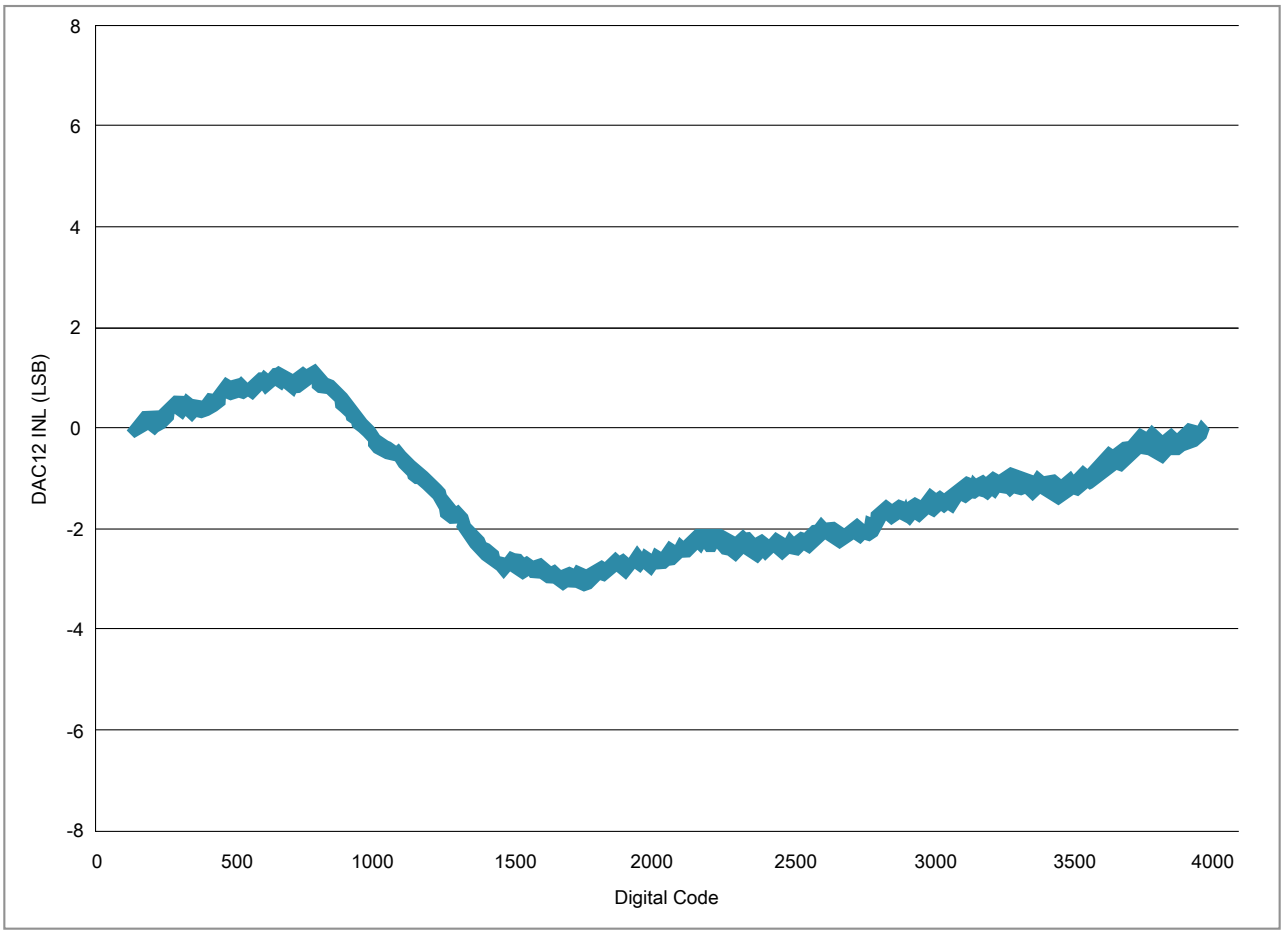

Figure 16. Typical INL error vs. digital code

Table 35. Slave mode DSPI timing for fast pads (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		25	MHz
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	17	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	11	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	11	ns

Table 36. Slave mode DSPI timing for open drain pads (limited voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	4 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) – 2	(t_{SCK}/2) + 2	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	28	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	22	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	22	ns

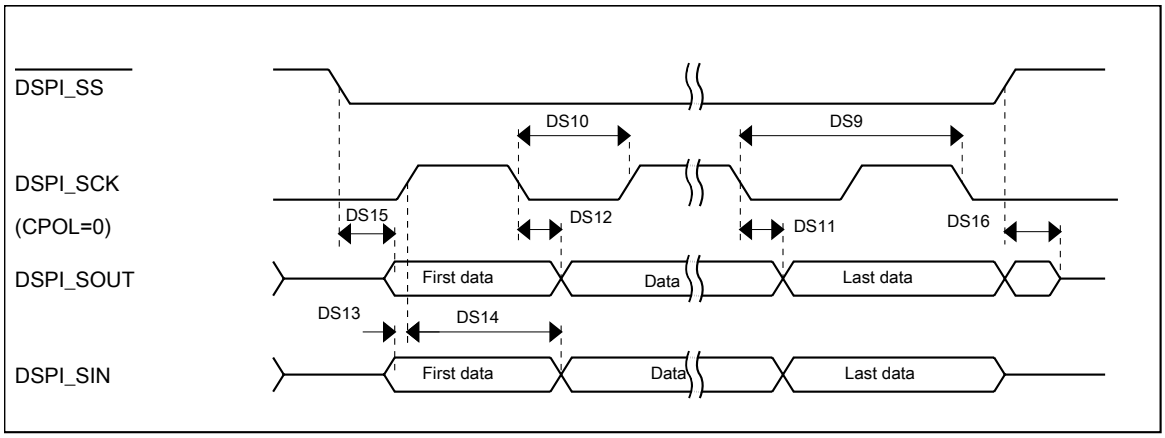

Figure 19. DSPI classic SPI timing — slave mode

Table 38. Master mode DSPI timing fast pads (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	4 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) - 4	($t_{SCK/2)}$ + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 4	—	ns	2
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 4	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-7.8	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	17	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

Table 39. Master mode DSPI timing open drain pads (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	18.75	MHz	
DS1	DSPI_SCK output cycle time	4 x t_{BUS}	—	ns	
DS2	DSPI_SCK output high/low time	(t_{SCK}/2) - 4	($t_{SCK/2)}$ + 4	ns	
DS3	DSPI_PCS*n* valid to DSPI_SCK delay	(t_{BUS} x 2) – 4	—	ns	2
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	(t_{BUS} x 2) – 4	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	26	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-7.8	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	24	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

Table 42. Slave mode DSPI timing for open drain pads (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	9.375	MHz
DS9	DSPI_SCK input cycle time	8 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t_{SCK}/2) - 4	($t_{SCK/2}$) + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	43.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.5	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	38	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	38	ns

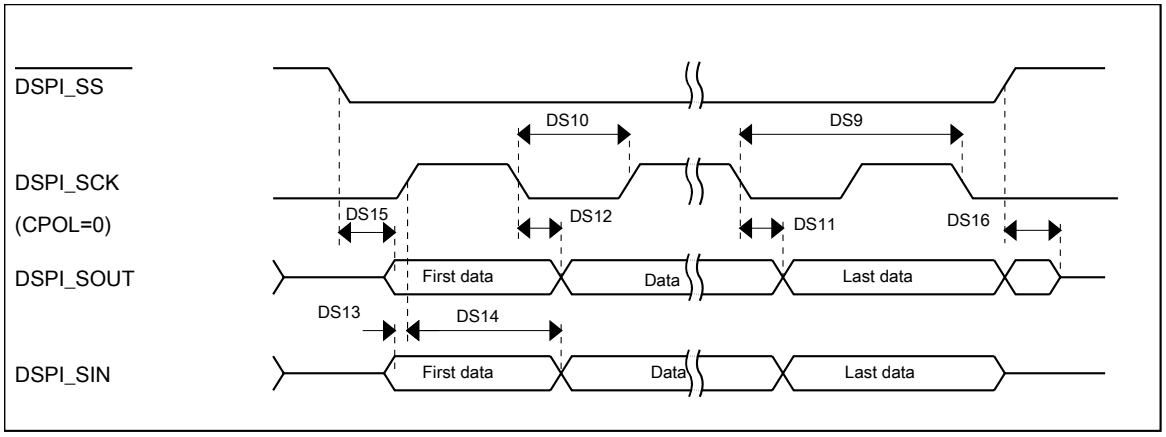

Figure 21. DSPI classic SPI timing — slave mode

3.9.3 I²C

See General switching specifications.

3.9.4 UART

See General switching specifications.

3.10 Kinetis Motor Suite (KMS)

100 LQFP	64 LQFP	48 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
55	37	29	PTB2	ADCA_CH6e/ CMP2_IN2	ADCA_CH6e/ CMP2_IN2	PTB2	I2C0_SCL	UART0_ RTS_b	FTM0_FLT1		FTM0_FLT3	
56	38	30	PTB3	ADCB_CH7e/ CMP3_IN5	ADCB_CH7e/ CMP3_IN5	PTB3	I2C0_SDA	UART0_ CTS_b/ UART0_ COL_b			FTM0_FLT0	
57	—	—	PTB9	DISABLED		PTB9						
58	—	—	PTB10	ADCB_CH6a	ADCB_CH6a	PTB10					FTM0_FLT1	
59	—	—	PTB11	ADCB_CH7a	ADCB_CH7a	PTB11					FTM0_FLT2	
60	—	—	VSS	VSS	VSS							
61	—	—	VDD	VDD	VDD							
62	39	31	PTB16	DISABLED		PTB16		UART0_RX	FTM_CLKIN2	CAN0_TX	EWM_IN	XBAR0_IN5
63	40	32	PTB17	DISABLED		PTB17		UART0_TX	FTM_CLKIN1	CAN0_RX	EWM_OUT_b	
64	41	—	PTB18	DISABLED		PTB18	CAN0_TX		FTM3_CH2			
65	42	—	PTB19	DISABLED		PTB19	CAN0_RX		FTM3_CH3			
66	—	—	PTB20	DISABLED		PTB20				FLEXPWMA_ X0	CMP0_OUT	
67	—	—	PTB21	DISABLED		PTB21				FLEXPWMA_ X1	CMP1_OUT	
68	—	—	PTB22	DISABLED		PTB22				FLEXPWMA_ X2	CMP2_OUT	
69	—	—	PTB23	DISABLED		PTB23		SPI0_PCS5		FLEXPWMA_ X3	CMP3_OUT	
70	43	33	PTC0	ADCB_CH6b	ADCB_CH6b	PTC0	SPI0_PCS4	PDB0_ EXTRG			FTM0_FLT1	SPI0_PCS0
71	44	34	PTC1/ LLWU_P6	ADCB_CH7b	ADCB_CH7b	PTC1/ LLWU_P6	SPI0_PCS3	UART1_ RTS_b	FTM0_CH0	FLEXPWMA_ A3	XBAR0_IN11	
72	45	35	PTC2	ADCB_CH6c/ CMP1_IN0	ADCB_CH6c/ CMP1_IN0	PTC2	SPI0_PCS2	UART1_ CTS_b	FTM0_CH1	FLEXPWMA_ B3	XBAR0_IN6	
73	46	36	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	FTM3_FLT0	
74	47	—	VSS	VSS	VSS							
75	48	—	VDD	VDD	VDD							
76	49	37	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT	
77	50	38	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2	XBAR0_IN2		CMP0_OUT	FTM0_CH2
78	51	39	PTC6/ LLWU_P10	CMP2_IN4/ CMP0_IN0	CMP2_IN4/ CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_ EXTRG	XBAR0_IN3	UART0_RX	XBAR0_ OUT6	I2C0_SCL
79	52	40	PTC7	CMP3_IN4/ CMP0_IN1	CMP3_IN4/ CMP0_IN1	PTC7	SPI0_SIN		XBAR0_IN4	UART0_TX	XBAR0_ OUT7	I2C0_SDA
80	53	—	PTC8	ADCB_CH7c/ CMP0_IN2	ADCB_CH7c/ CMP0_IN2	PTC8		FTM3_CH4				
81	54	—	PTC9	ADCB_CH6d/ CMP0_IN3	ADCB_CH6d/ CMP0_IN3	PTC9		FTM3_CH5				

100 LQFP	64 LQFP	48 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
82	55	—	PTC10	ADCB_CH7d	ADCB_CH7d	PTC10		FTM3_CH6				
83	56	—	PTC11/ LLWU_P11	ADCB_CH6e	ADCB_CH6e	PTC11/ LLWU_P11		FTM3_CH7				
84	—	—	PTC12	DISABLED		PTC12			FTM_CLKIN0		FTM3_FLT0	
85	—	—	PTC13	DISABLED		PTC13			FTM_CLKIN1			
86	—	—	PTC14	DISABLED		PTC14		I2C0_SCL				
87	—	—	PTC15	DISABLED		PTC15		I2C0_SDA				
88	—	—	VSS	VSS	VSS							
89	—	—	VDD	VDD	VDD							
90	—	—	PTC16	DISABLED		PTC16	CAN1_RX					
91	—	—	PTC17	DISABLED		PTC17	CAN1_TX					
92	—	—	PTC18	DISABLED		PTC18						
93	57	41	PTD0/ LLWU_P12	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0		FTM3_CH0	FTM0_CH0	FLEXPWMA_ A0	
94	58	42	PTD1	ADCA_CH7f	ADCA_CH7f	PTD1	SPI0_SCK		FTM3_CH1	FTM0_CH1	FLEXPWMA_ B0	
95	59	43	PTD2/ LLWU_P13	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT		FTM3_CH2	FTM0_CH2	FLEXPWMA_ A1	I2C0_SCL
96	60	44	PTD3	DISABLED		PTD3	SPI0_SIN		FTM3_CH3	FTM0_CH3	FLEXPWMA_ B1	I2C0_SDA
97	61	45	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI0_PCS1	UART0_ RTS_b	FTM0_CH4	FLEXPWMA_ A2	EWM_IN	SPI0_PCS0
98	62	46	PTD5	ADCA_CH6g	ADCA_CH6g	PTD5	SPI0_PCS2	UART0_ CTS_b/ UART0_ COL_b	FTM0_CH5	FLEXPWMA_ B2	EWM_OUT_b	SPI0_SCK
99	63	47	PTD6/ LLWU_P15	ADCA_CH7g	ADCA_CH7g	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6	FTM1_CH0	FTM0_FLT0	SPI0_SOUT
100	64	48	PTD7	DISABLED		PTD7		UART0_TX	FTM0_CH7	FTM1_CH1	FTM0_FLT1	SPI0_SIN

5.2 Pinout diagrams

The following diagrams show pinouts for the packages. For each pin, the diagrams show the default function. However, many signals may be multiplexed onto a single pin.

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the MKV4x device numbers.

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

Q KV## A FFF T PP CC S N

7.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
KV##	Kinetis family	• KV42 • KV44 • KV46
A	Key attribute	• F = Cortex-M4 w/ DSP and FPU
FFF	Program flash memory size	• 64 = 64 KB • 128 = 128 KB • 256 = 256 KB
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• LF = 48 LQFP (7 mm x 7 mm) • LH = 64 LQFP (10 mm x 10 mm) • LL = 100 LQFP (14 mm x 14 mm)
CC	Maximum CPU frequency (MHz)	• 16 = 168 MHz

Table continues on the next page...

Field	Description	Values
S	Software type	• P = KMS-PMSM and BLDC • (Blank) = Not software enabled
N	Packaging type	• R = Tape and reel • (Blank) = Trays

7.4 Example

This is an example part number:

MKV46F256VLL16

8 Terminology and guidelines

8.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

8.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

8.2 Definition: Operating behavior

Unless otherwise specified, an *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

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