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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	168MHz
Connectivity	CANbus, I ² C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 29x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mkv44f256vlh16

General

- Pin Group 4: XTAL, EXTAL
 - Pin Group 5: DAC analog output
2. Continuous clamp current per pin is -2.0 mA

2 General

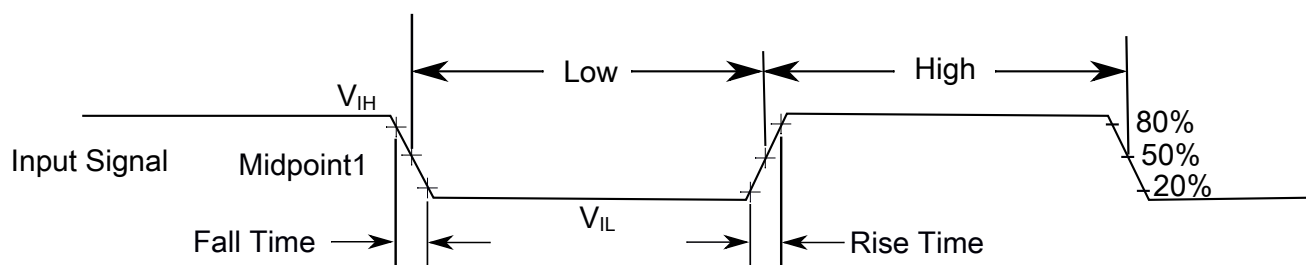
Electromagnetic compatibility (EMC) performance depends on the environment in which the MCU resides. Board design and layout, circuit topology choices, location, characteristics of external components, and MCU software operation play a significant role in EMC performance.

See the following applications notes available on nxp.com for guidelines on optimizing EMC performance.

- *AN2321: Designing for Board Level Electromagnetic Compatibility*
- *AN1050: Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers*
- *AN1263: Designing for Electromagnetic Compatibility with Single-Chip Microcontrollers*
- *AN2764: Improving the Transient Immunity Performance of Microcontroller-Based Applications*
- *AN1259: System Design and Layout Techniques for Noise Reduction in MCU-Based Systems*

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is $V_{IL} + (V_{IH} - V_{IL}) / 2$

Figure 2. Input signal measurement reference

General

- If the ADC is enabled, minimum V_{DD} is 2.7 V and minimum V_{DDA} is 2.7 V. ADCA and ADCB are not guaranteed to operate below 2.7 V. All other analog modules besides the ADC and Nano-edge will operate down to 1.71 V.
- If the Nano-edge is enabled, minimum V_{DD} is 3.0 V and minimum V_{DDA} is 3.0 V. Nano-edge is not guaranteed to operate below 3.0 V. All other analog modules besides the ADC and Nano-edge will operate down to 1.71 V.

2.2.2 LVD and POR operating requirements

Table 3. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling V_{DD} POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
V_{LVW1H}	Low-voltage warning thresholds — high range					1
	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
V_{LVW1L}	Low-voltage warning thresholds — low range					1
	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

- Rising thresholds are falling threshold + hysteresis voltage

2.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{OH}	Output high voltage — normal drive pad					
		$V_{DD} - 0.5$	—	—	V	
		$V_{DD} - 0.5$	—	—	V	

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -10\text{mA}$ $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -5\text{mA}$					
	Output high voltage — High drive pad					1
	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = -20\text{mA}$ $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = -10\text{mA}$	$V_{DD} - 0.5$	—	—	V	
		$V_{DD} - 0.5$	—	—	V	
I_{OHT}	Output high current total for all ports	—	—	100	mA	
V_{OL}	Output low voltage — open drain pad	—	—	0.5	V	2
	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OH} = 3\text{ mA}$ $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OH} = 1\text{ mA}$	—	—	0.5	V	
V_{OL}	Output low voltage — normal drive pad	—	—	0.5	V	
	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 10\text{ mA}$ $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 5\text{ mA}$	—	—	0.5	V	
	Output low voltage — high drive pad	—	—	0.5	V	1
	$2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$, $I_{OL} = 20\text{ mA}$ $1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}$, $I_{OL} = 10\text{ mA}$	—	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	—	100	mA	
I_{IN}	Input leakage current, analog and digital pins $V_{SS} \leq V_{IN} \leq V_{DD}$	—	0.002	0.5	μA	3
R_{PU}	Internal pullup resistors(except RTC_WAKEUP pins)	20	—	50	$\text{k}\Omega$	4
R_{PD}	Internal pulldown resistors	20	—	50	$\text{k}\Omega$	5

1. High drive pads are PTB0, PTB1, PTC3, PTC4, PTD4, PTD5, PTD6 and PTD7.

2. Open drain pads are PTC6 and PTC7.

3. Measured at $V_{DD}=3.6\text{V}$

4. Measured at V_{DD} supply voltage = V_{DD} min and $V_{input} = V_{SS}$

5. Measured at V_{DD} supply voltage = V_{DD} min and $V_{input} = V_{DD}$

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and $VLLSx \rightarrow \text{RUN}$ recovery times in the following table assume this clock configuration:

- CPU and system clocks = 100 MHz
- Bus and flash clock = 25 MHz
- FEI clock mode

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	μs	
	• VLLS0 → RUN	—	—	173	μs	
	• VLLS1 → RUN	—	—	172	μs	
	• VLLS2 → RUN	—	—	96	μs	
	• VLLS3 → RUN	—	—	96	μs	
	• VLPS → RUN	—	—	5.4	μs	
	• STOP → RUN	—	—	5.4	μs	

2.2.5 Power consumption operating behaviors

NOTE

The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean+3 σ)

Table 6. Power consumption operating behaviors (All IDD's are Target values)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash, excludes IDDA					Core frequency of 25 MHz.
	• @ 1.8V	—	6.8	17.2	mA	
	• @ 3.0V	—	6.9	17.4	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash, excludes IDDA					Core frequency of 50 MHz.
	• @ 1.8V					
	• @ 3.0V	—	9.9	19.7	mA	

Table continues on the next page...

Table 7. Low power mode peripheral adders — typical value (continued)

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
		510	560	560	560	610	680	
I _{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	μA
I _{UART}	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							μA
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	
	OSCERCLK (4 MHz external crystal)	214	234	246	254	260	268	
I _{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx or VLLSx mode.	45	45	45	45	45	45	μA

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode, and BLPE for VLPR mode
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA

Table 10. Typical device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
f _{FPCK}	Fast peripheral clock	—	100	MHz	
f _{NANO}	Nano-edge clock	—	200	MHz	
Low Speed RUN mode					
f _{SYS}	System and core clock	—	50	MHz	
f _{BUS}	Bus and Flash clock	—	25	MHz	
f _{FPCK}	Fast peripheral clock	—	100	MHz	
f _{NANO}	Nano-edge clock	—	200	MHz	

NOTE

When NaneEdge circuit is enabled, the following clock set must be followed:

1. NanoEdge clock source must be from the PLL output
2. NanoEdge clock must be 2x the fast peripheral clock
3. NanoEdge clock must in the range of 164 Mhz ~232 Mhz

2.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and I²C signals.

Table 11. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
	External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
	GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
	Port rise and fall time				3
	Fast slew rate				
	1.71 ≤ VDD ≤ 2.7 V	—	8	ns	
	2.7 ≤ VDD ≤ 3.6 V	—	7	ns	
	Port rise and fall time				
	Slow slew rate				
	1.71 ≤ VDD ≤ 2.7 V	—	25	ns	
	2.7 ≤ VDD ≤ 3.6 V	—	15	ns	

4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

3 Peripheral operating requirements and behaviors

3.1 Core modules

3.1.1 SWD Electricals

Table 14. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation Serial wire debug	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

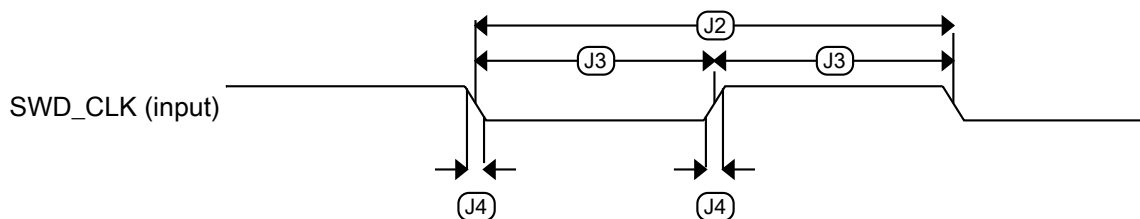


Figure 5. Serial wire clock input timing

Table 18. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f _{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f _{ints_t}	—	—	kHz	
FLL							
f _{fil_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f _{dco}	DCO output frequency range	Low range (DRS=00) 640 × f _{fil_ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f _{fil_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f _{fil_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f _{fil_ref}	80	83.89	100	MHz	
f _{dco_t_DMx3_2}	DCO output frequency	Low range (DRS=00) 732 × f _{fil_ref}	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) 1464 × f _{fil_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f _{fil_ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f _{fil_ref}	—	95.98	—	MHz	
J _{cyc_fll}	FLL period jitter		—	180	—	ps	
	- f_{DCO} = 48 MHz - f_{DCO} = 98 MHz		—	150	—		
t _{fil_acquire}	FLL target frequency acquisition time		—	—	1	ms	6
PLL							
f _{pll_ref}	PLL reference frequency range		8	—	16	MHz	
f _{vcoclk_2x}	VCO output frequency		220	—	480	MHz	
f _{vcoclk}	PLL output frequency		110	—	240	MHz	
f _{vcoclk_90}	PLL quadrature output frequency		110	—	240	MHz	
I _{pll}	PLL operating current VCO @ 176 MHz (f_{osc_hi_1} = 32 MHz, f_{pll_ref} = 8 MHz, VDIV multiplier = 22)		—	2.8	—	mA	7
I _{pll}	PLL operating current VCO @ 360 MHz (f_{osc_hi_1} = 32 MHz, f_{pll_ref} = 8 MHz, VDIV multiplier = 45)		—	4.7	—	mA	7
J _{cyc_pll}	PLL period jitter (RMS)						8
	- f_{vco} = 48 MHz - f_{vco} = 120 MHz		— —	120 75	— —	ps ps	
J _{acc_pll}	PLL accumulated jitter over 1μs (RMS)						8

Table continues on the next page...

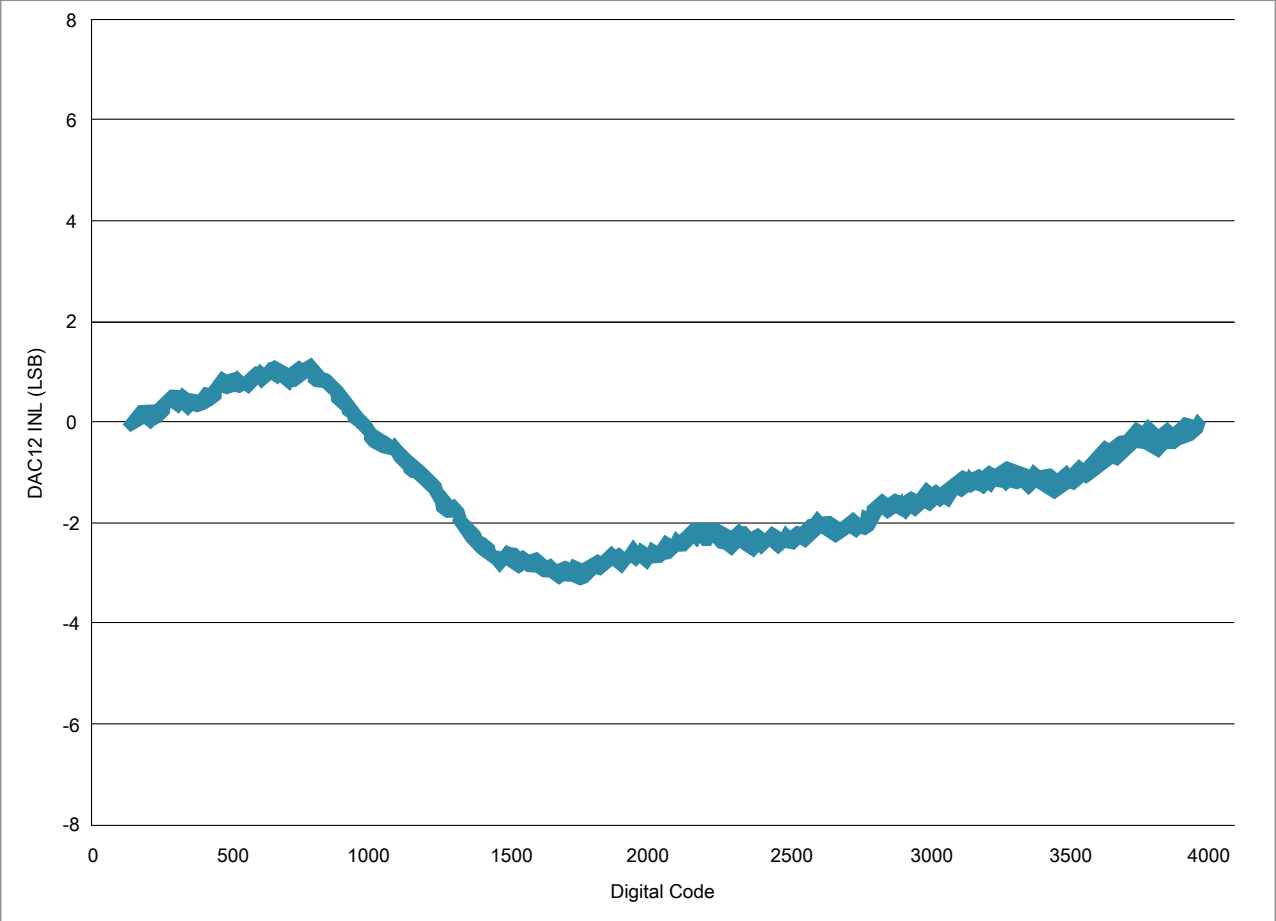


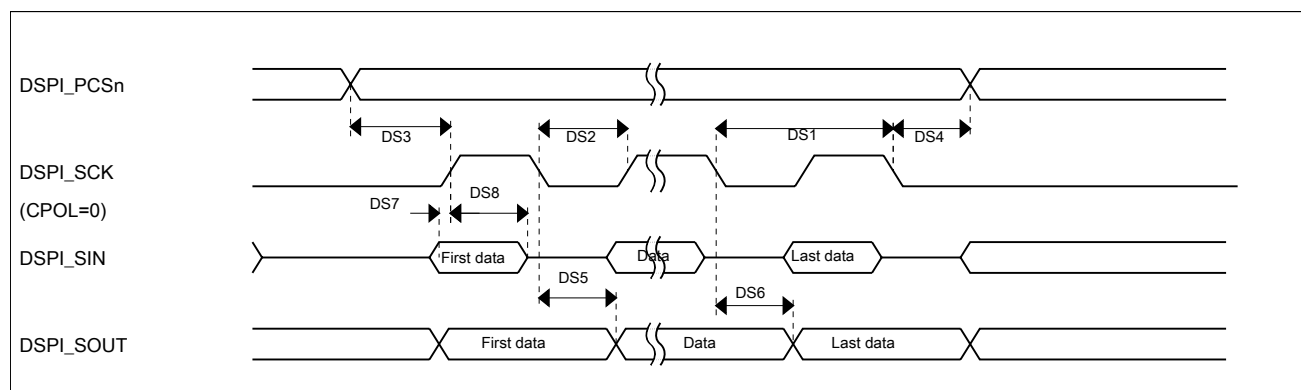
Figure 16. Typical INL error vs. digital code

Table 33. Master mode DSPI timing for open drain pads (limited voltage range) (continued)

Num	Description	Min.	Max.	Unit	Notes
	Frequency of operation	—	25	MHz	
DS1	DSPI_SCK output cycle time	$2 \times t_{\text{BUS}}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{\text{SCK}}/2) - 2$	$(t_{\text{SCK}}/2) + 2$	ns	
DS3	DSPI_PCSn to DSPI_SCK output valid	$(t_{\text{BUS}} \times 2) - 2$	—	ns	1
DS4	DSPI_SCK to DSPI_PCSn output hold	$(t_{\text{BUS}} \times 2) - 2$	—	ns	2
DS5	DSPI_SCK to DSPI_SOUT valid	—	15.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	—3	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	17	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].

2. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

**Figure 18. DSPI classic SPI timing — master mode****Table 34. Slave mode DSPI timing for normal pads (limited voltage range)**

Num	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
	Frequency of operation		12.5	MHz
DS9	DSPI_SCK input cycle time	$4 \times t_{\text{BUS}}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{\text{SCK}}/2) - 2$	$(t_{\text{SCK}}/2) + 2$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	21	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	15	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	15	ns

3.9.2 SPI (DSPI) switching specifications (full voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provides DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

NOTE

Fast pads:

- SIN: PTE19
- SOUT: PTE18
- SCK: PTE17
- PCS: PTE16

Open drain pads:

- SIN: PTC7
- SOUT: PTC6

Table 37. Master mode DSPI timing for normal pads (full voltage range)

Num	Description	Min.	Max.	Unit	Notes
	Operating voltage	1.71	3.6	V	1
	Frequency of operation	—	18.75	MHz	
DS1	DSPI_SCK output cycle time	$4 \times t_{BUS}$	—	ns	
DS2	DSPI_SCK output high/low time	$(t_{SCK}/2) - 4$	$(t_{SCK}/2) + 4$	ns	
DS3	DSPI_PCS _n valid to DSPI_SCK delay	$(t_{BUS} \times 2) - 4$	—	ns	2
DS4	DSPI_SCK to DSPI_PCS _n invalid delay	$(t_{BUS} \times 2) - 4$	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-7.8	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	24	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

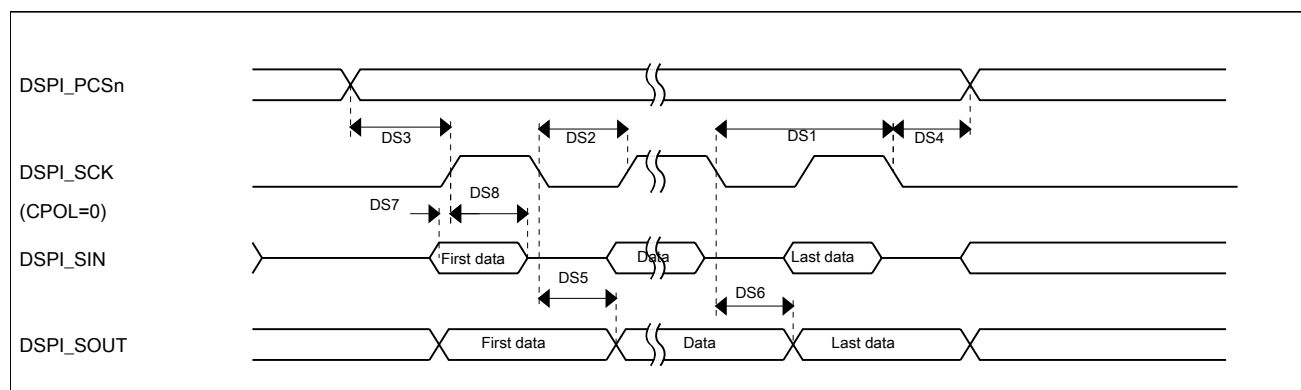


Figure 20. DSPI classic SPI timing — master mode

Table 40. Slave mode DSPI timing for normal pads (full voltage range)

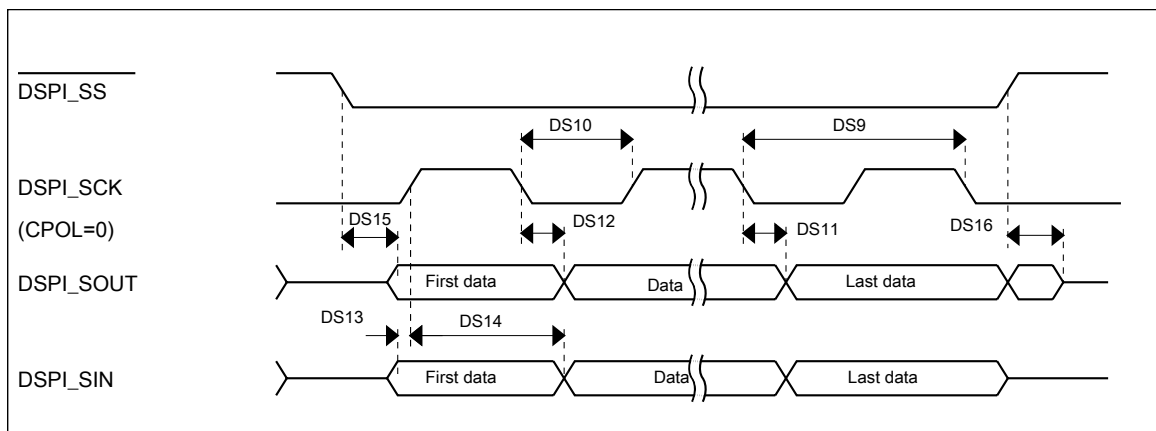
Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	12.5	MHz
DS9	DSPI_SCK input cycle time	$8 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 4$	$(t_{SCK}/2) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	27.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.5	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	22	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	22	ns

Table 41. Slave mode DSPI timing for fast pads (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	18.75	MHz
DS9	DSPI_SCK input cycle time	$8 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 4$	$(t_{SCK}/2) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.5	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	15	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	15	ns

Table 42. Slave mode DSPI timing for open drain pads (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	9.375	MHz
DS9	DSPI_SCK input cycle time	$8 \times t_{\text{BUS}}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{\text{SCK}}/2) - 4$	$(t_{\text{SCK}}/2) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	43.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.5	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	—	38	ns </td
DS16	DSPI_SS inactive to DSPI_SOUT not driven	—	38	ns

**Figure 21. DSPI classic SPI timing — slave mode**

3.9.3 I²C

See [General switching specifications](#).

3.9.4 UART

See [General switching specifications](#).

3.10 Kinetis Motor Suite (KMS)

Dimensions

Kinetis Motor Suite is a bundled software solution that enables the rapid configuration of motor drive systems, and accelerates development of the final motor drive application.

Several members of the KV4x family are enabled with Kinetis Motor Suite. The enabled devices can be identified within the orderable part numbers in [KMS Orderable part numbers summary](#). For more information, see Kinetis Motor Suite User's Guide (KMS100UG) and Kinetis Motor Suite API Reference Manual (KMS100RM).

NOTE

To find the associated resource, go to <http://www.nxp.com> and perform a search using the Document ID.

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to www.nxp.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
48-pin LQFP	98ASH00962A
64-pin LQFP	98ASS23234W
100-pin LQFP	98ASS23308W

5 Pinout

5.1 KV4x Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

Pinout

100 LQFP	64 LQFP	48 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
30	—	—	VDD	VDD	VDD							
31	20	15	PTE24	ADCB_CH4	ADCB_CH4	PTE24	CAN1_TX	FTM0_CH0	XBAR0_IN2	I2C0_SCL	EWM_OUT_b	XBAR0_OUT4
32	21	16	PTE25/ LLWU_P21	ADCB_CH5	ADCB_CH5	PTE25/ LLWU_P21	CAN1_RX	FTM0_CH1	XBAR0_IN3	I2C0_SDA	EWM_IN	XBAR0_OUT5
33	—	—	PTE26	DISABLED		PTE26						
34	22	17	PTA0	JTAG_TCLK/ SWD_CLK		PTA0	UART0_CTS_b/ UART0_COL_b	FTM0_CH5	XBAR0_IN4	EWM_IN		JTAG_TCLK/ SWD_CLK
35	23	18	PTA1	JTAG_TDI		PTA1	UART0_RX	FTM0_CH6	CMP0_OUT		FTM1_CH1	JTAG_TDI
36	24	19	PTA2	JTAG_TDO/ TRACE_SWO		PTA2	UART0_TX	FTM0_CH7	CMP1_OUT		FTM1_CH0	JTAG_TDO/ TRACE_SWO
37	25	20	PTA3	JTAG_TMS/ SWD_DIO		PTA3	UART0_RTS_b	FTM0_CH0	XBAR0_IN9	EWM_OUT_b	FLEXPWMA_A0	JTAG_TMS/ SWD_DIO
38	26	21	PTA4/ LLWU_P3	NMI_b		PTA4/ LLWU_P3		FTM0_CH1	XBAR0_IN10	FTM0_FLT3	FLEXPWMA_B0	NMI_b
39	27	—	PTA5	DISABLED		PTA5		FTM0_CH2		CMP2_OUT		JTAG_TRST_b
40	—	22	VDD	VDD	VDD							
41	—	23	VSS	VSS	VSS							
42	28	—	PTA12	CMP2_IN0	CMP2_IN0	PTA12	CAN0_TX	FTM1_CH0				FTM1_QD_PHA
43	29	—	PTA13/ LLWU_P4	CMP2_IN1	CMP2_IN1	PTA13/ LLWU_P4	CAN0_RX	FTM1_CH1				FTM1_QD_PHB
44	—	—	PTA14	CMP3_IN0	CMP3_IN0	PTA14	SPI0_PCS0	UART0_TX				
45	—	—	PTA15	CMP3_IN1	CMP3_IN1	PTA15	SPI0_SCK	UART0_RX				
46	—	—	PTA16	CMP3_IN2	CMP3_IN2	PTA16	SPI0_SOUT	UART0_CTS_b/ UART0_COL_b				
47	—	—	PTA17	ADCA_CH7e	ADCA_CH7e	PTA17	SPI0_SIN	UART0_RTS_b				
48	30	—	VDD	VDD	VDD							
49	31	—	VSS	VSS	VSS							
50	32	24	PTA18	EXTAL0	EXTAL0	PTA18	XBAR0_IN7	FTM0_FLT2	FTM_CLKIN0	XBAR0_OUT8	FTM3_CH2	
51	33	25	PTA19	XTAL0	XTAL0	PTA19	XBAR0_IN8	FTM1_FLT0	FTM_CLKIN1	XBAR0_OUT9	LPTMR0_ALT1	
52	34	26	RESET_b	RESET_b	RESET_b							
53	35	27	PTB0/ LLWU_P5	ADCB_CH2	ADCB_CH2	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_PHA	UART0_RX
54	36	28	PTB1	ADCB_CH3	ADCB_CH3	PTB1	I2C0_SDA	FTM1_CH1	FTM0_FLT2	EWM_IN	FTM1_QD_PHB	UART0_TX

Pinout

100 LQFP	64 LQFP	48 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
82	55	—	PTC10	ADCB_CH7d	ADCB_CH7d	PTC10		FTM3_CH6				
83	56	—	PTC11/ LLWU_P11	ADCB_CH6e	ADCB_CH6e	PTC11/ LLWU_P11		FTM3_CH7				
84	—	—	PTC12	DISABLED		PTC12			FTM_CLKIN0		FTM3_FLT0	
85	—	—	PTC13	DISABLED		PTC13			FTM_CLKIN1			
86	—	—	PTC14	DISABLED		PTC14		I2C0_SCL				
87	—	—	PTC15	DISABLED		PTC15		I2C0_SDA				
88	—	—	VSS	VSS	VSS							
89	—	—	VDD	VDD	VDD							
90	—	—	PTC16	DISABLED		PTC16	CAN1_RX					
91	—	—	PTC17	DISABLED		PTC17	CAN1_TX					
92	—	—	PTC18	DISABLED		PTC18						
93	57	41	PTD0/ LLWU_P12	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0		FTM3_CH0	FTM0_CH0	FLEXPWMA_ A0	
94	58	42	PTD1	ADCA_CH7f	ADCA_CH7f	PTD1	SPI0_SCK		FTM3_CH1	FTM0_CH1	FLEXPWMA_ B0	
95	59	43	PTD2/ LLWU_P13	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT		FTM3_CH2	FTM0_CH2	FLEXPWMA_ A1	I2C0_SCL
96	60	44	PTD3	DISABLED		PTD3	SPI0_SIN		FTM3_CH3	FTM0_CH3	FLEXPWMA_ B1	I2C0_SDA
97	61	45	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI0_PCS1	UART0_ RTS_b	FTM0_CH4	FLEXPWMA_ A2	EWM_IN	SPI0_PCS0
98	62	46	PTD5	ADCA_CH6g	ADCA_CH6g	PTD5	SPI0_PCS2	UART0_ CTS_b/ UART0_ COL_b	FTM0_CH5	FLEXPWMA_ B2	EWM_OUT_b	SPI0_SCK
99	63	47	PTD6/ LLWU_P15	ADCA_CH7g	ADCA_CH7g	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6	FTM1_CH0	FTM0_FLT0	SPI0_SOUT
100	64	48	PTD7	DISABLED		PTD7		UART0_TX	FTM0_CH7	FTM1_CH1	FTM0_FLT1	SPI0_SIN

5.2 Pinout diagrams

The following diagrams show pinouts for the packages. For each pin, the diagrams show the default function. However, many signals may be multiplexed onto a single pin.

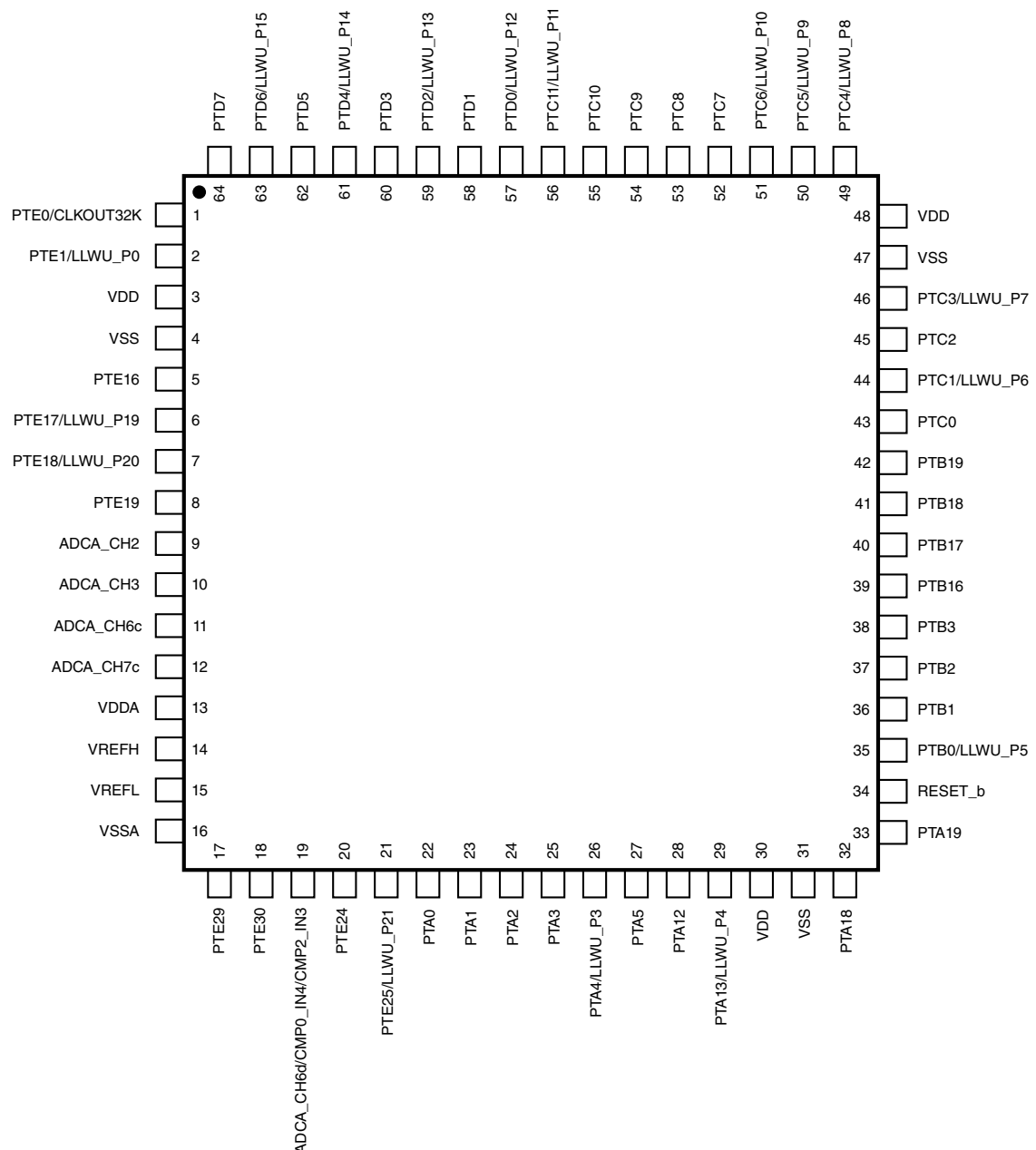
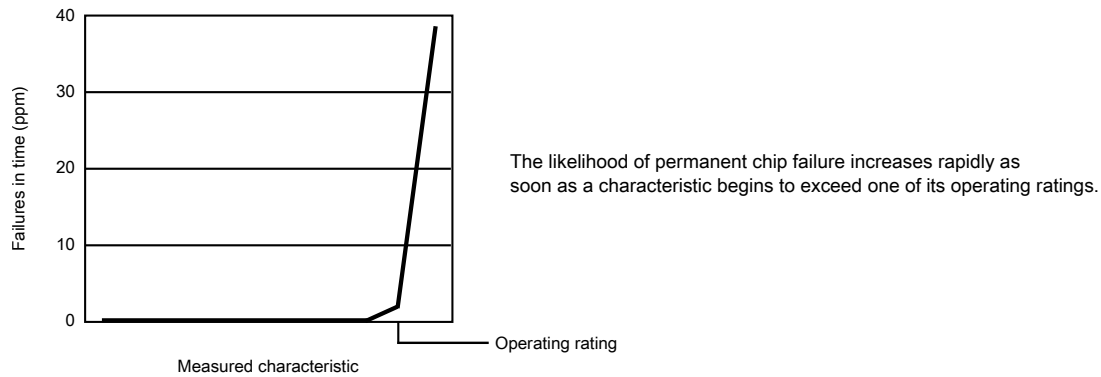
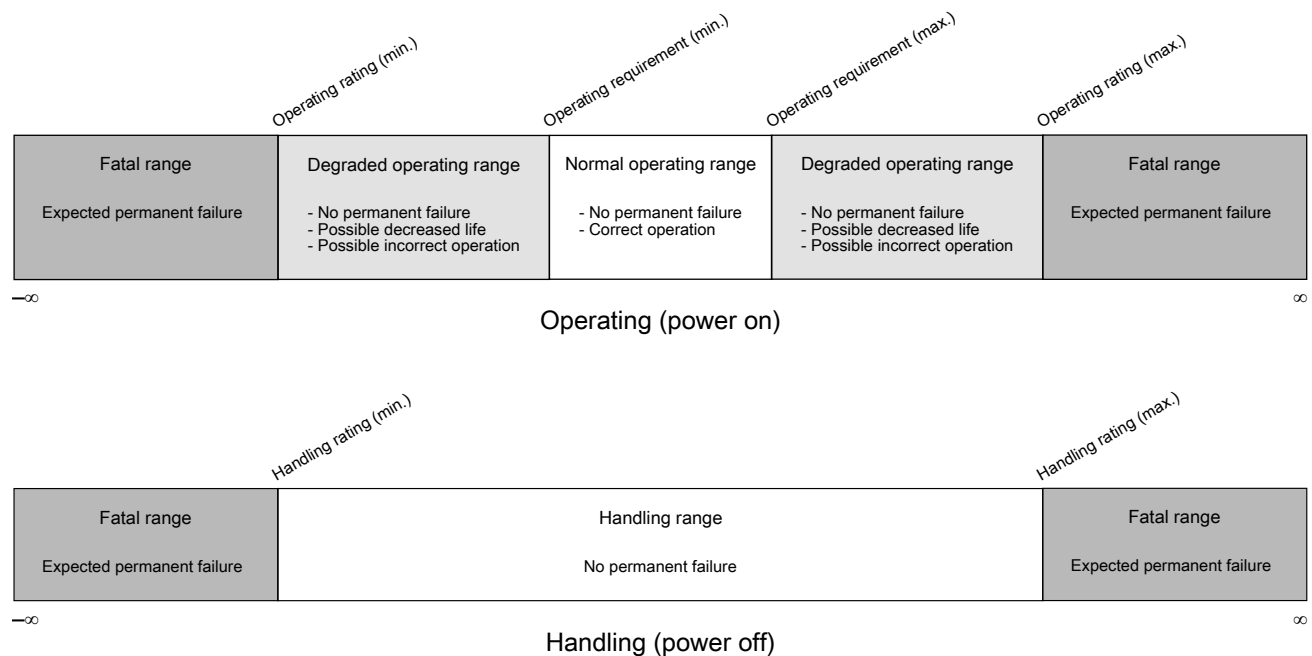


Figure 23. 64-pin LQFP

8.5 Result of exceeding a rating



8.6 Relationship between ratings and operating requirements



8.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.

- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

8.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

8.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	μA

8.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:

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