What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	168MHz
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	48
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 29x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkv46f256vlh16

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	μs	
	• VLLS0 → RUN	—	—	173	μs	
	• VLLS1 → RUN	—	—	172	μs	
	• VLLS2 → RUN	—	—	96	μs	
	• VLLS3 → RUN	—	—	96	μs	
	• VLPS → RUN	—	—	5.4	μs	
	• STOP → RUN	—	—	5.4	μs	

2.2.5 Power consumption operating behaviors

NOTE

The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean+3σ)

Table 6. Power consumption operating behaviors (All IDDs are Target values)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash, excludes IDDA • @ 1.8V • @ 3.0V	— —	6.8 6.9	17.2 17.4	mA mA	Core frequency of 25 MHz.
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash, excludes IDDA • @ 1.8V • @ 3.0V	—	9.9	19.7	mA	Core frequency of 50 MHz.

Table continues on the next page...

Table 6. Power consumption operating behaviors (All IDDs are Target values) (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• @ –40 to 25°C	—	2.7	3.3	μA	
	• @ 70°C	—	6.6	12.2	μA	
	• @ 105°C	—	25.9	50.5	μA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V					
	• @ –40 to 25°C	—	740	1200	nA	
	• @ 70°C	—	2.5	10.6	μA	
	• @ 105°C	—	11.1	26.5	μA	
I_{DD_VLLS0B}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled					
	• @ –40 to 25°C	—	420	832	nA	
	• @ 70°C	—	1.9	9.4	μA	
	• @ 105°C	—	10.8	26.3	μA	
I_{DD_VLLS0A}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled					
	• @ –40 to 25°C	—	200	599	nA	
	• @ 70°C	—	1.8	10.5	μA	
	• @ 105°C	—	10.8	26.3	μA	

Table 7. Low power mode peripheral adders — typical value

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{IREFSTEN4MHz}$	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	μA
$I_{IREFSTEN32KHz}$	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	μA
$I_{EREFSTEN4MHz}$	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	206	228	237	245	251	258	uA
$I_{EREFSTEN32KHz}$	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.							nA
	VLLS1							
	VLLS3	440	490	540	560	570	580	
	VLPS	440	490	540	560	570	580	
	STOP	510	560	560	560	610	680	

Table continues on the next page...

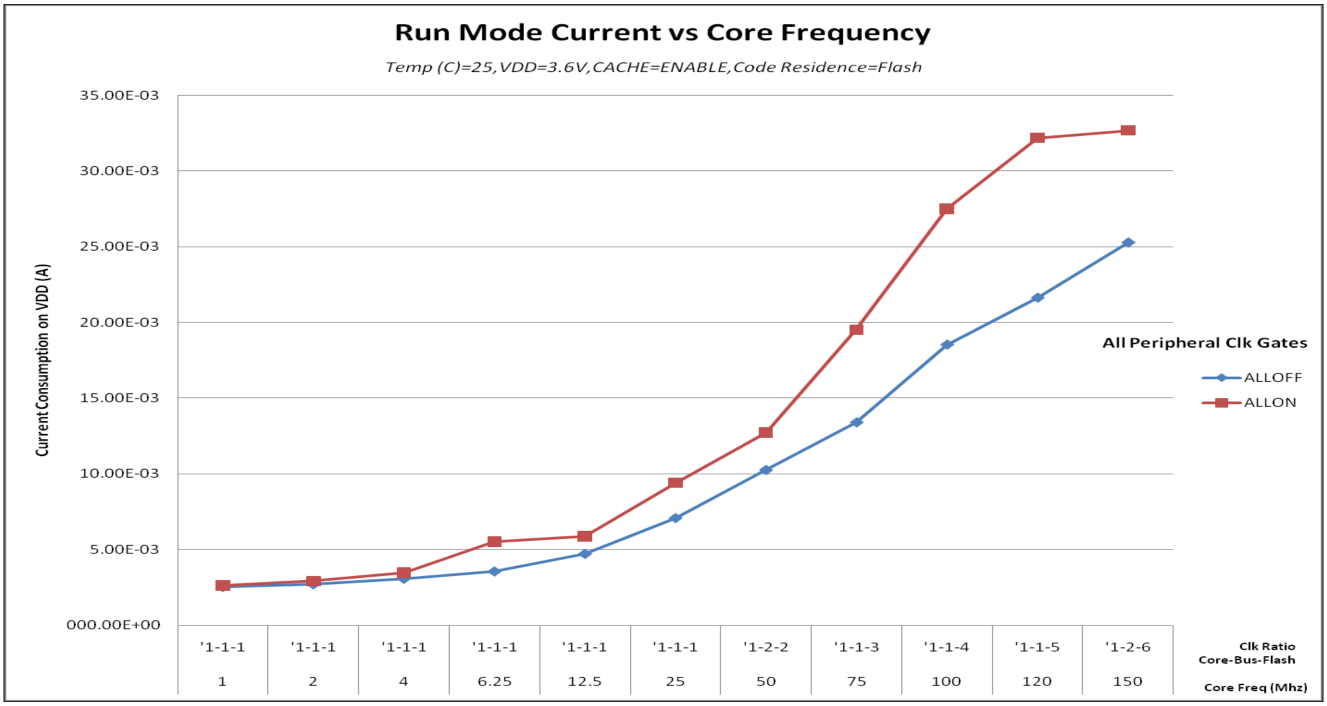


Figure 3. Run mode supply current vs. core frequency

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.
2. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = 10 MHz (crystal), f_{SYS} = 75 MHz, f_{BUS} = 25 MHz
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.nxp.com.
2. Perform a keyword search for “EMC design.”

2.2.8 Capacitance attributes

Table 9. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

2.3 Switching specifications

2.3.1 Typical device clock specifications

Table 10. Typical device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
High Speed RUN mode					
f_{SYS}	System and core clock	—	168	MHz	
f_{BUS}	Bus and Flash clock	—	24	MHz	
f_{FPCK}	Fast peripheral clock	—	84	MHz	
f_{NANO}	Nano-edge clock	—	168	MHz	
Normal run mode					
f_{SYS}	System and core clock	—	100	MHz	
f_{BUS}	Bus and Flash clock	—	25	MHz	

Table continues on the next page...

Table 16. JTAG limited voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J11	TCLK low to TDO data valid	—	19	ns
J12	TCLK low to TDO high-Z	—	17	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

Table 17. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation • Boundary Scan • JTAG and CJTAG • Serial Wire Debug	 0 0 0	 10 20 40	MHz
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width • Boundary Scan • JTAG and CJTAG • Serial Wire Debug	 50 25 12.5	 — — —	 ns ns ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	2.0	—	ns
J7	TCLK low to boundary scan output data valid	—	30.6	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.0	—	ns
J11	TCLK low to TDO data valid	—	19.0	ns
J12	TCLK low to TDO high-Z	—	17.0	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

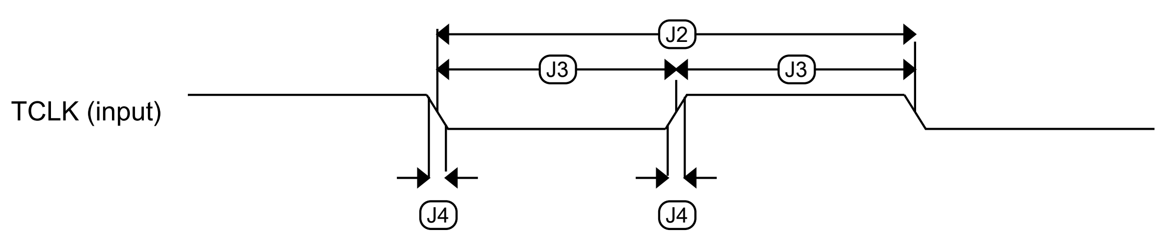


Figure 9. Test clock input timing

Table 18. MCG specifications (continued)

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
			FLL				
f_{fll_ref}	FLL reference frequency range		31.25	—	39.0625	kHz	
f_{dco}	DCO output frequency range	Low range (DRS=00) 640 × f_{fll_ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f_{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f_{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f_{fll_ref}	80	83.89	100	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS=00) 732 × f_{fll_ref}	—	23.99	—	MHz	4, 5
		Mid range (DRS=01) 1464 × f_{fll_ref}	—	47.97	—	MHz	
		Mid-high range (DRS=10) 2197 × f_{fll_ref}	—	71.99	—	MHz	
		High range (DRS=11) 2929 × f_{fll_ref}	—	95.98	—	MHz	
J_{cyc_fll}	FLL period jitter • f_{DCO} = 48 MHz • f_{DCO} = 98 MHz		— —	180 150	— —	ps	
$t_{fll\_acquire}$	FLL target frequency acquisition time		—	—	1	ms	6
			PLL				
f_{pll_ref}	PLL reference frequency range		8	—	16	MHz	
f_{vcoclk_2x}	VCO output frequency		220	—	480	MHz	
f_{vcoclk}	PLL output frequency		110	—	240	MHz	
f_{vcoclk_90}	PLL quadrature output frequency		110	—	240	MHz	
I_{pll}	PLL operating current • VCO @ 176 MHz ($f_{osc\_hi\_1}$ = 32 MHz, f_{pll_ref} = 8 MHz, VDIV multiplier = 22)		—	2.8	—	mA	7
I_{pll}	PLL operating current • VCO @ 360 MHz ($f_{osc\_hi\_1}$ = 32 MHz, f_{pll_ref} = 8 MHz, VDIV multiplier = 45)		—	4.7	—	mA	7
J_{cyc_pll}	PLL period jitter (RMS) • f_{vco} = 48 MHz • f_{vco} = 120 MHz		— —	120 75	— —	ps ps	8
J_{acc_pll}	PLL accumulated jitter over 1µs (RMS)						8

Table continues on the next page...

Table 18. MCG specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• f_{vco} = 48 MHz • f_{vco} = 120 MHz	— —	1350 600	— —	ps ps	
D_{unl}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%	
t_{pll_lock}	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll\_ref})$	s	9

1. This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
2. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=0.
3. The resulting system clock frequencies should not exceed their maximum specified values. The DCO frequency deviation (Δf_{dco_t}) over voltage and temperature should be considered.
4. These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32=1.
5. The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Excludes any oscillator currents that are also consuming power while PLL is in operation.
8. This specification was obtained using a NXP developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
9. This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3.3.2 Oscillator electrical specifications

3.3.2.1 Oscillator DC electrical specifications

Table 19. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0) • 32 kHz • 4 MHz • 8 MHz • 16 MHz • 24 MHz • 32 MHz	 — — — — — —	 500 200 300 950 1.2 1.5	 — — — — — —	 nA μA μA μA mA mA	1
I_{DDOSC}	Supply current — high gain mode (HGO=1) • 4 MHz	 —	 400	 —	 μA	1

Table continues on the next page...

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

3.6.1 12-bit cyclic Analog-to-Digital Converter (ADC) parameters

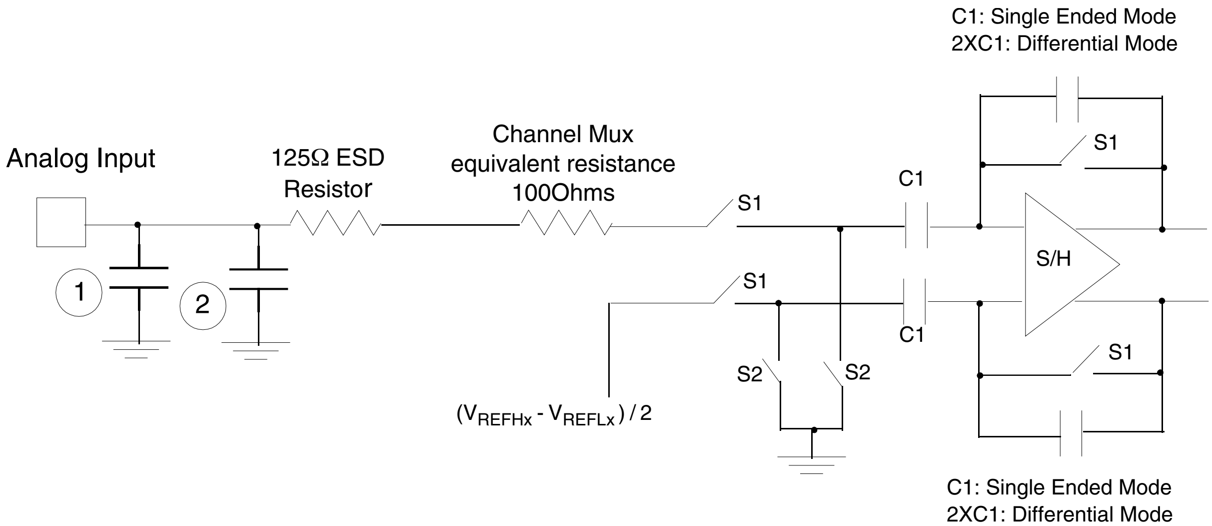
NOTE

The maximum values represent characterized results equivalent to the mean plus three times the standard deviation (mean+3σ).

Table 25. 12-bit ADC electrical specifications

Characteristic	Symbol	Min	Typ	Max	Unit
Recommended Operating Conditions					
Supply Voltage[1]	V_{DDA}	2.7	3.3	3.6	V
V_{refh} Supply Voltage,[2]	Vrefhx	2.7		V_{DDA}	V
ADC Conversion Clock[3]	f_{ADCCLK}	0.6		25	MHz
Conversion Range	R_{AD}	V_{REFL}		V_{REFH}	V
Input Voltage Range External Reference Internal Reference	V_{ADIN}	 V_{REFL} V_{SSA}		 V_{REFH} V_{DDA}	V
Timing and Power					
Conversion Time	t_{ADC}		6		ADC Clock Cycles
ADC Power-Up Time (from adc_pdn)	t_{ADPU}		13		ADC Clock Cycles
ADC RUN Current (per ADC block) • at 600 kHz ADC Clock, LP mode • ≤ 8.33 MHz ADC Clock, 00 mode • ≤ 12.5 MHz ADC Clock, 01 mode • ≤ 16.67 MHz ADC Clock, 10 mode • ≤ 20 MHz ADC Clock, 11 mode • ≤ 25 MHz ADC Clock	I_{ADRUN}		 1 5.7 10.5 17.7 22.6 27.5		mA
ADC Powerdown Current (adc_pdn enabled)	$I_{ADPWRDWN}$		0.02		μA
V_{REFH} Current	I_{VREFH}		0.001		μA
Accuracy (DC or Absolute)					
Integral non-Linearity[4]	INL		+/- 3	+/- 5	LSB[5]
Differential non-Linearity[4]	DNL		+/- 0.6	+/- 0.9	LSB[5]

Table continues on the next page...



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling = 1.8pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing = 2.04pF
3. Sampling capacitor at the sample and hold circuit. Capacitor C1 (4.8pF) is normally disconnected from the input, and is only connected to the input at sampling time.
4. S1 and S2 switch phases are non-overlapping and operate at the ADC clock frequency

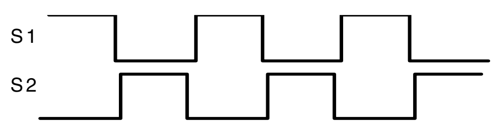


Figure 13. Equivalent circuit for A/D loading

3.6.2 CMP and 6-bit DAC electrical specifications

Table 26. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, high-speed mode (EN = 1, PMODE = 1)	—	—	200	μA
I_{DDLS}	Supply current, low-speed mode (EN = 1, PMODE = 0)	—	—	20	μA
V_{AIN}	Analog input voltage	V_{SS}	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				

Table continues on the next page...

Table 26. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	$V_{DD} – 0.5$	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN = 1, PMODE = 1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN = 1, PMODE = 0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	μs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	μA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.7 to V_{DD} – 0.7 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}$/64

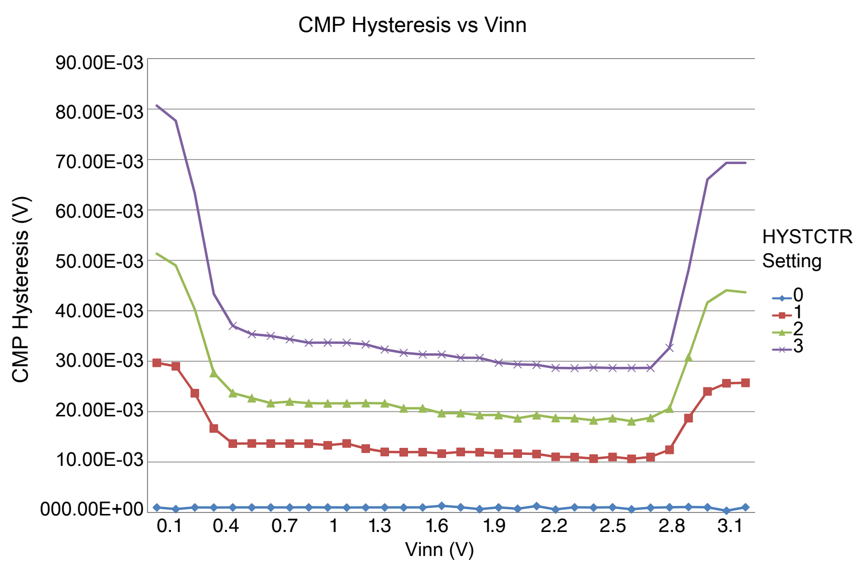


Figure 14. Typical hysteresis vs. Vin level (V_{DD} = 3.3 V, PMODE = 0)

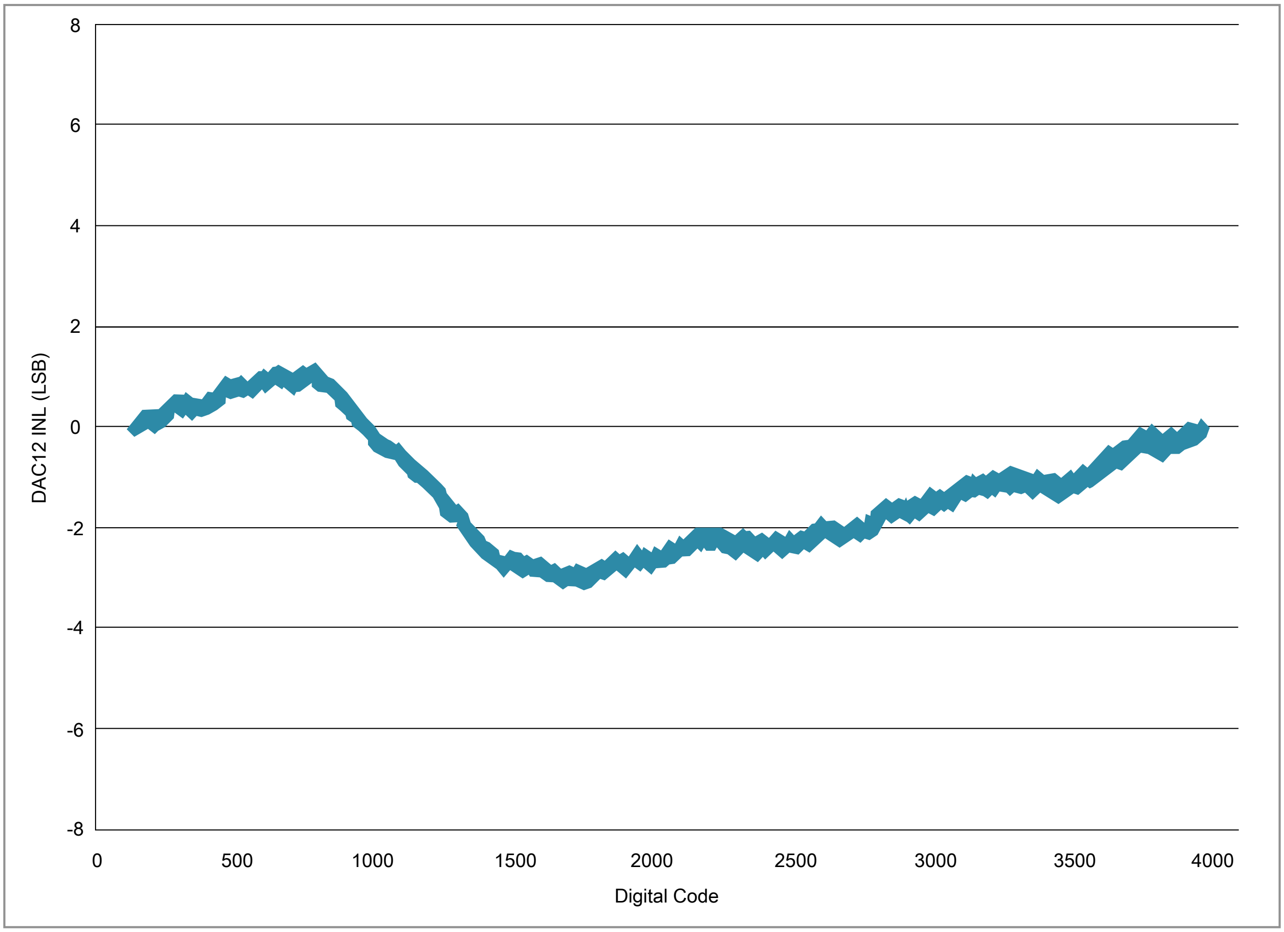


Figure 16. Typical INL error vs. digital code

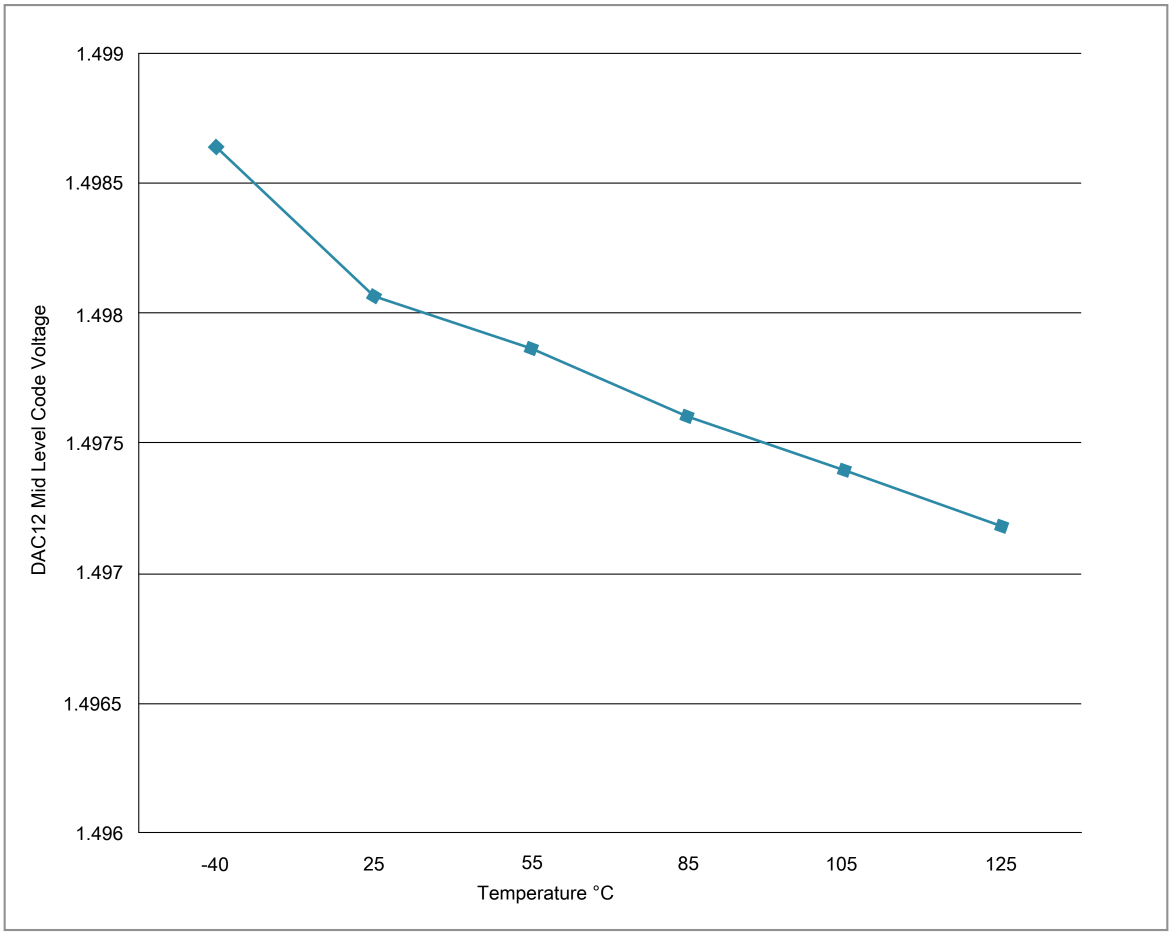


Figure 17. Offset at half scale vs. temperature

3.7 Timers

See General switching specifications.

3.8 Enhanced NanoEdge PWM characteristics

Table 29. NanoEdge PWM timing parameters - 100 Mhz operating frequency

Characteristic	Symbol	Min.	Typ.	Max.	Unit
PWM clock frequency			100		MHz
NanoEdge Placement (NEP) Step Size[1], [2]	pwmp		312		ps

Table continues on the next page...

Table 29. NanoEdge PWM timing parameters - 100 Mhz operating frequency (continued)

Characteristic	Symbol	Min.	Typ.	Max.	Unit
Delay for fault input activating to PWM output deactivated		1			ns
Power-up Time[3]	t_{pu}		25		µs

1. Reference 100 MHz in NanoEdge Placement mode.
2. Temperature and voltage variations do not affect NanoEdge Placement step size.
3. Powerdown to NanoEdge mode transition.

Table 30. NanoEdge PWM timing parameters - 84 Mhz operating frequency

Characteristic	Symbol	Min.	Typ.	Max.	Unit
PWM clock frequency			84		MHz
NanoEdge Placement (NEP) Step Size[1], [2]	pwmp		372		ps
Delay for fault input activating to PWM output deactivated		1			ns
Power-up Time[3]	t_{pu}		30		µs

1. Reference 84 MHz in NanoEdge Placement mode.
2. Temperature and voltage variations do not affect NanoEdge Placement step size.
3. Powerdown to NanoEdge mode transition.

3.9 Communication interfaces

3.9.1 SPI (DSPI) switching specifications (limited voltage range)

The DMA Serial Peripheral Interface (DSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The tables below provide DSPI timing characteristics for classic SPI timing modes. Refer to the DSPI chapter of the Reference Manual for information on the modified transfer formats used for communicating with slower peripheral devices.

NOTE

Fast pads:

- SIN: PTE19
- SOUT: PTE18
- SCK: PTE17
- PCS: PTE16

Open drain pads:

Table 42. Slave mode DSPI timing for open drain pads (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	9.375	MHz
DS9	DSPI_SCK input cycle time	8 x t_{BUS}	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2)$ - 4	$(t_{SCK/2})$ + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	43.5	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2.5	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	38	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	38	ns

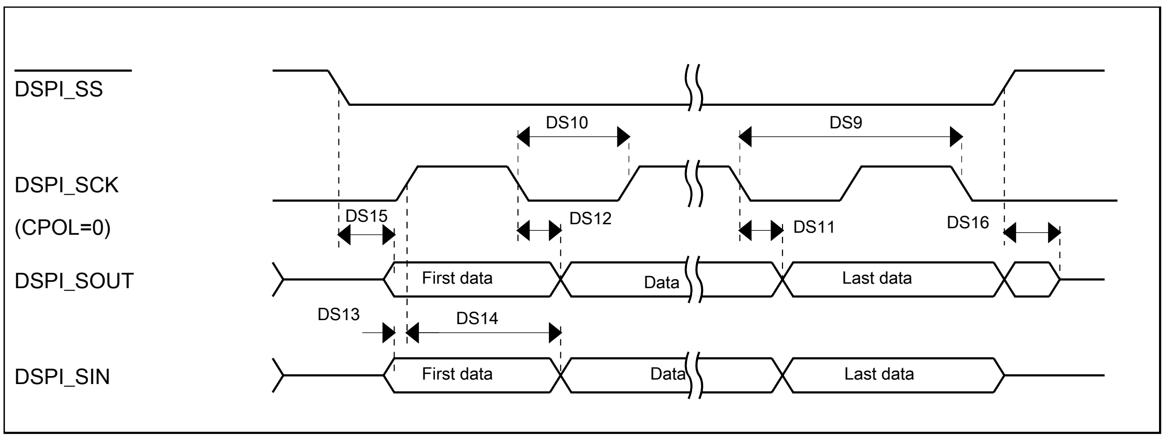


Figure 21. DSPI classic SPI timing — slave mode

3.9.3 I²C

See General switching specifications.

3.9.4 UART

See General switching specifications.

3.10 Kinetis Motor Suite (KMS)

100 LQFP	64 LQFP	48 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	1	—	PTE0/ CLKOUT32K	ADCB_CH6f	ADCB_CH6f	PTE0/ CLKOUT32K		UART1_TX	XBAR0_ OUT10	XBAR0_IN11		
2	2	—	PTE1/ LLWU_P0	ADCB_CH7f	ADCB_CH7f	PTE1/ LLWU_P0		UART1_RX	XBAR0_ OUT11	XBAR0_IN7		
3	—	—	PTE2/ LLWU_P1	ADCB_CH6g	ADCB_CH6g	PTE2/ LLWU_P1		UART1_ CTS_b				
4	—	—	PTE3	ADCB_CH7g	ADCB_CH7g	PTE3		UART1_ RTS_b				
5	—	—	PTE4/ LLWU_P2	DISABLED		PTE4/ LLWU_P2						
6	—	—	PTE5	DISABLED		PTE5					FTM3_CH0	
7	—	—	PTE6/ LLWU_P16	DISABLED		PTE6/ LLWU_P16					FTM3_CH1	
8	3	1	VDD	VDD	VDD							
9	4	2	VSS	VSS	VSS							
10	5	3	PTE16	ADCA_CH0	ADCA_CH0	PTE16	SPI0_PCS0	UART1_TX	FTM_CLKIN0		FTM0_FLT3	
11	6	4	PTE17/ LLWU_P19	ADCA_CH1	ADCA_CH1	PTE17/ LLWU_P19	SPI0_SCK	UART1_RX	FTM_CLKIN1		LPTMR0_ ALT3	
12	7	5	PTE18/ LLWU_P20	ADCB_CH0	ADCB_CH0	PTE18/ LLWU_P20	SPI0_SOUT	UART1_ CTS_b	I2C0_SDA			
13	8	6	PTE19	ADCB_CH1	ADCB_CH1	PTE19	SPI0_SIN	UART1_ RTS_b	I2C0_SCL		CMP3_OUT	
14	—	—	ADCA_CH6a	ADCA_CH6a	ADCA_CH6a							
15	—	—	ADCA_CH7a	ADCA_CH7a	ADCA_CH7a							
16	—	7	PTE20	ADCA_CH6b	ADCA_CH6b	PTE20		FTM1_CH0	UART0_TX			
17	—	8	PTE21	ADCA_CH7b	ADCA_CH7b	PTE21		FTM1_CH1	UART0_RX			
18	9	—	ADCA_CH2	ADCA_CH2	ADCA_CH2							
19	10	—	ADCA_CH3	ADCA_CH3	ADCA_CH3							
20	11	—	ADCA_CH6c	ADCA_CH6c	ADCA_CH6c							
21	12	—	ADCA_CH7c	ADCA_CH7c	ADCA_CH7c							
22	13	9	VDDA	VDDA	VDDA							
23	14	10	VREFH	VREFH	VREFH							
24	15	11	VREFL	VREFL	VREFL							
25	16	12	VSSA	VSSA	VSSA							
26	17	13	PTE29	ADCA_CH4/ CMP1_IN5/ CMP0_IN5	ADCA_CH4/ CMP1_IN5/ CMP0_IN5	PTE29		FTM0_CH2		FTM_CLKIN0		
27	18	14	PTE30	DAC0_OUT/ CMP1_IN3/ ADCA_CH5	DAC0_OUT/ CMP1_IN3/ ADCA_CH5	PTE30		FTM0_CH3		FTM_CLKIN1		
28	19	—	ADCA_CH6d/ CMP0_IN4/ CMP2_IN3	ADCA_CH6d/ CMP0_IN4/ CMP2_IN3	ADCA_CH6d/ CMP0_IN4/ CMP2_IN3							
29	—	—	VSS	VSS	VSS							

100 LQFP	64 LQFP	48 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
55	37	29	PTB2	ADCA_CH6e/ CMP2_IN2	ADCA_CH6e/ CMP2_IN2	PTB2	I2C0_SCL	UART0_RTS_b	FTM0_FLT1		FTM0_FLT3	
56	38	30	PTB3	ADCB_CH7e/ CMP3_IN5	ADCB_CH7e/ CMP3_IN5	PTB3	I2C0_SDA	UART0_CTS_b/ UART0_COL_b			FTM0_FLT0	
57	—	—	PTB9	DISABLED		PTB9						
58	—	—	PTB10	ADCB_CH6a	ADCB_CH6a	PTB10					FTM0_FLT1	
59	—	—	PTB11	ADCB_CH7a	ADCB_CH7a	PTB11					FTM0_FLT2	
60	—	—	VSS	VSS	VSS							
61	—	—	VDD	VDD	VDD							
62	39	31	PTB16	DISABLED		PTB16		UART0_RX	FTM_CLKIN2	CAN0_TX	EWM_IN	XBAR0_IN5
63	40	32	PTB17	DISABLED		PTB17		UART0_TX	FTM_CLKIN1	CAN0_RX	EWM_OUT_b	
64	41	—	PTB18	DISABLED		PTB18	CAN0_TX		FTM3_CH2			
65	42	—	PTB19	DISABLED		PTB19	CAN0_RX		FTM3_CH3			
66	—	—	PTB20	DISABLED		PTB20				FLEXPWMA_X0	CMP0_OUT	
67	—	—	PTB21	DISABLED		PTB21				FLEXPWMA_X1	CMP1_OUT	
68	—	—	PTB22	DISABLED		PTB22				FLEXPWMA_X2	CMP2_OUT	
69	—	—	PTB23	DISABLED		PTB23		SPI0_PCS5		FLEXPWMA_X3	CMP3_OUT	
70	43	33	PTC0	ADCB_CH6b	ADCB_CH6b	PTC0	SPI0_PCS4	PDB0_EXTRG			FTM0_FLT1	SPI0_PCS0
71	44	34	PTC1/ LLWU_P6	ADCB_CH7b	ADCB_CH7b	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_b	FTM0_CH0	FLEXPWMA_A3	XBAR0_IN11	
72	45	35	PTC2	ADCB_CH6c/ CMP1_IN0	ADCB_CH6c/ CMP1_IN0	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1	FLEXPWMA_B3	XBAR0_IN6	
73	46	36	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	FTM3_FLT0	
74	47	—	VSS	VSS	VSS							
75	48	—	VDD	VDD	VDD							
76	49	37	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT	
77	50	38	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ALT2	XBAR0_IN2		CMP0_OUT	FTM0_CH2
78	51	39	PTC6/ LLWU_P10	CMP2_IN4/ CMP0_IN0	CMP2_IN4/ CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_EXTRG	XBAR0_IN3	UART0_RX	XBAR0_OUT6	I2C0_SCL
79	52	40	PTC7	CMP3_IN4/ CMP0_IN1	CMP3_IN4/ CMP0_IN1	PTC7	SPI0_SIN		XBAR0_IN4	UART0_TX	XBAR0_OUT7	I2C0_SDA
80	53	—	PTC8	ADCB_CH7c/ CMP0_IN2	ADCB_CH7c/ CMP0_IN2	PTC8		FTM3_CH4				
81	54	—	PTC9	ADCB_CH6d/ CMP0_IN3	ADCB_CH6d/ CMP0_IN3	PTC9		FTM3_CH5				

100 LQFP	64 LQFP	48 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
82	55	—	PTC10	ADCB_CH7d	ADCB_CH7d	PTC10		FTM3_CH6				
83	56	—	PTC11/ LLWU_P11	ADCB_CH6e	ADCB_CH6e	PTC11/ LLWU_P11		FTM3_CH7				
84	—	—	PTC12	DISABLED		PTC12			FTM_CLKIN0		FTM3_FLT0	
85	—	—	PTC13	DISABLED		PTC13			FTM_CLKIN1			
86	—	—	PTC14	DISABLED		PTC14		I2C0_SCL				
87	—	—	PTC15	DISABLED		PTC15		I2C0_SDA				
88	—	—	VSS	VSS	VSS							
89	—	—	VDD	VDD	VDD							
90	—	—	PTC16	DISABLED		PTC16	CAN1_RX					
91	—	—	PTC17	DISABLED		PTC17	CAN1_TX					
92	—	—	PTC18	DISABLED		PTC18						
93	57	41	PTD0/ LLWU_P12	DISABLED		PTD0/ LLWU_P12	SPI0_PCS0		FTM3_CH0	FTM0_CH0	FLEXPWMA_ A0	
94	58	42	PTD1	ADCA_CH7f	ADCA_CH7f	PTD1	SPI0_SCK		FTM3_CH1	FTM0_CH1	FLEXPWMA_ B0	
95	59	43	PTD2/ LLWU_P13	DISABLED		PTD2/ LLWU_P13	SPI0_SOUT		FTM3_CH2	FTM0_CH2	FLEXPWMA_ A1	I2C0_SCL
96	60	44	PTD3	DISABLED		PTD3	SPI0_SIN		FTM3_CH3	FTM0_CH3	FLEXPWMA_ B1	I2C0_SDA
97	61	45	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI0_PCS1	UART0_ RTS_b	FTM0_CH4	FLEXPWMA_ A2	EWM_IN	SPI0_PCS0
98	62	46	PTD5	ADCA_CH6g	ADCA_CH6g	PTD5	SPI0_PCS2	UART0_ CTS_b/ UART0_ COL_b	FTM0_CH5	FLEXPWMA_ B2	EWM_OUT_b	SPI0_SCK
99	63	47	PTD6/ LLWU_P15	ADCA_CH7g	ADCA_CH7g	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6	FTM1_CH0	FTM0_FLT0	SPI0_SOUT
100	64	48	PTD7	DISABLED		PTD7		UART0_TX	FTM0_CH7	FTM1_CH1	FTM0_FLT1	SPI0_SIN

5.2 Pinout diagrams

The following diagrams show pinouts for the packages. For each pin, the diagrams show the default function. However, many signals may be multiplexed onto a single pin.

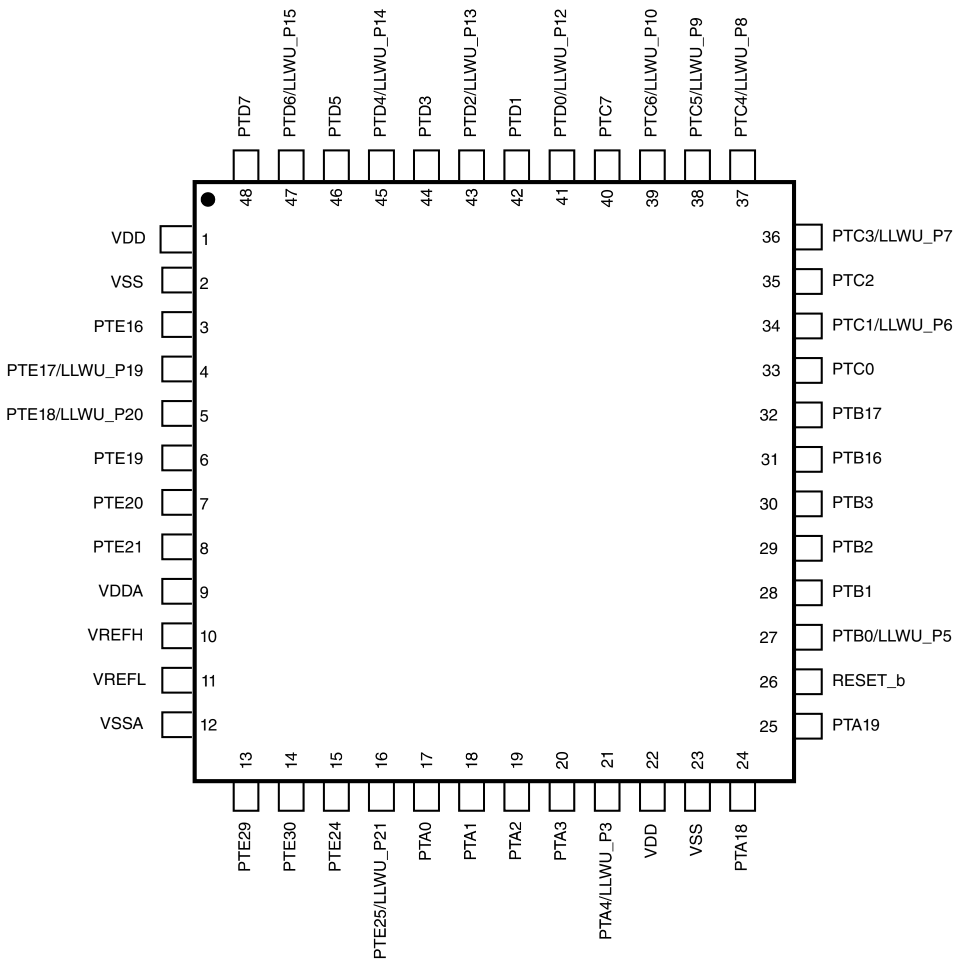


Figure 24. 48-pin LQFP

6 Ordering parts

8.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

8.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

8.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

8.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

8.4.1 Example

This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

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Document Number KV4XP100M168
Revision 3, 06/2016