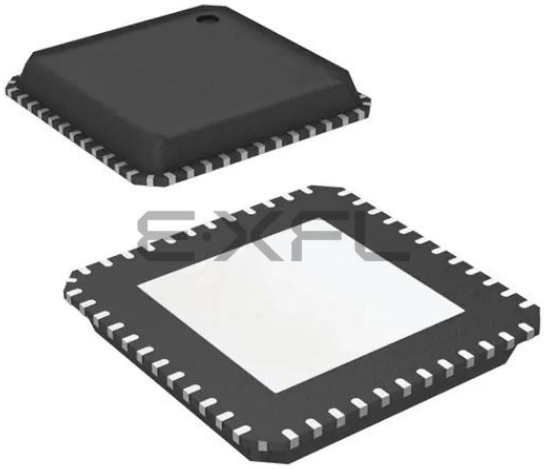

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Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Automotive
Core Processor	ARM® Cortex®-M3
Program Memory Type	FLASH (128kB)
Controller Series	-
RAM Size	6K x 8
Interface	LIN, SSI, UART
Number of I/O	10
Voltage - Supply	5.5V ~ 28V
Operating Temperature	-40°C ~ 175°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-48-29
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/tle9879qxw40xuma1

2 Block Diagram

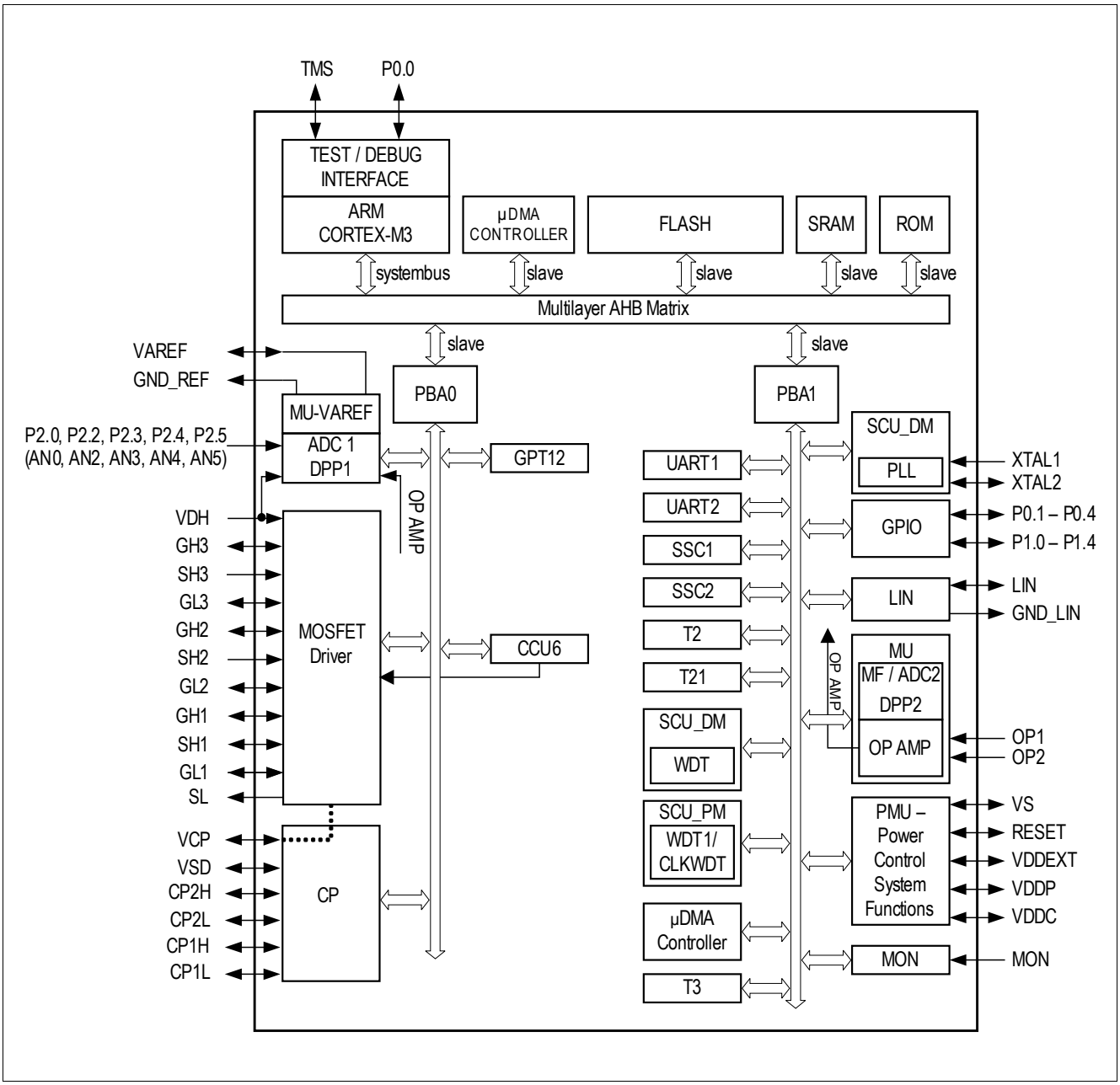

Figure 1 Block Diagram TLE9879QXW40

5.2.1 Block Diagram

The following figure shows the structure of the Power Management Unit. **Table 4** describes the submodules in more detail.

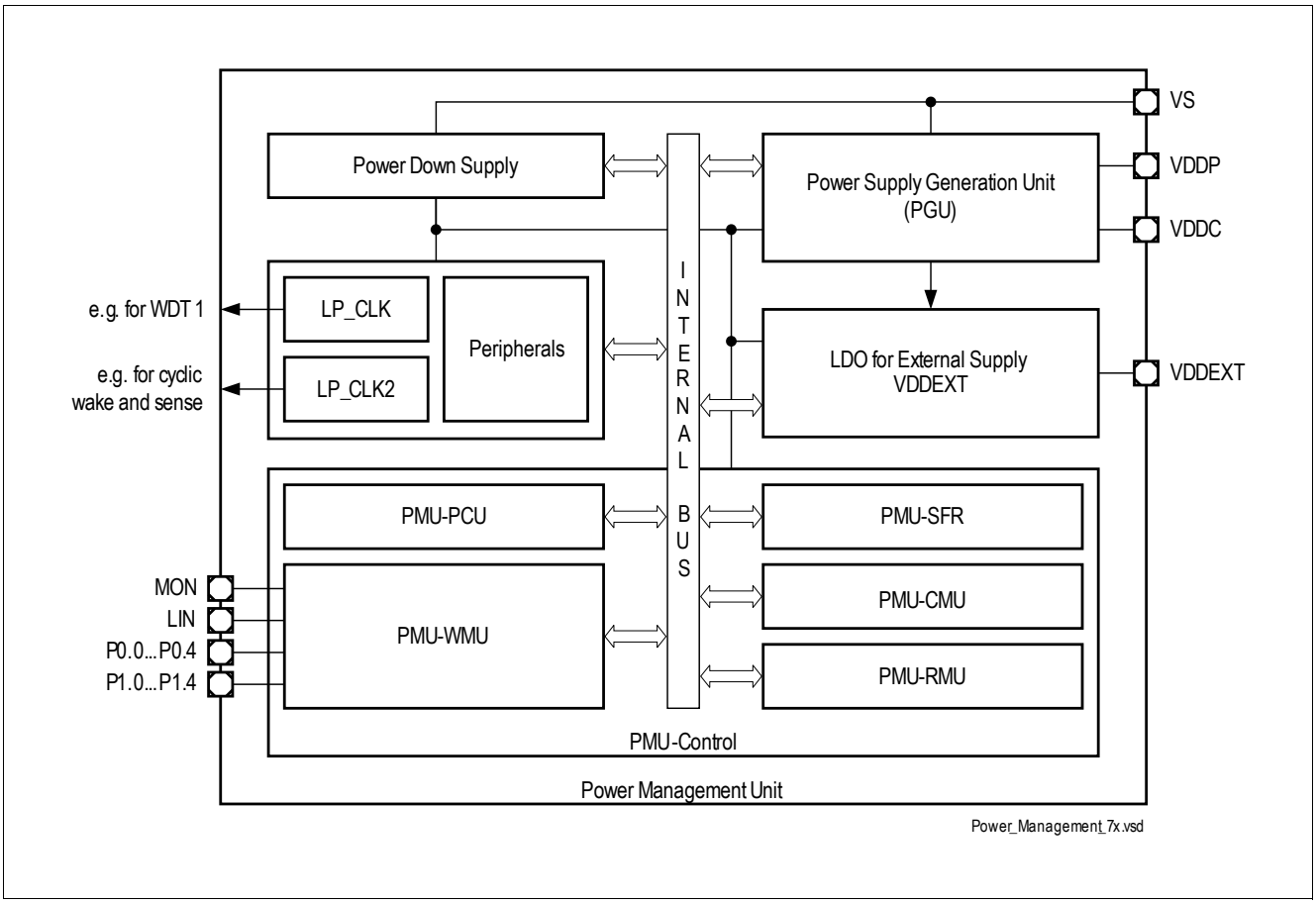

Figure 3 Power Management Unit Block Diagram

Table 4 Description of PMU Submodules

Mod. Name	Modules	Functions
Power Down Supply	Independent supply voltage generation for PMU	This supply is dedicated to the PMU to ensure an independent operation from generated power supplies (VDDP, VDDC).
LP_CLK (= 18 MHz)	- Clock source for all PMU submodules - Backup clock source for System - Clock source for WDT1	This ultra low power oscillator generates the clock for the PMU. This clock is also used as backup clock for the system in case of PLL Clock failure and as an independent clock source for WDT1.
LP_CLK2 (= 100 kHz)	Clock source for PMU	This ultra low power oscillator generates the clock for the PMU in Stop Mode and in the cyclic modes.
Peripherals	Peripheral blocks of PMU	These blocks include the analog peripherals to ensure a stable and fail-safe PMU startup and operation (bandgap, bias).

WDT1 (System Watchdog)

- LP_CLK clock source for all PMU submodules and WDT1

ICU (Interrupt Control Unit)

- PREWARN_SUP_NMI supply prewarning NMI request
- PREWARN_SUP_INT supply prewarning interrupt
- grouping of peripheral interrupts for external interupt nodes:
  - grouping single peripheral interrupts for interrupt node INT<2> (Measurement Unit (MU))
  - grouping single peripheral interrupts for interrupt node INT<3> (ADC1-VAREF)
  - grouping single peripheral interrupts for interrupt node INT<10> (UART1-LIN Transceiver)
  - grouping single peripheral interrupts for interrupt node INT<14> (Bridge Driver)

11 Memory Control Unit

11.1 Features

- Handles all system memories and their interaction with the CPU
- Memory protection functions for all system memories (D-Flash, P-Flash, RAM)
- Address management with access violation detection including reporting
- Linear address range for all memories (no paging)

11.2 Introduction

11.2.1 Block Diagram

The Memory Control Unit (MCU) is divided in the following sub-modules:

- NVM memory module (embedded Flash Memory)
- RAM memory module
- BootROM memory module
- Memory Protection Unit (MPU) module
- Peripheral Bridge PBA0

13.2 Introduction

The behavior of the Watchdog Timer in Active Mode is illustrated in **Figure 16**.

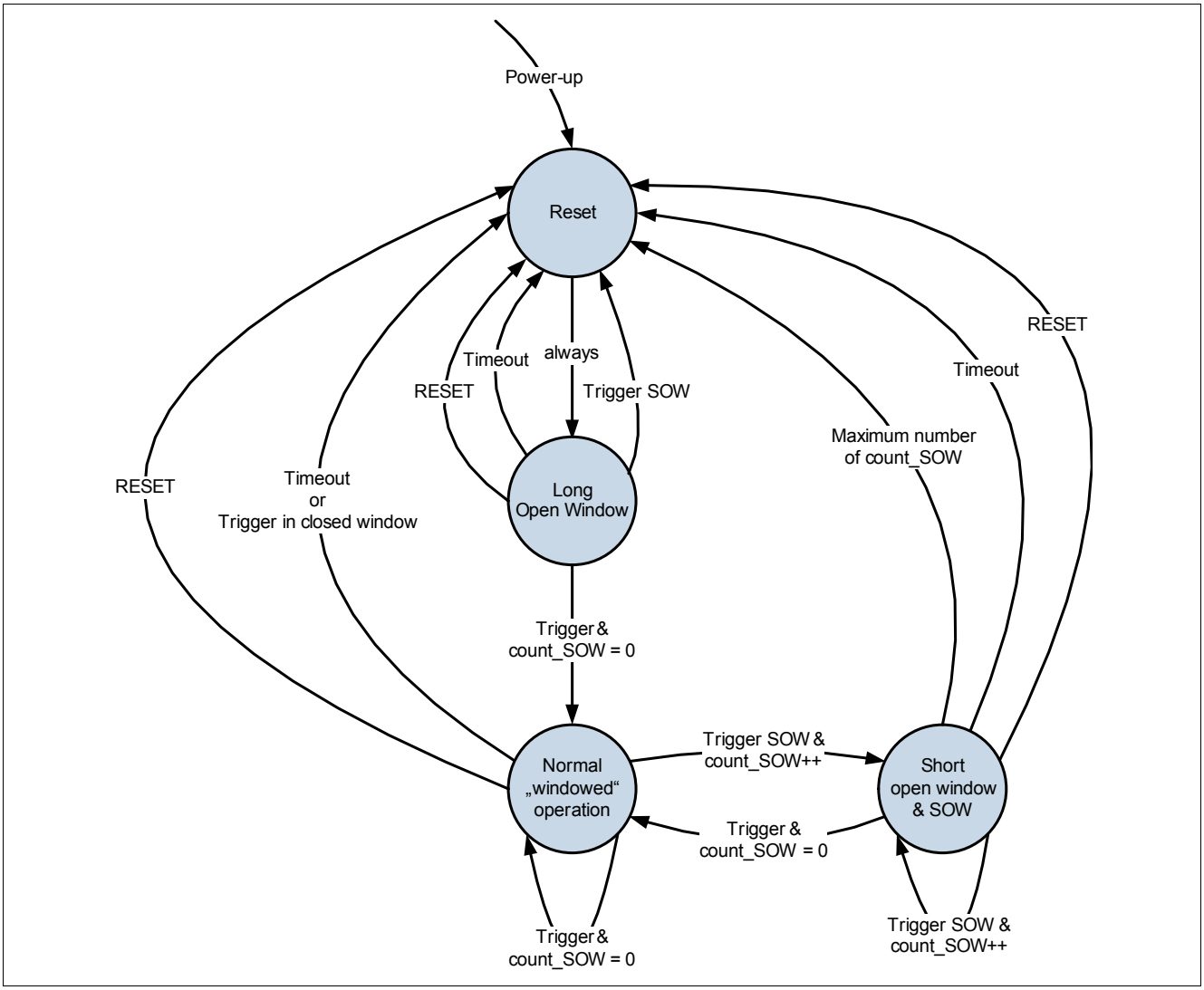

Figure 16 Watchdog Timer Behavior

Table 8 Port 0 Input/Output Functions (cont'd)

Port Pin	Input/Output	Select	Connected Signal(s)	From/to Module
P0.2	Input	GPI	P0_DATA.P2	
		INP1	CCPOS2_1	CCU6
		INP2	T2EUDA	GPT12T2
		INP3	MTSR_1	SSC1
		INP4	T21EX_0	Timer 21
		INP5	T6INA	GPT12T6
	Output	GPO	P0_DATA.P2	–
		ALT1	COUT60_0	CCU6
		ALT2	MTSR_1	SSC1
		ALT3	EXF2_0	Timer 2
P0.3	Input	GPI	P0_DATA.P3	
		INP1	SCK_1	SSC1
		INP2	CAPINB	GPT12
		INP3	T5INA	GPT12T5
		INP4	T4EUDA	GPT12T4
		INP5	CCPOS0_1	CCU6
	Output	GPO	P0_DATA.P3	
		ALT1	SCK_1	SSC1
		ALT2	EXF21_2	Timer 21
		ALT3	T6OUT	GPT12T6
P0.4	Input	GPI	P0_DATA.P4	
		INP1	MRST_1_0	SSC1
		INP2	CC60_0	CCU6
		INP3	T21_2	Timer 21
		INP4	EXINT2_2	SCU
		INP5	T3EUDA	GPT12T3
		INP6	CCPOS1_1	CCU6
	Output	GPO	P0_DATA.P4	
		ALT1	MRST_1_0	SSC1
		ALT2	CC60_0	CCU6
		ALT3	CLKOUT_0	SCU

15 General Purpose Timer Units (GPT12)

15.1 Features

15.1.1 Features Block GPT1

The following list summarizes the supported features:

- f_{GPT}/4 maximum resolution
- 3 independent timers/counters
- Timers/counters can be concatenated
- 4 operating modes:
  - Timer Mode
  - Gated Timer Mode
  - Counter Mode
  - Incremental Interface Mode
- Reload and Capture functionality
- Shared interrupt: Node 0

15.1.2 Features Block GPT2

The following list summarizes the supported features:

- f_{GPT}/2 maximum resolution
- 2 independent timers/counters
- Timers/counters can be concatenated
- 3 operating modes:
  - Timer Mode
  - Gated Timer Mode
  - Counter Mode
- Extended capture/reload functions via 16-bit capture/reload register CAPREL
- Shared interrupt: Node 1

15.2 Introduction

The General Purpose Timer Unit blocks GPT1 and GPT2 have very flexible multifunctional timer structures which may be used for timing, event counting, pulse width measurement, pulse generation, frequency multiplication, and other purposes.

They incorporate five 16-bit timers that are grouped into the two timer blocks GPT1 and GPT2. Each timer in each block may operate independently in a number of different modes such as Gated timer or Counter Mode, or may be concatenated with another timer of the same block.

Each block has alternate input/output functions and specific interrupts associated with it. Input signals can be selected from several sources by register PISEL.

The GPT module is clocked with clock f_{GPT}. f_{GPT} is a clock derived from f_{SYS}.

15.2.2 Block Diagram GPT2

Block GPT2 contains two timers/counters: The core timer T6 and the auxiliary timer T5. The maximum resolution is $f_{GPT}/2$. An additional Capture/Reload register (CAPREL) supports capture and reload operation with extended functionality.

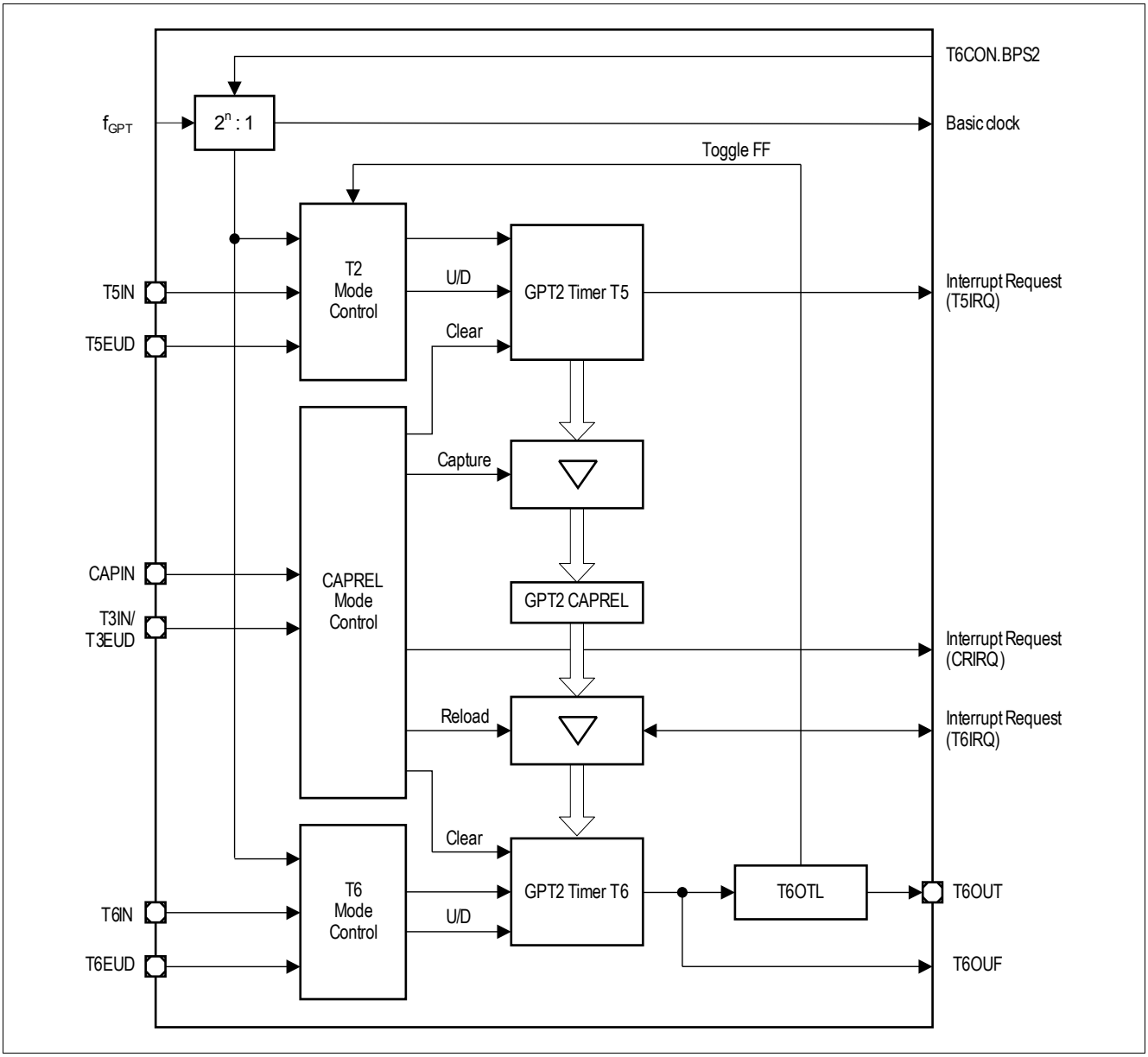

Figure 20 GPT2 Block Diagram (n = 1 … 4)

20.2 Introduction

The LIN Module is a transceiver for the Local Interconnect Network (LIN) compliant to the LIN2.2 standard, backward compatible to LIN1.3, LIN2.0 and LIN2.1. It operates as a bus driver between the protocol controller and the physical network. The LIN bus is a single wire, bi-directional bus typically used for in-vehicle networks, using baud rates between 2.4 kBaud and 20 kBaud. Additionally baud rates up to 115.2 kBaud are implemented.

The LIN Module offers several different operation modes, including a LIN Sleep Mode and the LIN Normal Mode. The integrated slope control allows to use several data transmission rates with optimized EMC performance. For data transfer at the end of line, a Flash Mode up to 115.2 kBaud is implemented. This Flash Mode can be used for data transfer under special conditions for up to 250 kbit/s (in production environment, point-to-point communication with reduced wire length and limited supply voltage).

20.2.1 Block Diagram

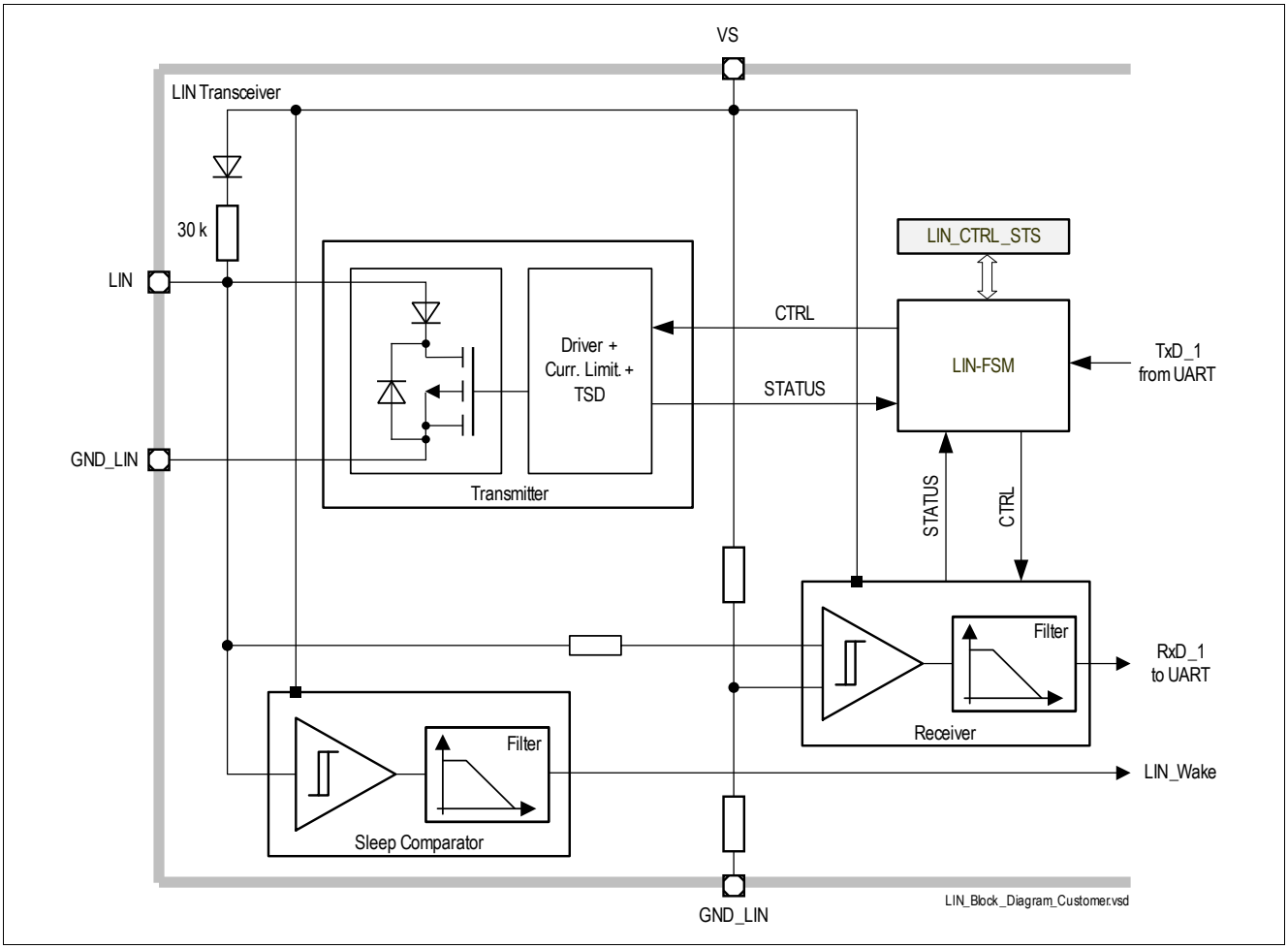

Figure 23 LIN Transceiver Block Diagram

21.2 Introduction

The High-Speed Synchronous Serial Interface (SSC) supports both full-duplex and half-duplex serial synchronous communication. The serial clock signal can be generated by the SSC internally (master mode), using its own 16-bit baud rate generator, or can be received from an external master (slave mode). Data width, shift direction, clock polarity, and phase are programmable. This allows communication with SPI-compatible devices or devices using other synchronous serial interfaces.

Data is transmitted or received on TXD and RXD lines, which are normally connected to the MTSR (MasterTransmit/Slave Receive) and MRST (Master Receive/Slave Transmit) pins. The clock signal is output via line MS_CLK (Master Serial Shift Clock) or input via line SS_CLK (Slave Serial Shift Clock). Both lines are normally connected to the pin SCLK. Transmission and reception of data are double-buffered.

21.2.1 Block Diagram

Figure 24 shows all functional relevant interfaces associated with the SSC Kernel.

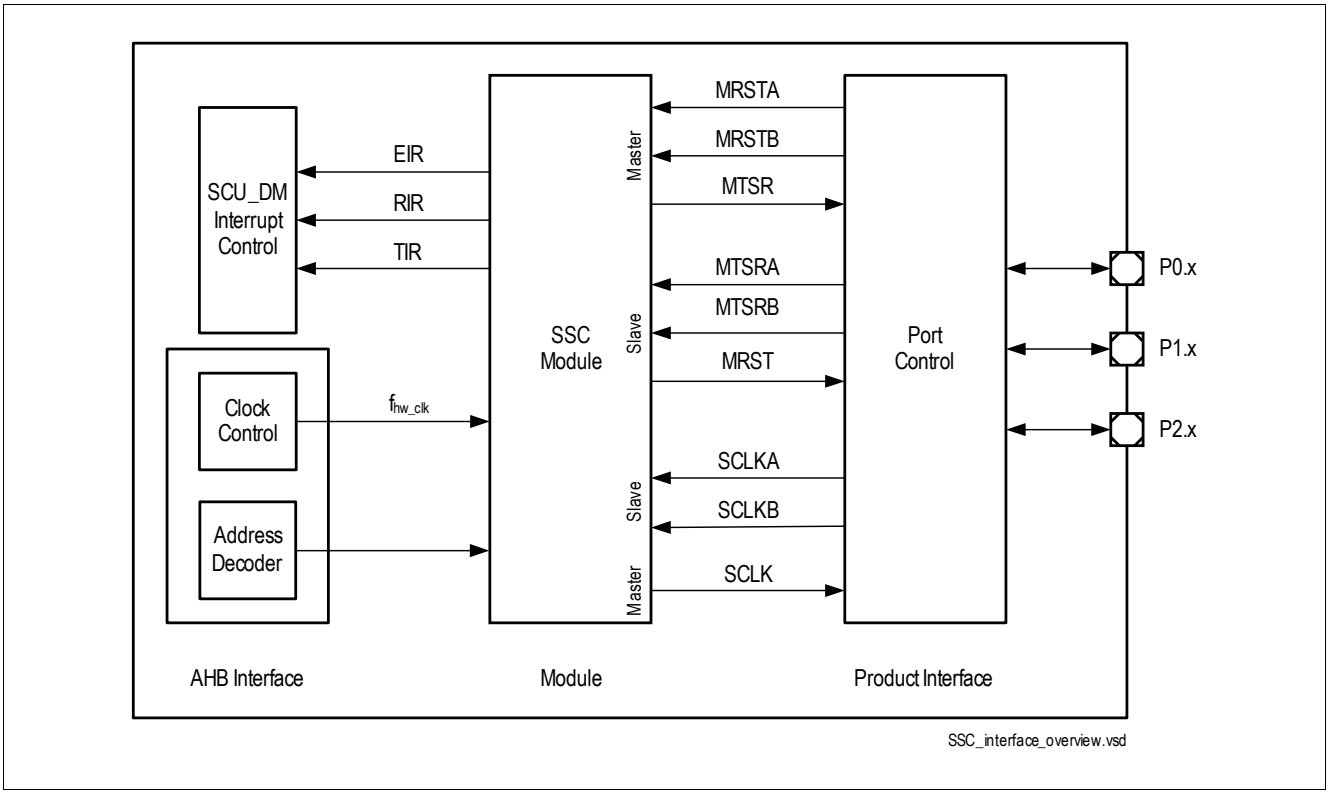

Figure 24 SSC Interface Diagram

22.2.1.1 Block Diagram BEMF Comparator

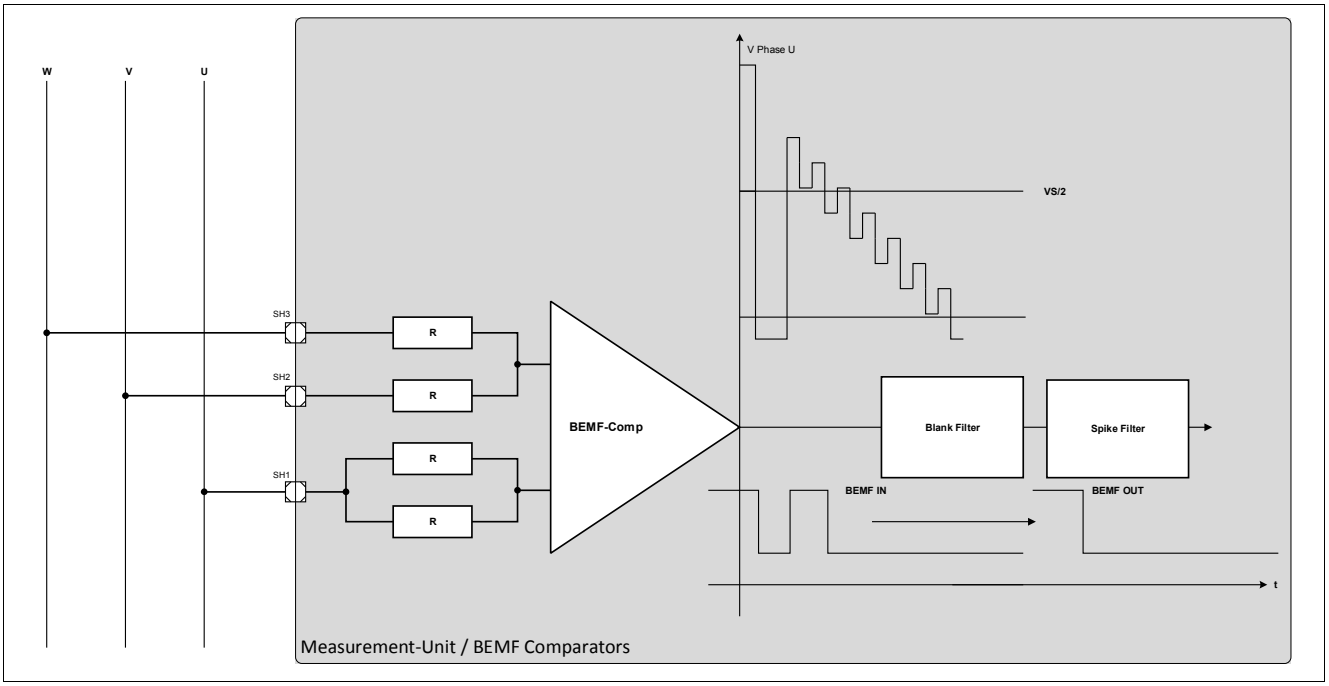

Figure 26 3 Times BEMF Comparator

29.2 Power Management Unit (PMU)

This chapter includes all electrical characteristics of the Power Management Unit

29.2.1 PMU I/O Supply (VDDP) Parameters

This chapter describes all electrical parameters which are observable on SoC level. For this purpose only the pad-supply VDDP and the transition times between the system modes are specified here.

Table 22 Electrical Characteristics

V_S = 5.5 V to 28 V, T_j = -40 °C to +175 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Specified output current	I_{VDDP}	0	–	50	mA	1)	P_2.1.1
Specified output current	I_{VDDP}	0	–	30	mA	1)2)	P_2.1.22
Required decoupling capacitance	C_{VDDP1}	0.47	–	2.2	µF	3)4) ESR < 1Ω; the specified capacitor value is a typical value.	P_2.1.2
Required buffer capacitance for stability (load jumps)	C_{VDDP2}	1	–	2.2	µF	3)4) The specified capacitor value is a typical value.	P_2.1.20
Output voltage including line and load regulation @ Active Mode	V_{DDPOUT}	4.9	5.0	5.1	V	5) I_{load} < 90mA; V_S > 5.5V	P_2.1.3
Output voltage including line and load regulation @ Active Mode	V_{DDPOUT}	4.9	5.0	5.1	V	2)5) I_{load} < 70mA; V_S > 5.5V	P_2.1.23
Output voltage including line and load regulation @ Stop Mode	$V_{DDPOUTSTOP}$	4.5	5.0	5.5	V	5) I_{load} is only internal; V_S > 5.5V; -40°C ≤ T_j ≤ -150°C.	P_2.1.21
Output voltage including line and load regulation @ Stop Mode - Extended temperature range	$V_{DDPOUTSTOP\_HT}$	3.5	5.0	5.8	V	5) I_{load} is only internal; V_S > 5.5V; 150°C < T_j ≤ 175°C.	P_2.1.29
Output drop @ Active Mode	$V_{SVDDPout}$	–	50	400	mV	I_{VDDP} = 30mA6); 3.5V < V_S < 5.0V	P_2.1.4
Load regulation @ Active Mode	$V_{VDDPLOR}$	-50	–	50	mV	2 ... 90mA; C = 570nF -40°C < T_j ≤ 150°C	P_2.1.5
Load regulation @ Active Mode-Extended temperature range	$V_{VDDPLOR\_HT}$	-70	–	70	mV	2 ... 90mA; C = 570nF 150°C < T_j ≤ 175°C	P_2.1.30
Line regulation @ Active Mode	$V_{VDDPLIR}$	-50	–	50	mV	V_S = 5.5 ... 28V	P_2.1.6
Overvoltage detection	V_{DDPOV}	5.14	–	5.4	V	V_S > 5.5V; Overvoltage leads to SUPPLY_NMI	P_2.1.7
Overvoltage detection filter time	t_{FILT_VDDPOV}	–	735	–	µs	3)7)	P_2.1.24

29.2.2 PMU Core Supply (VDDC) Parameters

This chapter describes all electrical parameters which are observable on SoC level. For this purpose only the core-supply VDDC and the transition times between the system modes are specified here.

Table 23 Electrical Characteristics

V_S = 5.5 V to 28 V, T_j = -40 °C to +175 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Required decoupling capacitance	C_{VDDC1}	0.1	–	1	µF	1)2) ESR < 1Ω; the specified capacitor value is a typical value.	P_2.2.1
Required buffer capacitance for stability (load jumps)	C_{VDDC2}	0.33	–	1	µF	2)the specified capacitor value is a typical value.	P_2.2.17
Output voltage including line regulation @ Active Mode	V_{DDCOUT}	1.44	1.5	1.56	V	I_{load} < 40mA	P_2.2.2
Reduced output voltage including line regulation @ Stop Mode	$V_{DDCOUT\_Stop\_Red}$	0.95	1.1	1.3	V	with internal VDDC load only: $I_{load\_internal}$ < 1.5mA	P_2.2.23
Load Regulation @ Active Mode	V_{DDCLOR}	-50	–	50	mV	2 ... 40mA; C =430nF	P_2.2.3
Line regulation @ Active Mode	V_{DDCLIR}	-25	–	25	mV	V_{DDP} = 2.5 ... 5.5V	P_2.2.4
Overvoltage detection	V_{DDCOV}	1.59	1.62	1.68	V	Overvoltage leads to SUPPLY_NMI	P_2.2.5
Overvoltage detection filter time	t_{FILT_VDDCOV}	–	735	–	µs	1)3)	P_2.2.18
Voltage OK detection range[4)]	ΔV_{DDCOK}	- 280	–	+ 280	mV	1)	P_2.2.19
Voltage stable detection range[5)]	ΔV_{DDCSTB}	- 110	–	+ 110	mV	1)	P_2.2.20
Undervoltage reset	V_{DDVUV}	1.136	1.20	1.264	V	–	P_2.2.6
Overcurrent diagnostic	I_{VDDCOC}	45	–	100	mA	–	P_2.2.7
Overcurrent diagnostic filter time	t_{FILT_VDDCOC}	–	27	–	µs	1)3)	P_2.2.21
Overcurrent diagnostic shutdown time	$t_{FILT\_VDDCOC\_SD}$	–	290	–	µs	1)3)6)	P_2.2.22

1) Not subject to production test, specified by design.
2) Ceramic capacitor.
3) This filter time and its variation is derived from the time base t_{LP_CLK} = 1 / f_{LP_CLK}.
4) The absolute voltage value is the sum of parameters V_{DDC} + ΔV_{DDCSTB}.
5) The absolute voltage value is the sum of parameters V_{DDC} + ΔV_{DDCOK}.
6) After $t_{FILT\_VDDCOC\_SD}$ is passed and the overcurrent condition is still present the device will enter sleep mode.

29.3 System Clocks

29.3.1 Oscillators and PLL Parameters

Table 27 Electrical Characteristics System Clocks

V_S = 5.5 V to 28 V, T_j = -40 °C to +175 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
PMU Oscillators (Power Management Unit)							
Frequency of LP_CLK	f_{LP_CLK}	14	18	22	MHz	This clock is used at startup and can be used in case the PLL fails	P_3.1.1
Frequency of LP_CLK2	f_{LP_CLK2}	70	100	130	kHz	This clock is used for cyclic wake	P_3.1.2
CGU Oscillator (Clock Generation Unit Microcontroller)							
Short term frequency deviation[1)]	f_{TRIMST}	-0.4	–	+0.4	%	[2)3)] Within any 10 ms, e.g. after synchronization to a LIN frame (PLL settings untouched within 10 ms)	P_3.1.3
Absolute accuracy	$f_{TRIMABSA}$	-1.5	–	+1.5	%	Including temperature and lifetime deviation; -40°C ≤ T_j ≤ 150°C	P_3.1.4
Absolute accuracy - Extended temperature range	$f_{TRIMABSA\_HT}$	-2.0	–	+2.0	%	Including temperature and lifetime deviation; 150°C ≤ T_j ≤ 175°C	P_3.1.18
CGU-OSC Start-up time	t_{OSC}	–	–	10	µs	[3)] Startup time OSC from Sleep Mode, power supply stable	P_3.1.5
PLL (Clock Generation Unit Microcontroller) [3)]							
VCO frequency range Mode 0	f_{VCO-0}	48	–	112	MHz	VCOSEL =”0”	P_3.1.6
VCO frequency range Mode 1	f_{VCO-1}	96	–	160	MHz	VCOSEL =”1”	P_3.1.7
Input frequency range	f_{OSC}	4	–	16	MHz	–	P_3.1.8
XTAL1 input freq. range	f_{OSC}	4	–	16	MHz	–	P_3.1.9
Output freq. range	f_{PLL}	0.04687	–	80	MHz	–	P_3.1.10
Free-running frequency Mode 0	$f_{VCOfree\_0}$	–	–	38	MHz	VCOSEL =”0”	P_3.1.11
Free-running frequency Mode 1	$f_{VCOfree\_1}$	–	–	76	MHz	VCOSEL =”1”	P_3.1.12
Input clock high/low time	$t_{high/low}$	10	–	–	ns	–	P_3.1.13

29.5 Parallel Ports (GPIO)

29.5.1 Description of Keep and Force Current

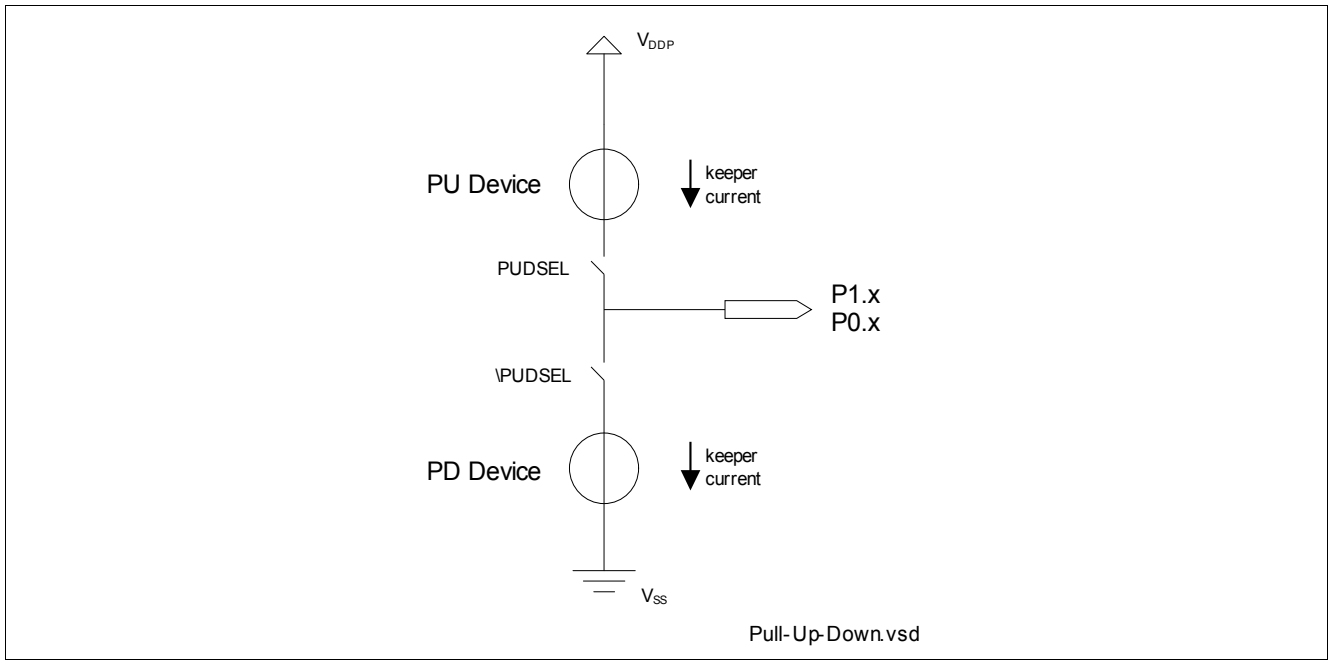

Figure 34 Pull-Up/Down Device

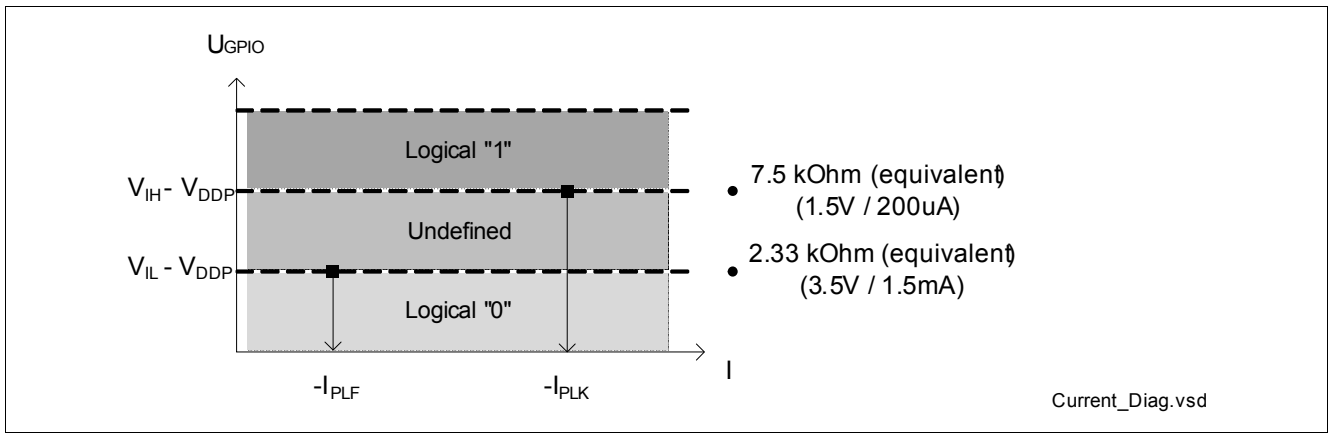

Figure 35 Pull-Up Keep and Forced Current

5) As a rule, with decreasing output current the output levels approach the respective supply level ($V_{OL} \rightarrow GND$, $V_{OH} \rightarrow V_{DDP}$). Tested at 4.9V < V_{DDP} < 5.1V, I_{OL} = 1mA, I_{OH} = -1mA.
6) The given values are worst-case values. In production tests, this leakage current is only tested at 150°C; other values are ensured by correlation. For derating, please refer to the following descriptions:
Leakage derating depending on temperature (T_J = junction temperature [°C]):
$I_{OZ} = 0.05 \times e^{(1.5 + 0.028 \times TJ)}$ [µA]. For example, at a temperature of 95°C the resulting leakage current is 3.2 µA.
Leakage derating depending on voltage level (DV = V_{DDP} - V_{PIN} [V]):
$I_{OZ} = I_{OZtempmax}$ - (1.6 × DV) [µA]
This voltage derating formula is an approximation which applies for maximum temperature.
7) Keep current: Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level: $V_{PIN} \geq V_{IH}$ for a pull-up; $V_{PIN} \leq V_{IL}$ for a pull-down.
Force current: Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device: $V_{PIN} \leq V_{IL}$ for a pull-up; $V_{PIN} \geq V_{IH}$ for a pull-down.
These values apply to the fixed pull-devices in dedicated pins and to the user-selectable pull-devices in general purpose IO pins.

29.5.3 DC Parameters of Port 2

These parameters apply to the IO voltage range, 4.5 V ≤ V_{DDP} ≤ 5.5 V.

Note: Operating Conditions apply.
Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV}.

Table 32 DC Characteristics Port 2

V_S = 5.5 V to 28 V, T_j = -40 °C to +175 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input low voltage	V_{IL}	-0.3	–	0.3 x V_{DDP}	V	1)4.5V ≤ V_{DDP} ≤ 5.5V	P_5.2.1
Input low voltage	V_{IL_extend}	-0.3	0.42 x V_{DDP}	–	V	2)2.6V ≤ V_{DDP} ≤ 4.5V	P_5.2.10
Input high voltage	V_{IH}	0.7 x V_{DDP}	–	V_{DDP} + 0.3	V	1)4.5V ≤ V_{DDP} ≤ 5.5V	P_5.2.2
Input high voltage	V_{IH_extend}	–	0.52 x V_{DDP}	V_{DDP} + 0.3	V	2)2.6V ≤ V_{DDP} ≤ 4.5V	P_5.2.11
Input hysteresis	HYS_{P2}	0.11 x V_{DDP}	–	–	V	2)Series resistance = 0 Ω; 4.5V ≤ V_{DDP} ≤ 5.5V	P_5.2.3
Input hysteresis	HYS_{P2_extend}	–	0.09 x V_{DDP}	–	V	2)Series resistance = 0 Ω; 2.6V ≤ VDDP < 4.5V	P_5.2.12
Input leakage current	I_{OZ2}	-400	–	+400	nA	3)T_J ≤ 85°C, 0 V < V_{IN} < V_{DDP}	P_5.2.4
Input leakage current-Extended temperature range for port pin P2.0	$I_{OZ2\_HT\_P2\_0}$	-2500	–	+2500	nA	3)85°C < Tj ≤ 175°C, 0 V < VIN < VDDP	P_5.2.14

29.6 LIN Transceiver

29.6.1 Electrical Characteristics

Table 33 Electrical Characteristics LIN Transceiver

V_s = 5.5V to 18V, T_j = -40 °C to +175 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Bus Receiver Interface							
Receiver threshold voltage, recessive to dominant edge	V_{th_dom}	0.4 × V_S	0.45 × V_S	0.53 x V_S	V	SAE J2602	P_6.1.1
Receiver dominant state	V_{BUSdom}	-27	–	0.4 × V_S	V	LIN Spec 2.2 (Par. 17)	P_6.1.2
Receiver threshold voltage, dominant to recessive edge	V_{th_rec}	0.47 x V_S	0.55 × V_S	0.6 × V_S	V	SAE J2602	P_6.1.3
Receiver recessive state	V_{BUSrec}	0.6 × V_S	–	1.15 × V_S	V	[1] LIN Spec 2.2 (Par. 18)	P_6.1.4
Receiver center voltage	V_{BUS_CNT}	0.475 × V_S	0.5 × V_S	0.525 × V_S	V	[2] LIN Spec 2.2 (Par. 19)	P_6.1.5
Receiver hysteresis	V_{HYS}	0.07 V_S	0.12 × V_S	0.175 × V_S	V	[3] LIN Spec 2.2 (Par. 20)	P_6.1.6
Wake-up threshold voltage	$V_{BUS,wk}$	0.4 × V_S	0.5 × V_S	0.6 × V_S	V	–	P_6.1.7
Dominant time for bus wake-up (internal analog filter delay)	$t_{WK,bus}$	3	–	15	µs	The overall dominant time for bus wake-up is a sum of $t_{WK,bus}$ + adjustable digital filter time. The digital filter time can be adjusted by PMU.CNF_WAKE_FILTER.CNF_LIN_FT;	P_6.1.8
Bus Transmitter Interface							
Bus recessive output voltage	$V_{BUS,ro}$	0.8 × V_S	–	V_S	V	V_{TxD} = high Level	P_6.1.9
Bus dominant output voltage	$V_{BUS,do}$	–	–	0.22 × V_S	V	Driver Dominant Voltage R_L = 500 Ohm	P_6.1.78

Table 33 Electrical Characteristics LIN Transceiver (cont'd)

V_s = 5.5V to 18V, T_j = -40 °C to +175 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Bus short circuit current	$I_{BUS,sc}$	40	100	150	mA	Current Limitation for driver dominant state driver on V_{BUS} = 18 V; LIN Spec 2.2 (Par. 12)	P_6.1.10
Bus short circuit filter time	$t_{BUS,sc}$	–	5	–	µs	[6]The overall bus short circuit filter time is a sum of tBUS,sc + digital filter time. The digital filter time is 4 µs (typ.)	P_6.1.71
Leakage current (loss of ground)	$I_{BUS\_NO\_GND}$	-1000	-450	1000	µA	V_S = 12 V; 0 < V_{BUS} < 18 V; LIN Spec 2.2 (Par. 15)	P_6.1.11
Leakage current	$I_{BUS\_NO\_BAT}$	–	10	20	µA	V_S = 0 V; V_{BUS} = 18 V; LIN Spec 2.2 (Par. 16)	P_6.1.12
Leakage current	$I_{BUS\_PAS\_dom}$	-1	–	–	mA	V_S = 18 V; V_{BUS} = 0 V; LIN Spec 2.2 (Par. 13)	P_6.1.13
Leakage current	$I_{BUS\_PAS\_rec}$	–	–	20	µA	V_S = 8 V; V_{BUS} = 18 V; LIN Spec 2.2 (Par. 14)	P_6.1.14
Bus pull-up resistance	R_{BUS}	20	30	47	kΩ	Normal mode LIN Spec 2.2 (Par. 26)	P_6.1.15
AC Characteristics - Transceiver Normal Slope Mode							
Propagation delay bus dominant to RxD LOW	$t_{d(L),R}$	0.1	–	6	µs	LIN Spec 2.2 (Param. 31)	P_6.1.16
Propagation delay bus recessive to RxD HIGH	$t_{d(H),R}$	0.1	–	6	µs	LIN Spec 2.2 (Param. 31)	P_6.1.17
Receiver delay symmetry	$t_{sym,R}$	-2	–	2	µs	$t_{sym,R}$ = $t_{d(L),R}$ - $t_{d(H),R}$; LIN Spec 2.2 (Par. 32)	P_6.1.18
Duty cycle D1 Normal Slope Mode (for worst case at 20 kbit/s)	t_{duty1}	0.396	–	–		[4] duty cycle 1 TH_{Rec}(max) = 0.744 × V_S; TH_{Dom}(max) = 0.581 × V_S; V_S = 5.5 … 18 V; t_{bit} = 50 µs; D1 = $t_{bus\_rec(min)}$/2 t_{bit}; LIN Spec 2.2 (Par. 27)	P_6.1.19

Table 42 Electrical Characteristics MOSFET Driver (cont'd)

V_S = 5.5 V to 28 V, T_j = -40 °C to +175 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output voltage VCP vs. VSD-Extended temperature range	V_{CPmin1_HT}	8.4	–	–	V	V_{VSD} = 5.4V, I_{CP}=5 mA, C_{CP1}, C_{CP2} = 220 nF, Bridge Driver enabled 150°C < T_j ≤ 175°C	P_12.1.85
Regulated output voltage VCP vs. VSD	V_{CP}	12	14	16	V	8 V ≤ V_{VSD} ≤ 28, I_{CP}=10mA, C_{CP1}, C_{CP2}=220 nF, f_{CP}=250kHz	P_12.1.49
Turn ON Time	t_{ON_VCP}	10	24	40	us	8 V ≤ V_{VSD} ≤ 28, (25%) of V_{CP} 1)4), C_{CP1}, C_{CP2}=220 nF, f_{CP}=250kHz	P_12.1.59
Rise time	t_{rise_VCP}	20	60	88	us	8 V ≤ V_{VSD} ≤ 28, (25-75%) of V_{CP} 1)5), C_{CP1}, C_{CP2}=220 nF, f_{CP}=250kHz	P_12.1.60

1) Not subject to production test.
2) The condition I_{CP} = 2.5 mA emulates an BLDC Driver with 6 MOSFET switching at 20 KHz with a C_{Load}=3.3nF. Test condition: I_{Gx} = - 100 µA, ICHARGE = IDISCHARGE = 31(max), IDISCHARGEDIV2_N = 1 and ICHARGEDIV2_N = 1.
3) This resistance is connected through a diode between SHx and GHx to ground.
4) This time applies when Bit DRV_CP_CTRL_STS.bit.CP_EN is set
5) This time applies when Bit DRV_CP_CLK_CTRL.bit.CPCLK_EN is set