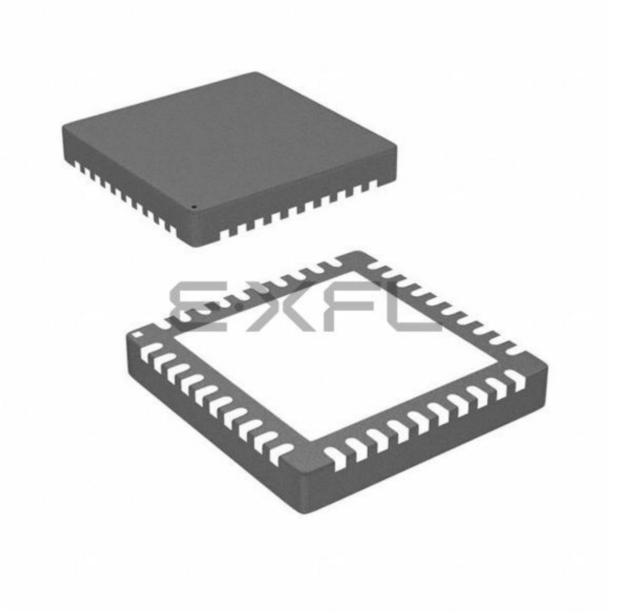


What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, IrDA, SPI, UART/USART
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 10x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN-EP (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk10dx128vfm5

3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

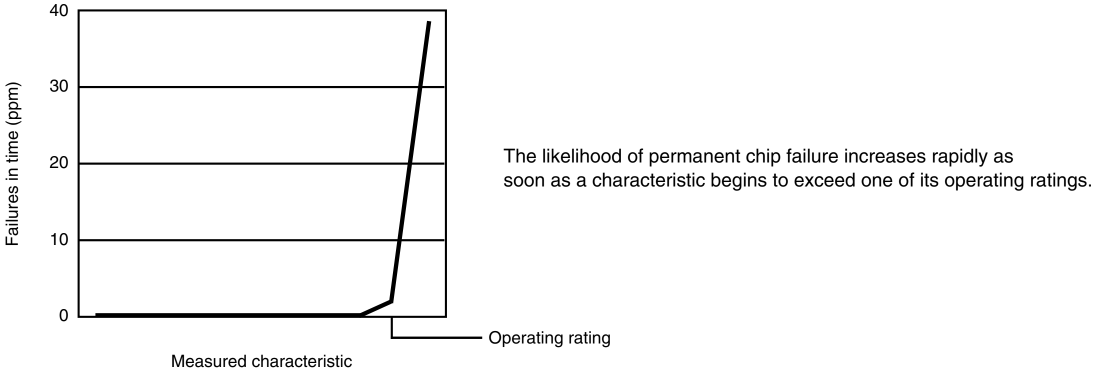
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

3.4.1 Example

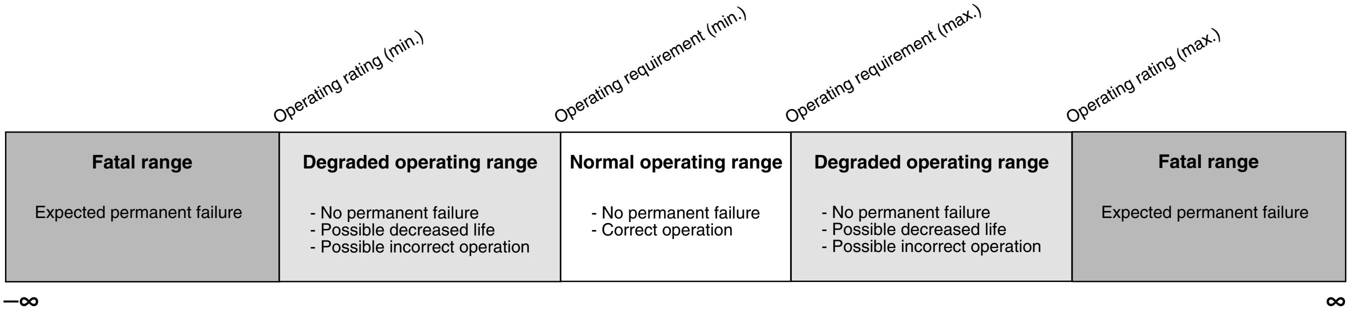
This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

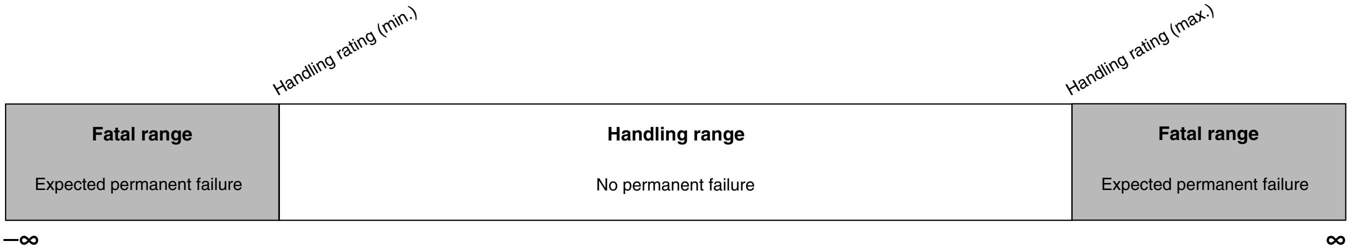
3.5 Result of exceeding a rating



3.6 Relationship between ratings and operating requirements



Operating (power on)



Handling (power off)

3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

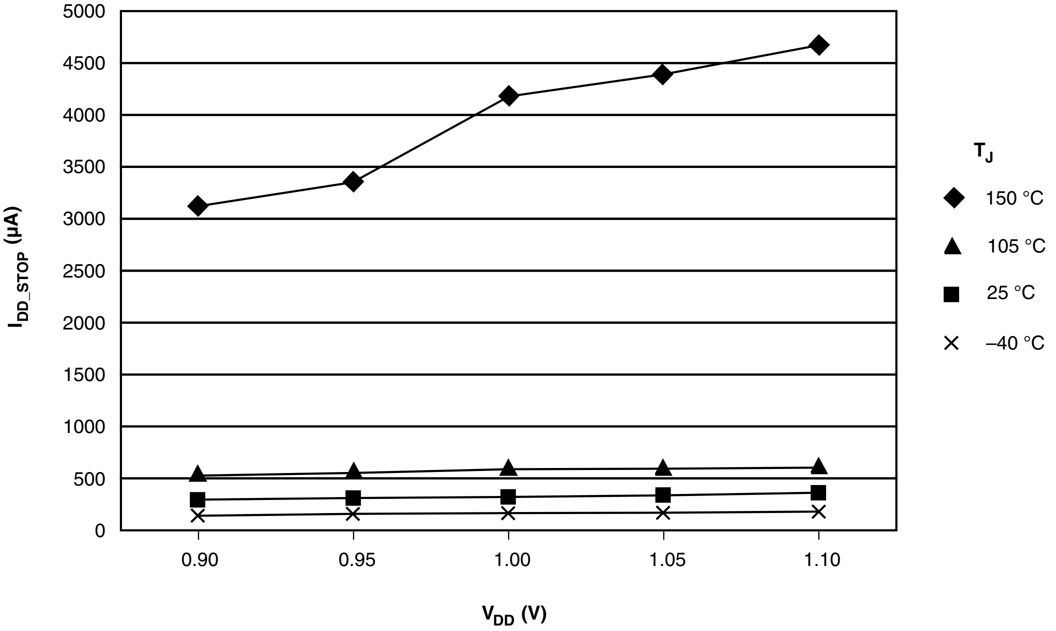
3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

Symbol	Description	Min.	Max.	Unit
I_{DD}	Digital supply current	—	155	mA
V_{DIO}	Digital input voltage (except $\overline{\text{RESET}}$, EXTAL, and XTAL)	–0.3	V_{DD} + 0.3	V
V_{AIO}	Analog[1], $\overline{\text{RESET}}$, EXTAL, and XTAL input voltage	–0.3	V_{DD} + 0.3	V
I_D	Maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{BAT}	RTC battery supply voltage	–0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5 General

5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

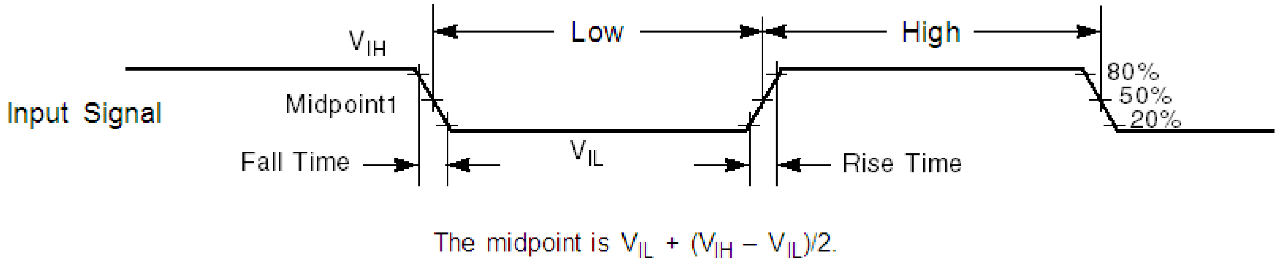


Figure 1. Input signal measurement reference

All digital I/O switching characteristics assume:

1. output pins
   - have C_L=30pF loads,
   - are configured for fast slew rate (PORTx_PCRn[SRE]=0), and
   - are configured for high drive strength (PORTx_PCRn[DSE]=1)
2. input pins
   - have their passive filter disabled (PORTx_PCRn[PFE]=0)

5.2 Nonswitching electrical specifications

5.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — high drive strength				
	• $2.7\ V \le V_{DD} \le 3.6\ V$, $I_{OH} = -9\ mA$	$V_{DD} - 0.5$	—	V	
	• $1.71\ V \le V_{DD} \le 2.7\ V$, $I_{OH} = -3\ mA$	$V_{DD} - 0.5$	—	V	
	Output high voltage — low drive strength				
	• $2.7\ V \le V_{DD} \le 3.6\ V$, $I_{OH} = -2\ mA$	$V_{DD} - 0.5$	—	V	
	• $1.71\ V \le V_{DD} \le 2.7\ V$, $I_{OH} = -0.6\ mA$	$V_{DD} - 0.5$	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	
V_{OL}	Output low voltage — high drive strength				
	• $2.7\ V \le V_{DD} \le 3.6\ V$, $I_{OL} = 9\ mA$	—	0.5	V	
	• $1.71\ V \le V_{DD} \le 2.7\ V$, $I_{OL} = 3\ mA$	—	0.5	V	
	Output low voltage — low drive strength				
	• $2.7\ V \le V_{DD} \le 3.6\ V$, $I_{OL} = 2\ mA$	—	0.5	V	
	• $1.71\ V \le V_{DD} \le 2.7\ V$, $I_{OL} = 0.6\ mA$	—	0.5	V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{IN}	Input leakage current (per pin)				1
	• @ full temperature range	—	1.0	μA	
	• @ 25 °C	—	0.1	μA	
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	μA	
I_{OZ}	Total Hi-Z (off-state) leakage current (all input pins)	—	4	μA	
R_{PU}	Internal pullup resistors	22	50	kΩ	2
R_{PD}	Internal pulldown resistors	22	50	kΩ	3

1. Tested by ganged leakage method
2. Measured at Vinput = V_{SS}
3. Measured at Vinput = V_{DD}

5.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 50 MHz
- Bus clock = 50 MHz
- Flash clock = 25 MHz

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	—	300	μs	1
	• VLLS0 → RUN	—	130	μs	
	• VLLS1 → RUN	—	130	μs	
	• VLLS2 → RUN	—	70	μs	
	• VLLS3 → RUN	—	70	μs	
	• LLS → RUN	—	6	μs	
	• VLPS → RUN	—	5.2	μs	
	• STOP → RUN	—	5.2	μs	

1. Normal boot (FTFL_OPT[LPBOOT]=1)

5.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash					2
	• @ 1.8V	—	13.7	15.1	mA	
	• @ 3.0V	—	13.9	15.3	mA	
I_{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash					3, 4
	• @ 1.8V	—	16.1	18.2	mA	
	• @ 3.0V					
	• @ 25°C	—	16.3	17.7	mA	
	• @ 125°C	—	16.7	18.4	mA	
I_{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled	—	7.5	8.4	mA	2
I_{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled	—	5.6	6.4	mA	5

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled					
	• @ –40 to 25°C	—	0.176	0.859	μA	
	• @ 70°C	—	2.2	13.1	μA	
	• @ 105°C	—	13	23.9	μA	
I_{DD_VBAT}	Average current with RTC and 32kHz disabled at 3.0 V					
	• @ –40 to 25°C	—	0.19	0.22	μA	
	• @ 70°C	—	0.49	0.64	μA	
	• @ 105°C	—	2.2	3.2	μA	
I_{DD_VBAT}	Average current when CPU is not accessing RTC registers					9
	• @ 1.8V					
	• @ –40 to 25°C	—	0.57	0.67	μA	
	• @ 70°C	—	0.90	1.2	μA	
	• @ 105°C	—	2.4	3.5	μA	
	• @ 3.0V					
	• @ –40 to 25°C	—	0.67	0.94	μA	
	• @ 70°C	—	1.0	1.4	μA	
	• @ 105°C	—	2.7	3.9	μA	

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. 50MHz core and system clock, 25MHz bus clock, and 25MHz flash clock . MCG configured for FEI mode. All peripheral clocks disabled.
3. 50MHz core and system clock, 25MHz bus clock, and 25MHz flash clock. MCG configured for FEI mode. All peripheral clocks enabled, and peripherals are in active operation.
4. Max values are measured with CPU executing DSP instructions
5. 25MHz core and system clock, 25MHz bus clock, and 12.5MHz flash clock. MCG configured for FEI mode.
6. 4 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing from flash.
7. 4 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing from flash.
8. 4 MHz core, system, and bus clock and 1MHz flash clock. MCG configured for BLPE mode. All peripheral clocks disabled.
9. Includes 32kHz oscillator current and RTC operation.

5.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG in FBE mode
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFL

Table 9. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Notes
f_{LPTMR_pin}	LPTMR clock	—	25	MHz	
f_{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz	
f_{I2S_MCLK}	I2S master clock	—	12.5	MHz	
f_{I2S_BCLK}	I2S bit clock	—	4	MHz	

1. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

5.3.2 General switching specifications

These general purpose specifications apply to all signals configured for GPIO, UART, CMT, and I^2C signals.

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	3
	GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	ns	3
	External reset pulse width (digital glitch filter disabled)	100	—	ns	3
	Mode select ($\overline{EZP\_CS}$) hold time after reset deassertion	2	—	Bus clock cycles	
	Port rise and fall time (high drive strength) • Slew disabled • $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$ • Slew enabled • $1.71 \le V_{DD} \le 2.7V$ • $2.7 \le V_{DD} \le 3.6V$	— — — —	13 7 36 24	ns ns ns ns	4

Table continues on the next page...

Board type	Symbol	Description	32 QFN	Unit	Notes
Single-layer (1s)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	78	°C/W	1,3
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	27	°C/W	,
—	$R_{\theta JB}$	Thermal resistance, junction to board	12	°C/W	5
—	$R_{\theta JC}$	Thermal resistance, junction to case	1.5	°C/W	6
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	6	°C/W	7

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)* with the single layer board horizontal. For the LQFP, the board meets the JESD51-3 specification. For the MAPBGA, the board meets the JESD51-9 specification.
3. Determined according to JEDEC Standard JESD51-6, *Integrated Circuits Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)* with the board horizontal.
5. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*. Board temperature is measured on the top surface of the board near the package.
6. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
7. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*.

6 Peripheral operating requirements and behaviors

6.1 Core modules

6.1.1 JTAG electricals

Table 12. JTAG voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	5.5	V

Table continues on the next page...

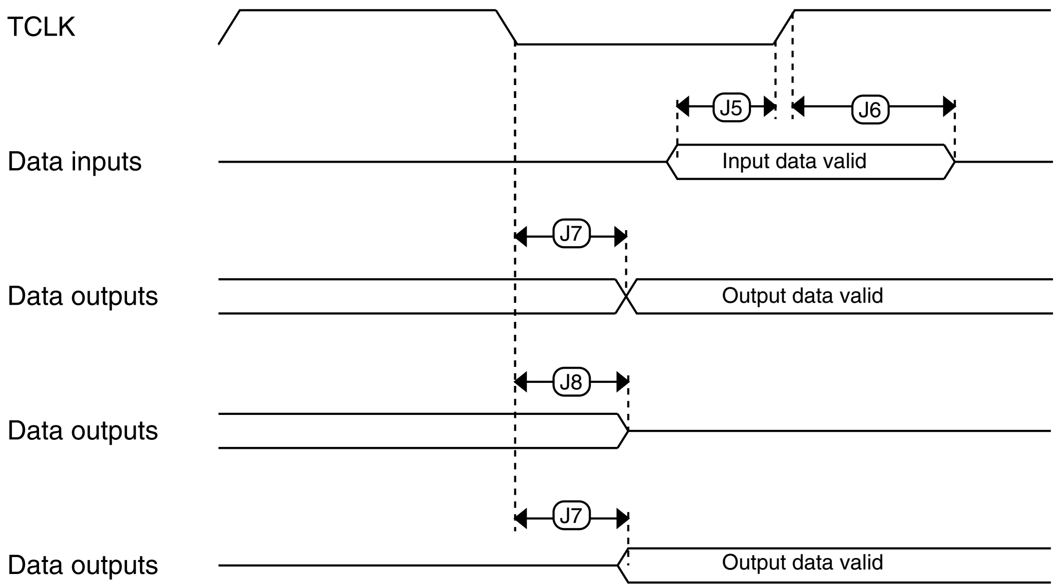


Figure 5. Boundary scan (JTAG) timing

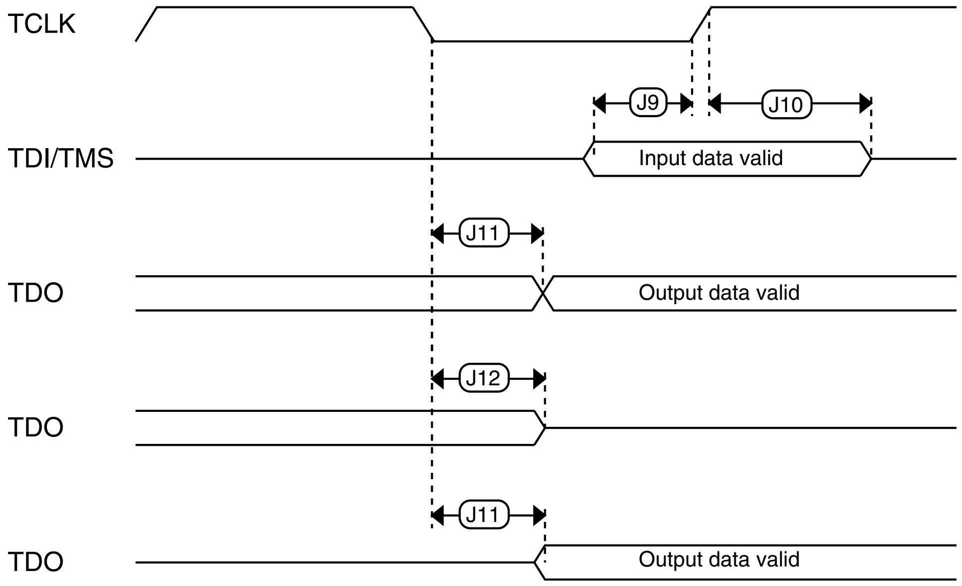


Figure 6. Test Access Port timing

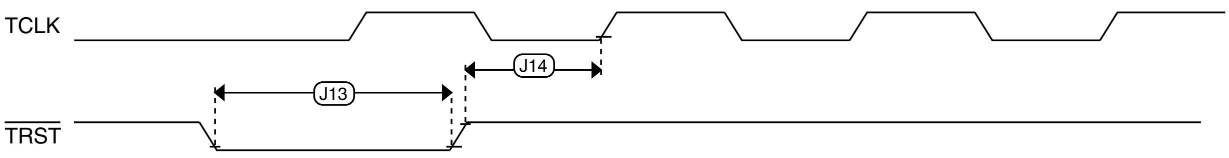


Figure 7. TRST timing

6.2 System modules

There are no specifications necessary for the device's system modules.

6.3 Clock modules

6.3.1 MCG specifications

Table 13. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal VDD and 25 °C	—	32.768	—	kHz	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM	—	± 0.3	± 0.6	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	+0.5/-0.7	± 3	$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C	—	± 0.3	—	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal VDD and 25°C	—	4	—	MHz	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal VDD and 25 °C	3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00	(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	(16/5) x f_{ints_t}	—	—	kHz	
FLL						

Table continues on the next page...

5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.2.2 Oscillator frequency specifications

Table 15. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FBE to FEI mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

6.3.3 32 kHz Oscillator Electrical Characteristics

This section describes the module electrical characteristics.

6.3.3.1 32 kHz oscillator DC electrical specifications

Table 16. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	MΩ

Table continues on the next page...

6.4.1.2 Flash timing specifications — commands

Table 19. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Read 1s Block execution time					
$t_{rd1blk32k}$	• 32 KB data flash	—	—	0.5	ms	
$t_{rd1blk128k}$	• 128 KB program flash	—	—	1.7	ms	
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)	—	—	60	μs	1
t_{pgmchk}	Program Check execution time	—	—	45	μs	1
t_{rdrsrc}	Read Resource execution time	—	—	30	μs	1
t_{pgm4}	Program Longword execution time	—	65	145	μs	
	Erase Flash Block execution time					2
$t_{ersblk32k}$	• 32 KB data flash	—	55	465	ms	
$t_{ersblk128k}$	• 128 KB program flash	—	61	495	ms	
t_{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
	Program Section execution time					
$t_{pgmsec512}$	• 512 B flash	—	4.7	—	ms	
$t_{pgmsec1k}$	• 1 KB flash	—	9.3	—	ms	
t_{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	
t_{rdonce}	Read Once execution time	—	—	25	μs	1
$t_{pgmonce}$	Program Once execution time	—	65	—	μs	
t_{ersall}	Erase All Blocks execution time	—	115	1000	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1
	Program Partition for EEPROM execution time					
$t_{pgmpart32k}$	• 32 KB FlexNVM	—	70	—	ms	
	Set FlexRAM Function execution time:					
$t_{setramff}$	• Control Code 0xFF	—	50	—	μs	
$t_{setram8k}$	• 8 KB EEPROM backup	—	0.3	0.5	ms	
$t_{setram32k}$	• 32 KB EEPROM backup	—	0.7	1.0	ms	
Byte-write to FlexRAM for EEPROM operation						
$t_{eewr8bers}$	Byte-write to erased FlexRAM location execution time	—	175	260	μs	3
	Byte-write to FlexRAM execution time:					
$t_{eewr8b8k}$	• 8 KB EEPROM backup	—	340	1700	μs	
$t_{eewr8b16k}$	• 16 KB EEPROM backup	—	385	1800	μs	
$t_{eewr8b32k}$	• 32 KB EEPROM backup	—	475	2000	μs	

Table continues on the next page...

Table 21. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
$t_{nvmretd1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycd}$	Cycling endurance	10 K	50 K	—	cycles	2
FlexRAM as EEPROM						
$t_{nvmretee100}$	Data retention up to 100% of write endurance	5	50	—	years	
$t_{nvmretee10}$	Data retention up to 10% of write endurance	20	100	—	years	
	Write endurance					3
$n_{nvmwree16}$	• EEPROM backup to FlexRAM ratio = 16	35 K	175 K	—	writes	
$n_{nvmwree128}$	• EEPROM backup to FlexRAM ratio = 128	315 K	1.6 M	—	writes	
$n_{nvmwree512}$	• EEPROM backup to FlexRAM ratio = 512	1.27 M	6.4 M	—	writes	
$n_{nvmwree4k}$	• EEPROM backup to FlexRAM ratio = 4096	10 M	50 M	—	writes	
$n_{nvmwree8k}$	• EEPROM backup to FlexRAM ratio = 8192	20 M	100 M	—	writes	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at $-40°C \le T_j \le 125°C$.
3. Write endurance represents the number of writes to each FlexRAM location at $-40°C \le Tj \le 125°C$ influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup. Minimum and typical values assume all byte-writes to FlexRAM.

6.4.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

The bytes not assigned to data flash via the FlexNVM partition code are used by the flash memory module to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

$$\text{Writes\_FlexRAM} = \frac{\text{EEPROM} - 2 \times \text{EEESIZE}}{\text{EEESIZE}} \times \text{Write\_efficiency} \times n_{nvmcycd}$$

where

- Writes_FlexRAM — minimum number of writes to each FlexRAM location

Table 23. 16-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
C_{rate}	ADC conversion rate	16 bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	5

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. DC potential difference.
3. This resistance is external to MCU. The analog source resistance should be kept as low as possible in order to achieve the best results. The results in this datasheet were derived from a system which has <8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to <1ns.
4. To use the maximum ADC conversion clock frequency, the ADHSC bit should be set and the ADLPC bit should be clear.
5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool: http://cache.freescale.com/files/soft_dev_tools/software/app_software/converters/ADC_CALCULATOR_CNV.zip?fpsp=1

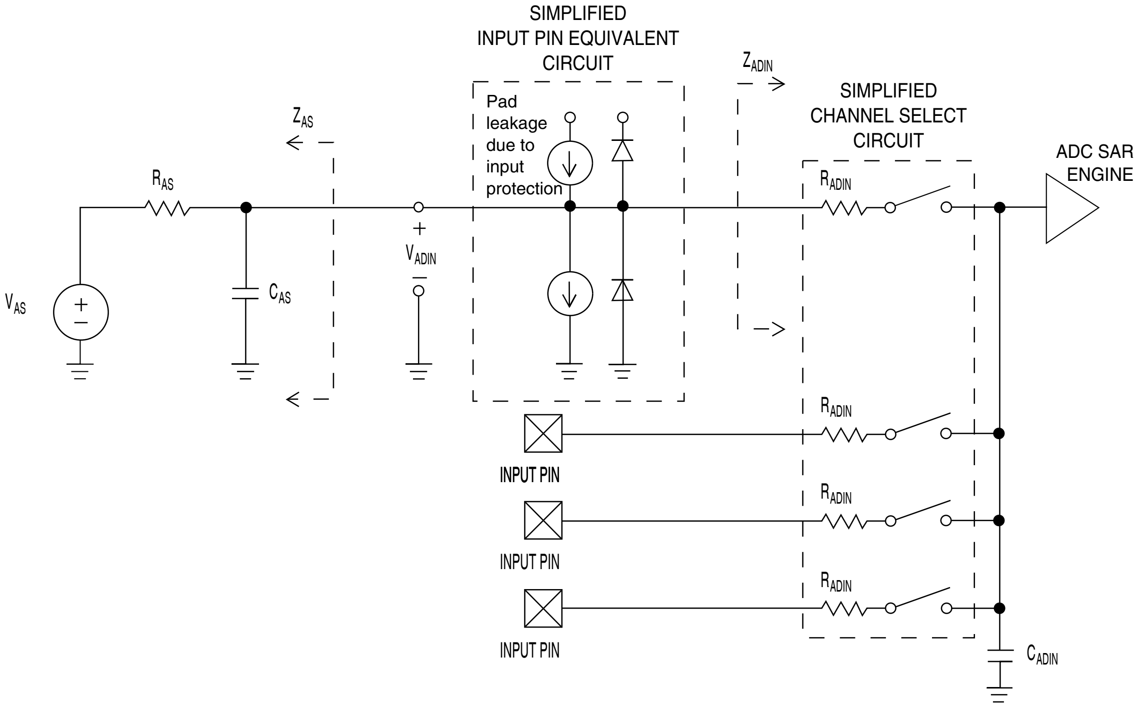


Figure 10. ADC input impedance equivalency diagram

6.6.1.2 16-bit ADC electrical characteristics

Table 24. 16-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3

Table continues on the next page...

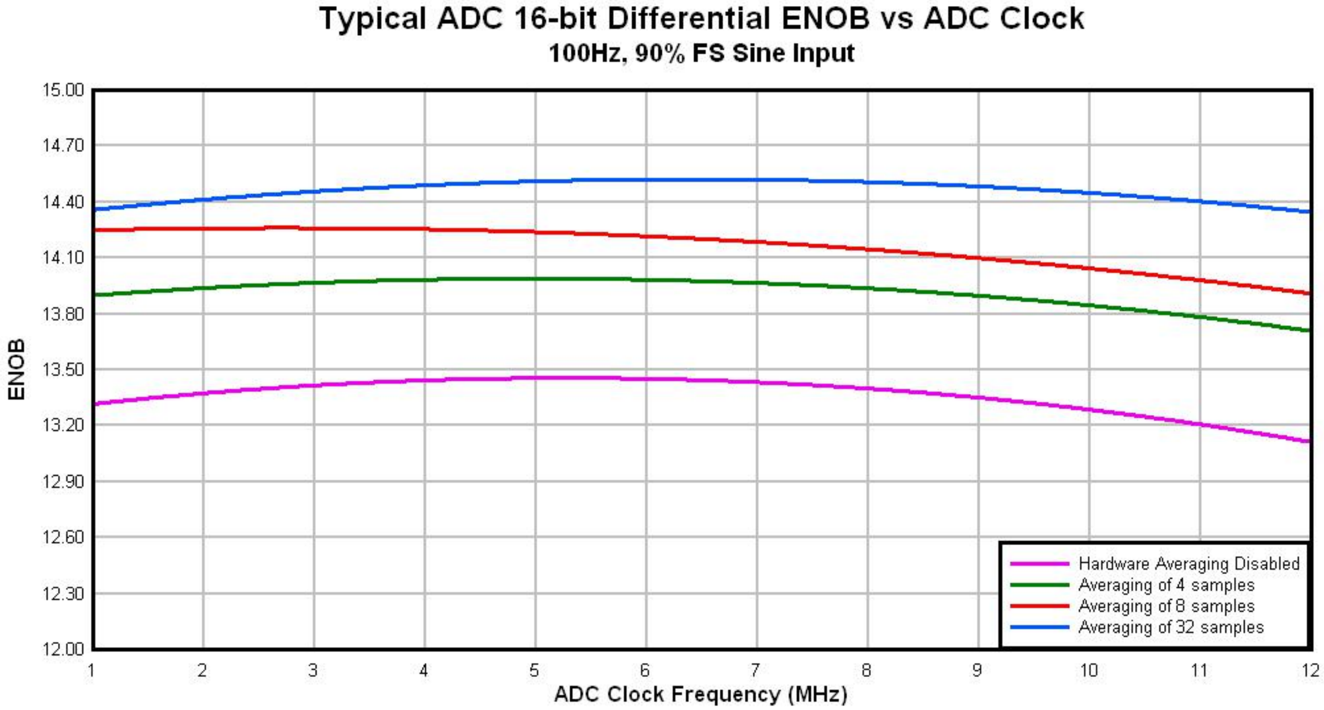


Figure 11. Typical ENOB vs. ADC_CLK for 16-bit differential mode

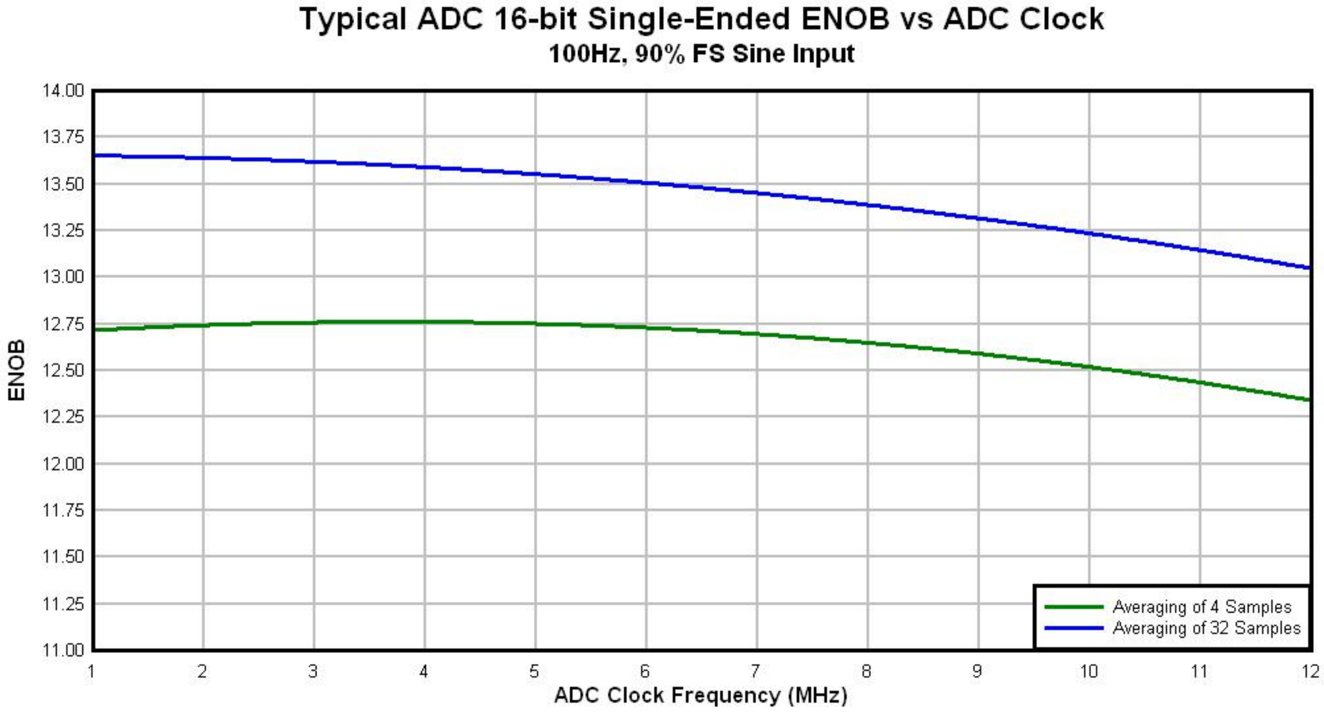


Figure 12. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

6.6.2 CMP and 6-bit DAC electrical specifications

Table 25. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	μA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	μA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1] • CR0[HYSTCTR] = 00 • CR0[HYSTCTR] = 01 • CR0[HYSTCTR] = 10 • CR0[HYSTCTR] = 11	 — — — —	 5 10 20 30	 — — — —	 mV mV mV mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	μs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	μA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}-0.6V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}$/64

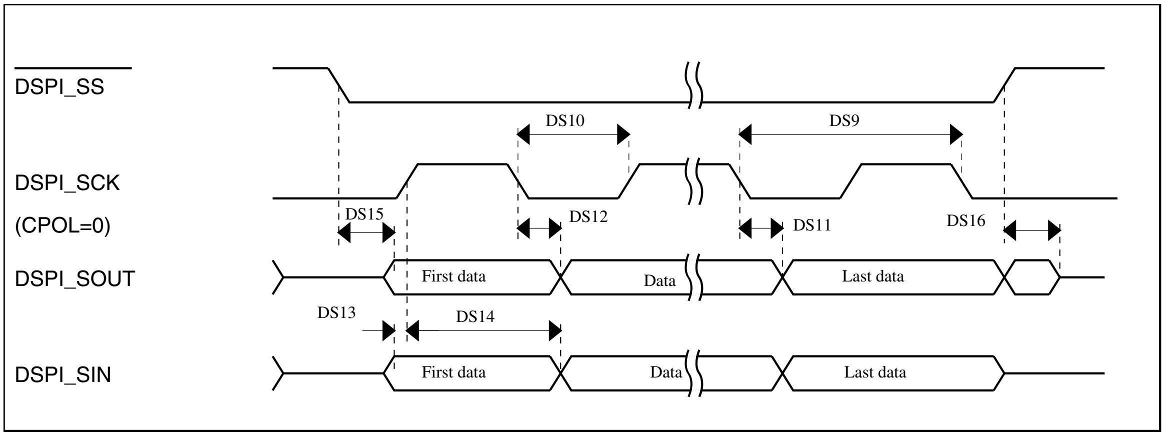


Figure 18. DSPI classic SPI timing — slave mode

6.8.3 I^{2}C switching specifications

See General switching specifications.

6.8.4 UART switching specifications

See General switching specifications.

6.8.5 I2S/SAI Switching Specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to http://www.freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
32-pin QFN	98ARE10566D

8 Pinout

8.1 K10 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

32 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
1	VDD	VDD	VDD								
2	VSS	VSS	VSS								
3	PTE16	ADC0_SE4a	ADC0_SE4a	PTE16	SPI0_PCS0	UART2_TX	FTM_CLKIN0		FTM0_FLT3		
4	PTE17	ADC0_SE5a	ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	FTM_CLKIN1		LPTMR0_ALT3		
5	PTE18	ADC0_SE6a	ADC0_SE6a	PTE18	SPI0_SOUT	UART2_CTS_b	I2C0_SDA				
6	PTE19	ADC0_SE7a	ADC0_SE7a	PTE19	SPI0_SIN	UART2_RTS_b	I2C0_SCL				
7	VDDA	VDDA	VDDA								
8	VSSA	VSSA	VSSA								
9	XTAL32	XTAL32	XTAL32								
10	EXTAL32	EXTAL32	EXTAL32								
11	VBAT	VBAT	VBAT								
12	PTA0	JTAG_TCLK/SWD_CLK/EZP_CLK	TSI0_CH1	PTA0	UART0_CTS_b/UART0_COL_b	FTM0_CH5				JTAG_TCLK/SWD_CLK	EZP_CLK
13	PTA1	JTAG_TDI/EZP_DI	TSI0_CH2	PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI

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Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
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www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

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