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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I ² C, IrDA, SPI, UART/USART
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 10x16b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-VFQFN Exposed Pad
Supplier Device Package	32-QFN-EP (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk10dx32vfm5

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to http://www.freescale.com and perform a part number search for the following device numbers: PK10 and MK10.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q K## A M FFF R T PP CC N

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	 M = Fully qualified, general market flow P = Prequalification
K##	Kinetis family	• K10
A	Key attribute	 D = Cortex-M4 w/ DSP F = Cortex-M4 w/ DSP and FPU
М	Flash memory type	 N = Program flash only X = Program flash and FlexMemory

Table continues on the next page ...

3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

Symbol	Description	Min.	Max.	Unit
I _{WP}	Digital I/O weak pullup/ pulldown current	10	130	μΑ

3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free	_	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.

2. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.

2. Determined according to JEDEC Standard JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components.

4.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V _{DD}	Digital supply voltage	-0.3	3.8	V

Table continues on the next page...

General

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V _{LVW1H}	Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V _{LVW2H}	Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V _{LVW3H}	 Level 3 falling (LVWV=10) 	2.82	2.90	2.98	V	
V _{LVW4H}	Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V _{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	_	±80	_	mV	
V _{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V _{LVW1L}	Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V _{LVW2L}	Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V _{LVW3L}	 Level 3 falling (LVWV=10) 	1.94	2.00	2.06	V	
V _{LVW4L}	Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V _{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±60	—	mV	
V _{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t _{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

Table 2. V_{DD} supply LVD and POR operating requirements (continued)

1. Rising thresholds are falling threshold + hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

Symbol	Description	Min.	Max.	Unit	Notes
t _{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execution of the first instruction across the operating temperature range of the chip.	_	300	μs	1
	• VLLS0 \rightarrow RUN	_	130	μs	
	• VLLS1 \rightarrow RUN	_	130	μs	
	• VLLS2 \rightarrow RUN	—	70	μs	
	• VLLS3 \rightarrow RUN	_	70	μs	
	• LLS → RUN	—	6	μs	
	• VLPS → RUN	_	5.2	μs	
	• STOP → RUN	_	5.2	μs	

Table 5. Power mode transition operating behaviors

1. Normal boot (FTFL_OPT[LPBOOT]=1)

5.2.5 Power consumption operating behaviors

Table 6. Power consumption operating behaviors

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DDA}	Analog supply current	_	—	See note	mA	1
I _{DD_RUN}	Run mode current — all peripheral clocks disabled, code executing from flash • @ 1.8V • @ 3.0V		13.7 13.9	15.1 15.3	mA mA	2
I _{DD_RUN}	Run mode current — all peripheral clocks enabled, code executing from flash • @ 1.8V	_	16.1	18.2	mA	3, 4
	• @ 3.0V	_	16.3	17.7	mA	
	• @ 25°C • @ 125°C	_	16.7	18.4	mA	
I _{DD_WAIT}	Wait mode high frequency current at 3.0 V — all peripheral clocks disabled		7.5	8.4	mA	2
I _{DD_WAIT}	Wait mode reduced frequency current at 3.0 V — all peripheral clocks disabled		5.6	6.4	mA	5

Table continues on the next page...





Figure 3. VLPR mode supply current vs. core frequency

5.2.6 EMC radiated emissions operating behaviors Table 7. EMC radiated emissions operating behaviors for 64LQFP

Symbol	Description	Frequency band (MHz)	Тур.	Unit	Notes
V _{RE1}	Radiated emissions voltage, band 1	0.15–50	19	dBµV	1,2
V _{RE2}	Radiated emissions voltage, band 2	50–150	21	dBµV	
V _{RE3}	Radiated emissions voltage, band 3	150–500	19	dBµV	
V _{RE4}	Radiated emissions voltage, band 4	500–1000	11	dBµV	
V _{RE_IEC}	IEC level	0.15–1000	L	—	2, 3

 Determined according to IEC Standard 61967-1, Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions and IEC Standard 61967-2, Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method. Measurements were made while the microcontroller was running basic application code. The reported

emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

- 2. $V_{DD} = 3.3 \text{ V}$, $T_A = 25 \text{ °C}$, $f_{OSC} = 12 \text{ MHz}$ (crystal), $f_{SYS} = 48 \text{ MHz}$, $f_{BUS} = 48 \text{ MHz}$
- 3. Specified according to Annex D of IEC Standard 61967-2, Measurement of Radiated Emissions TEM Cell and Wideband TEM Cell Method

5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

- 1. Go to http://www.freescale.com.
- 2. Perform a keyword search for "EMC design."

5.2.8 Capacitance attributes

Table 8. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C _{IN_A}	Input capacitance: analog pins	_	7	pF
C _{IN_D}	Input capacitance: digital pins	—	7	pF

5.3 Switching specifications

5.3.1 Device clock specifications

Table 9. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Notes
	Normal run mode	9			-
f _{SYS}	System and core clock	_	50	MHz	
f _{BUS}	Bus clock		50	MHz	
f _{FLASH}	Flash clock		25	MHz	
f _{LPTMR}	LPTMR clock		25	MHz	
	VLPR mode ¹				
f _{SYS}	System and core clock	—	4	MHz	
f _{BUS}	Bus clock	—	4	MHz	
f _{FLASH}	Flash clock	_	1	MHz	
f _{ERCLK}	External reference clock	_	16	MHz	

Table continues on the next page ...

Symbol	Description	Min.	Max.	Unit	Notes
	Port rise and fall time (low drive strength)				5
	Slew disabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	12	ns	
	• $2.7 \le V_{DD} \le 3.6V$	_	6	ns	
	Slew enabled				
	• $1.71 \le V_{DD} \le 2.7V$	—	36	ns	
	• $2.7 \le V_{DD} \le 3.6V$	_	24	ns	
		1			

Table 10. General switching specifications (continued)

- 1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop, VLPS, LLS, and VLLSx modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
- 2. The greater synchronous and asynchronous timing must be met.
- 3. This is the minimum pulse width that is guaranteed to be recognized as a pin interrupt request in Stop, VLPS, LLS, and VLLSx modes.
- 4. 75pF load
- 5. 15pF load

5.4 Thermal specifications

5.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit
TJ	Die junction temperature	-40	125	°C
T _A	Ambient temperature	-40	105	°C

5.4.2 Thermal attributes

Board type	Symbol	Description	32 QFN	Unit	Notes
Single-layer (1s)	R _{eJA}	Thermal resistance, junction to ambient (natural convection)	94	°C/W	1, 2
Four-layer (2s2p)	R _{ejA}	Thermal resistance, junction to ambient (natural convection)	32	°C/W	1, 3

Table continues on the next page...

Symbol	Description		Min.	Тур.	Max.	Unit	Notes
f _{fll_ref}	FLL reference free	quency range	31.25	—	39.0625	kHz	
f _{dco}	DCO output frequency range	Low range (DRS=00) 640 × f _{fll_ref}	20	20.97	25	MHz	2, 3
		Mid range (DRS=01) 1280 × f _{fll_ref}	40	41.94	50	MHz	
		Mid-high range (DRS=10) 1920 × f _{fll_ref}	60	62.91	75	MHz	
		High range (DRS=11) 2560 × f _{fll_ref}	80	83.89	100	MHz	
f _{dco_t_DMX3}	X3 DCO output frequency	Low range (DRS=00) 732 × f _{fll_ref}	_	23.99	—	MHz	4, 5
		Mid range (DRS=01) 1464 × f _{fll_ref}	_	47.97	_	MHz	
		Mid-high range (DRS=10) 2197 × f _{fll_ref}	_	71.99	_	MHz	
		High range (DRS=11) 2929 × f _{fll_ref}	_	95.98	_	MHz	
J _{cyc_fll}	FLL period jitter		_	180	_	ps	
	 f_{VCO} = 48 M f_{VCO} = 98 M 	Hz Hz	_	150	_		
t _{fll_acquire}	FLL target frequer	ncy acquisition time	—		1	ms	6
	-	Р	LL				
f _{vco}	VCO operating fre	quency	48.0	—	100	MHz	
I _{pll}	PLL operating cur PLL @ 96 M 2 MHz, VDI	rent 1Hz (f _{osc_hi_1} = 8 MHz, f _{pll_ref} = V multiplier = 48)	_	1060	_	μΑ	7
I _{pll}	PLL operating cur • PLL @ 48 M 2 MHz, VDI	rent 1Hz (f _{osc_hi_1} = 8 MHz, f _{pll_ref} = V multiplier = 24)		600	_	μA	7
f _{pll_ref}	PLL reference free	quency range	2.0	—	4.0	MHz	
J _{cyc_pll}	PLL period jitter (F	RMS)					8
	• f _{vco} = 48 MH	lz	-	120	—	ps	
	• f _{vco} = 100 M	Hz	-	50	-	ps	

Table 13. MCG specifications (continued)

Table continues on the next page ...

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	25	_	μA	
	• 4 MHz	—	400	_	μA	
	• 8 MHz (RANGE=01)	—	500	_	μA	
	• 16 MHz	—	2.5	_	mA	
	• 24 MHz	—	3	_	mA	
	• 32 MHz	—	4	_	mA	
C _x	EXTAL load capacitance	—	—			2, 3
Cy	XTAL load capacitance	—	—	—		2, 3
R _F	Feedback resistor — low-frequency, low-power mode (HGO=0)	_	—	_	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	_	10	_	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—		MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	_	1	_	MΩ	
R _S	Series resistor — low-frequency, low-power mode (HGO=0)	—	_	_	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	_	200	_	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	_	_	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)					
			0		kΩ	
V _{pp} ⁵	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)		0.6	_	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	_	V _{DD}	_	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	_	0.6	_	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	_	V _{DD}	_	V	

Table 14. Oscillator DC electrical specifications (continued)

1. V_{DD} =3.3 V, Temperature =25 °C

2. See crystal or resonator manufacturer's recommendation

3. C_x, C_y can be provided by using either the integrated capacitors or by using external components.

4. When low power mode is selected, R_F is integrated and must not be attached externally.

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
t _{nvmretd1k}	Data retention after up to 1 K cycles	20	100	_	years	
n _{nvmcycd}	Cycling endurance	_	cycles	2		
	FlexRAM as	s EEPROM				
t _{nvmretee100}	Data retention up to 100% of write endurance	5	50		years	
t _{nvmretee10}	Data retention up to 10% of write endurance	20	100		years	
	Write endurance					3
n _{nvmwree16}	• EEPROM backup to FlexRAM ratio = 16	35 K	175 K	—	writes	
n _{nvmwree128}	• EEPROM backup to FlexRAM ratio = 128	315 K	1.6 M	—	writes	
n _{nvmwree512}	• EEPROM backup to FlexRAM ratio = 512	1.27 M	6.4 M	—	writes	
n _{nvmwree4k}	• EEPROM backup to FlexRAM ratio = 4096	10 M	50 M	—	writes	
n _{nvmwree8k}	• EEPROM backup to FlexRAM ratio = 8192	20 M	100 M	—	writes	

Table 21. NVM reliability specifications (continued)

 Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.

2. Cycling endurance represents number of program/erase cycles at -40°C \leq T_j \leq 125°C.

3. Write endurance represents the number of writes to each FlexRAM location at -40°C ≤Tj ≤ 125°C influenced by the cycling endurance of the FlexNVM (same value as data flash) and the allocated EEPROM backup. Minimum and typical values assume all byte-writes to FlexRAM.

6.4.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

The bytes not assigned to data flash via the FlexNVM partition code are used by the flash memory module to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

Writes_FlexRAM =
$$\frac{\text{EEPROM} - 2 \times \text{EEESIZE}}{\text{EEESIZE}} \times \text{Write}_\text{efficiency} \times n_{\text{nvmcycd}}$$

where

• Writes_FlexRAM — minimum number of writes to each FlexRAM location

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
C _{rate}	ADC conversion rate	16 bit modes No ADC hardware averaging	37.037	_	461.467	Ksps	5
		Continuous conversions enabled, subsequent conversion time					

Table 23. 16-bit ADC operating conditions (continued)

- Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- 2. DC potential difference.
- 3. This resistance is external to MCU. The analog source resistance should be kept as low as possible in order to achieve the best results. The results in this datasheet were derived from a system which has <8 Ω analog source resistance. The R_{AS}/ C_{AS} time constant should be kept to <1ns.
- 4. To use the maximum ADC conversion clock frequency, the ADHSC bit should be set and the ADLPC bit should be clear.
- 5. For guidelines and examples of conversion rate calculation, download the ADC calculator tool: http://cache.freescale.com/ files/soft_dev_tools/software/app_software/converters/ADC_CALCULATOR_CNV.zip?fpsp=1



Figure 10. ADC input impedance equivalency diagram

6.6.1.2 16-bit ADC electrical characteristics Table 24. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions ¹	Min.	Typ. ²	Max.	Unit	Notes
I _{DDA_ADC}	Supply current		0.215		1.7	mA	3

Table continues on the next page ...

Num	Description	Min.	Max.	Unit	Notes
DS3	DSPI_PCSn valid to DSPI_SCK delay	(t _{BUS} x 2) – 4	_	ns	2
DS4	DSPI_SCK to DSPI_PCSn invalid delay	(t _{BUS} x 2) – 4	_	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	_	8.5	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-1.2	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	19.1	_	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	_	ns	

 Table 28.
 Master mode DSPI timing (full voltage range) (continued)

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.

2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].

3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].



Figure 17. DSPI classic SPI timing — master mode

Table 29. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	_	6.25	MHz
DS9	DSPI_SCK input cycle time	8 x t _{BUS}	—	ns
DS10	DSPI_SCK input high/low time	(t _{SCK} /2) - 4	(t _{SCK/2)} + 4	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	24	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	3.2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	DSPI_SS active to DSPI_SOUT driven	_	19	ns
DS16	DSPI_SS inactive to DSPI_SOUT not driven		19	ns

Table 32. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	_	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	_	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	_	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	_	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	45	_	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	_	ns



Figure 21. I2S/SAI timing — master modes

Table 33. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	_	ns

Table continues on the next page...

Table 33. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	_	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	3	_	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	63	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	_	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	_	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear





6.9 Human-machine interfaces (HMI)

6.9.1 TSI electrical specifications

Table 34. TSI electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{DDTSI}	Operating voltage	1.71		3.6	V	
C _{ELE}	Target electrode capacitance range	1	20	500	pF	1

Table continues on the next page ...

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
f _{REFmax}	Reference oscillator frequency	—	8	15	MHz	2, 3
f _{ELEmax}	Electrode oscillator frequency	—	1	1.8	MHz	2, 4
C _{REF}	Internal reference capacitor	_	1	_	pF	
V _{DELTA}	Oscillator delta voltage	_	500	_	mV	2, 5
I _{REF}	Reference oscillator current source base current • 2 μA setting (REFCHRG = 0)	_	2	3	μΑ	2, 6
	• 32 µA setting (REFCHRG = 15)	—	36	50		
I _{ELE}	Electrode oscillator current source base current • 2 µA setting (EXTCHRG = 0)	_	2	3	μA	2, 7
	• 32 µA setting (EXTCHRG = 15)	_	36	50		
Pres5	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	8
Pres20	Electrode capacitance measurement precision	—	8.3333	38400	fF/count	9
Pres100	Electrode capacitance measurement precision		8.3333	38400	fF/count	10
MaxSens	Maximum sensitivity	0.008	1.46	_	fF/count	11
Res	Resolution	_	—	16	bits	
T _{Con20}	Response time @ 20 pF	8	15	25	μs	12
I _{TSI_RUN}	Current added in run mode	_	55	—	μA	
I _{TSI_LP}	Low power mode current adder	_	1.3	2.5	μA	13

Table 34.	TSI electrical s	pecifications	(continued)
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1. The TSI module is functional with capacitance values outside this range. However, optimal performance is not guaranteed.

2. Fixed external capacitance of 20 pF.

3. REFCHRG = 2, EXTCHRG=0.

4. REFCHRG = 0, EXTCHRG = 10.

5. $V_{DD} = 3.0 V.$

6. The programmable current source value is generated by multiplying the SCANC[REFCHRG] value and the base current.

7. The programmable current source value is generated by multiplying the SCANC[EXTCHRG] value and the base current.

8. Measured with a 5 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 8; lext = 16.

9. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 128, NSCN = 2; lext = 16.

10. Measured with a 20 pF electrode, reference oscillator frequency of 10 MHz, PS = 16, NSCN = 3; lext = 16.

11. Sensitivity defines the minimum capacitance change when a single count from the TSI module changes. Sensitivity depends on the configuration used. The documented values are provided as examples calculated for a specific configuration of operating conditions using the following equation: (C_{ref} * I_{ext})/(I_{ref} * PS * NSCN)

The typical value is calculated with the following configuration:

 $I_{ext} = 6 \ \mu A \ (EXTCHRG = 2), PS = 128, NSCN = 2, I_{ref} = 16 \ \mu A \ (REFCHRG = 7), C_{ref} = 1.0 \ pF$

The minimum value is calculated with the following configuration:

I_{ext} = 2 μA (EXTCHRG = 0), PS = 128, NSCN = 32, I_{ref} = 32 μA (REFCHRG = 15), C_{ref} = 0.5 pF

The highest possible sensitivity is the minimum value because it represents the smallest possible capacitance that can be measured by a single count.

- 12. Time to do one complete measurement of the electrode. Sensitivity resolution of 0.0133 pF, PS = 0, NSCN = 0, 1 electrode, EXTCHRG = 7.
- 13. REFCHRG=0, EXTCHRG=4, PS=7, NSCN=0F, LPSCNITV=F, LPO is selected (1 kHz), and fixed external capacitance of 20 pF. Data is captured with an average of 7 periods window.

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to http://www.freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number			
32-pin QFN	98ARE10566D			

8 Pinout

8.1 K10 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

32 QFN	Pin Name	Default	ALTO	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
1	VDD	VDD	VDD								
2	VSS	VSS	VSS								
3	PTE16	ADC0_SE4a	ADC0_SE4a	PTE16	SPI0_PCS0	UART2_TX	FTM_CLKIN0		FTM0_FLT3		
4	PTE17	ADC0_SE5a	ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	FTM_CLKIN1		LPTMR0_ALT3		
5	PTE18	ADC0_SE6a	ADC0_SE6a	PTE18	SPI0_SOUT	UART2_CTS_b	I2C0_SDA				
6	PTE19	ADC0_SE7a	ADC0_SE7a	PTE19	SPI0_SIN	UART2_RTS_b	I2C0_SCL				
7	VDDA	VDDA	VDDA								
8	VSSA	VSSA	VSSA								
9	XTAL32	XTAL32	XTAL32								
10	EXTAL32	EXTAL32	EXTAL32								
11	VBAT	VBAT	VBAT								
12	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK	TSI0_CH1	PTAO	UART0_CTS_ b/ UART0_COL_b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	EZP_CLK
13	PTA1	JTAG_TDI/ EZP_DI	TSI0_CH2	PTA1	UARTO_RX	FTM0_CH6				JTAG_TDI	EZP_DI

32 QFN	Pin Name	Default	ALTO	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
14	PTA2	JTAG_TDO/ TRACE_SWO/ EZP_DO	TSI0_CH3	PTA2	UART0_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
15	PTA3	JTAG_TMS/ SWD_DIO	TSI0_CH4	PTA3	UARTO_RTS_b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
16	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b	TSI0_CH5	PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
17	PTA18	EXTALO	EXTAL0	PTA18		FTM0_FLT2	FTM_CLKIN0				
18	PTA19	XTAL0	XTAL0	PTA19		FTM1_FLT0	FTM_CLKIN1		LPTMR0_ALT1		
19	RESET_b	RESET_b	RESET_b								
20	PTB0/ LLWU_P5	ADC0_SE8/ TSI0_CH0	ADC0_SE8/ TSI0_CH0	PTB0/ LLWU_P5	I2C0_SCL	FTM1_CH0			FTM1_QD_ PHA		
21	PTB1	ADC0_SE9/ TSI0_CH6	ADC0_SE9/ TSI0_CH6	PTB1	I2C0_SDA	FTM1_CH1			FTM1_QD_ PHB		
22	PTC1/ LLWU_P6	ADC0_SE15/ TSI0_CH14	ADC0_SE15/ TSI0_CH14	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_b	FTM0_CH0		I2S0_TXD0		
23	PTC2	ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	PTC2	SPI0_PCS2	UART1_CTS_b	FTM0_CH1		I2S0_TX_FS		
24	PTC3/ LLWU_P7	CMP1_IN1	CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2		I2S0_TX_BCLK		
25	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT		
26	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ALT2	I2SO_RXDO		CMP0_OUT		
27	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_EXTRG	I2S0_RX_BCLK		I2S0_MCLK		
28	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_SIN		I2S0_RX_FS				
29	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI0_PCS1	UART0_RTS_b	FTM0_CH4		EWM_IN		
30	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI0_PCS2	UART0_CTS_ b/ UART0_COL_b	FTM0_CH5		EWM_OUT_b		
31	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI0_PCS3	UART0_RX	FTM0_CH6		FTM0_FLT0		
32	PTD7	DISABLED		PTD7	CMT_IRO	UART0_TX	FTM0_CH7		FTM0_FLT1		

8.2 K10 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

Revision History



Figure 23. K10 32 QFN Pinout Diagram

9 Revision History

The following table provides a revision history for this document.

Rev. No.	Date	Substantial Changes
2	2/2012	Initial public release
3	4/2012	 Replaced TBDs throughout. Updated "Power mode transition operating behaviors" table. Updated "Power consumption operating behaviors" table. For "Diagram: Typical IDD_RUN operating behavior" section, added "VLPR mode supply current vs. core frequency" figure. Updated "EMC radiated emissions operating behaviors" section. Updated "Thermal operating requirements" section. Updated "MCG specifications" table. Updated "VREF full-range operating behaviors" table. Updated "I2S/SAI Switching Specifications" table. Updated "TSI electrical specifications" table.

Table continues on the next page...

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