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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	-
Number of Macrocells	128
Number of Gates	-
Number of I/O	64
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m4-128n-64-10jc



Product Line	Ordering Part Number	Product Status	Reference PCN
M4-128/64 (Cont'd)	M4-128/64-7VC	Convert to M4A5	Contact pcn@latticesemi.com for more info.
	M4-128/64-10VC		
	M4-128/64-12VC		
	M4-128/64-15VC		
	M4-128/64-10VI		
	M4-128/64-12VI		
	M4-128/64-14VI		
	M4-128/64-18VI		
M4-128N/64	M4-128N/64-7JC	Active / Orderable	
	M4-128N/64-10JC		
	M4-128N/64-12JC		
	M4-128N/64-15JC		
	M4-128N/64-10JI		
	M4-128N/64-12JI		
	M4-128N/64-14JI		
	M4-128N/64-18JI		
M4-192/96	M4-192/96-7VC	Convert to M4A5	Contact pcn@latticesemi.com for more info.
	M4-192/96-10VC		
	M4-192/96-12VC		
	M4-192/96-15VC		
	M4-192/96-10VI		
	M4-192/96-12VI		
	M4-192/96-14VI		
	M4-192/96-18VI		
M4-256/128	M4-256/128-7YC	Convert to M4A5	Contact pcn@latticesemi.com for more info.
	M4-256/128-10YC		
	M4-256/128-12YC		
	M4-256/128-15YC		
	M4-256/128-10YI		
	M4-256/128-12YI		
	M4-256/128-14YI		
	M4-256/128-18YI		
M4LV-32/32	M4LV-32/32-7JC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-32/32-10JC		
	M4LV-32/32-12JC		
	M4LV-32/32-15JC		
	M4LV-32/32-10JI		
	M4LV-32/32-12JI		
	M4LV-32/32-14JI		
	M4LV-32/32-18JI		



Product Line	Ordering Part Number	Product Status	Reference PCN
M4LV-256/128	M4LV-256/128-7YC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-256/128-10YC		
	M4LV-256/128-12YC		
	M4LV-256/128-15YC		
	M4LV-256/128-10YI		
	M4LV-256/128-12YI		
	M4LV-256/128-14YI		
	M4LV-256/128-18YI		
	M4LV-256/128-7AC		
	M4LV-256/128-10AC		
	M4LV-256/128-12AC		
	M4LV-256/128-15AC		
	M4LV-256/128-10AI		
	M4LV-256/128-12AI		
	M4LV-256/128-14AI		
	M4LV-256/128-18AI		

GENERAL DESCRIPTION

The MACH[®] 4 family from Lattice offers an exceptionally flexible architecture and delivers a superior Complex Programmable Logic Device (CPLD) solution of easy-to-use silicon products and software tools. The overall benefits for users are a guaranteed and predictable CPLD solution, faster time-to-market, greater flexibility and lower cost. The MACH 4 devices offer densities ranging from 32 to 256 macrocells with 100% utilization and 100% pin-out retention. The MACH 4 family offer 5-V (M4-xxx) and 3.3-V (M4LV-xxx) operation.

MACH 4 products are 5-V or 3.3-V in-system programmable through the JTAG (IEEE Std. 1149.1) interface. JTAG boundary scan testing also allows product testability on automated test equipment for device connectivity.

All MACH 4 family members deliver First-Time-Fit and easy system integration with pin-out retention after any design change and refit. For both 3.3-V and 5-V operation, MACH 4 products can deliver guaranteed fixed timing as fast as 7.5 ns t_{PD} and 111 MHz f_{CNT} through the SpeedLocking feature when using up to 20 product terms per output (Table 2).

Table 2. MACH 4 Speed Grades

Device	Speed Grade ¹					
	-7	-10	-12	-14	-15	-18
M4-32/32	C	C, I	C, I	I	C	I
M4LV-32/32						
M4-64/32	C	C, I	C, I	I	C	I
M4LV-64/32						
M4-96/48	C	C, I	C, I	I	C	I
M4LV-96/48						
M4-128/64	C	C, I	C, I	I	C	I
M4LV-128/64						
M4-128N/64	C	C, I	C, I	I	C	I
M4LV-128N/64						
M4-192/96	C	C, I	C, I	I	C	I
M4LV-192/96						
M4-256/128	C	C, I	C, I	I	C	I
M4LV-256/128						

Note:

1. C = Commercial, I = Industrial

The MACH 4 family offers numerous density-I/O combinations in Thin Quad Flat Pack (TQFP), Plastic Quad Flat Pack (PQFP), Plastic Leaded Chip Carrier (PLCC), and Ball Grid Array (BGA) packages ranging from 44 to 256 pins (Table 3). It also offers I/O safety features for mixed-voltage designs so that the 3.3-V devices can accept 5-V inputs, and 5-V devices do not overdrive 3.3-V inputs. Additional features include Bus-Friendly inputs and I/Os, a programmable power-down mode for extra power savings and individual output slew rate control for the highest speed transition or for the lowest noise transition.

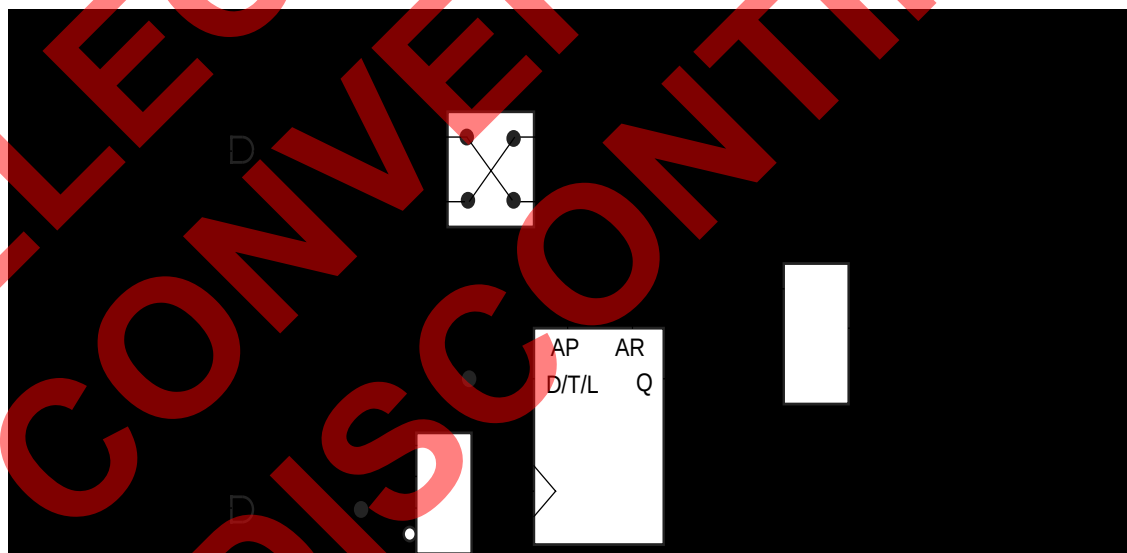


Table 3. MACH 4 Package and I/O Options (Number of I/Os and dedicated inputs in Table)

Package	M4-32/32 M4LV-32/32	M4-64/32 M4LV-64/32	M4-96/48 M4LV-96/48	M4-128/64 M4LV-128/64	M4-128N/64 M4LV-128N/64	M4-192/96 M4LV-192/96	M4LV-256/128
44-pin PLCC	32+2	32+2					
44-pin TQFP	32+2	32+2					
48-pin TQFP	32+2	32+2					
84-pin PLCC					64+6		
100-pin TQFP			48+8	64+6			
100-pin PQFP				64+6			
144-pin TQFP						96+16	
208-pin PQFP							128+14
256-ball BGA							128+14

Macrocell

The macrocell consists of a storage element, routing resources, a clock multiplexer, and initialization control. The macrocell has two fundamental modes: synchronous and asynchronous (Figure 5). The mode chosen only affects clocking and initialization in the macrocell.



b. Asynchronous mode

17466G-010

Figure 5. Macrocell

In either mode, a combinatorial path can be used. For combinatorial logic, the synchronous mode will generally be used, since it provides more product terms in the allocator.

Table 8. Register/Latch Operation

Configuration	Input(s)	CLK/LE ¹	Q+
D-type Register	D=X	0, 1, ↓ (↑)	Q
	D=0	↑ (↓)	0
	D=1	↑ (↓)	1
T-type Register	T=X	0, 1, ↓ (↑)	Q
	T=0	↑ (↓)	$\overline{Q}$
	T=1	↑ (↓)	$\overline{Q}$
D-type Latch	D=X	1 (0)	Q
	D=0	0 (1)	0
	D=1	0 (1)	1

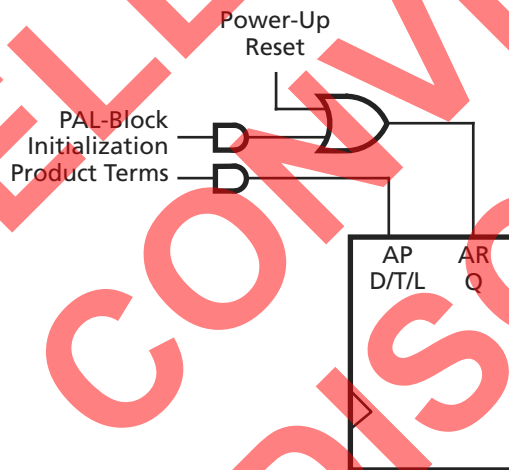
Note:

1. Polarity of CLK/LE can be programmed

Although the macrocell shows only one input to the register, the XOR gate in the logic allocator allows the D-, T-type register to emulate J-K, and S-R behavior. In this case, the available product terms are divided between J and K (or S and R). When configured as J-K, S-R, or T-type, the extra product term must be used on the XOR gate input for flip-flop emulation. In any register type, the polarity of the inputs can be programmed.

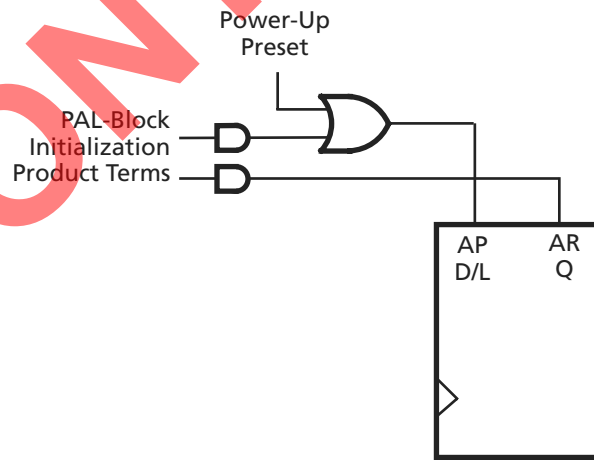
The clock input to the flip-flop can select any of the four PAL block clocks in synchronous mode, with the additional choice of either polarity of an individual product term clock in the asynchronous mode.

The initialization circuit depends on the mode. In synchronous mode (Figure 7), asynchronous reset and preset are provided, each driven by a product term common to the entire PAL block.



a. Power-up reset

17466G-012



b. Power-up preset

17466G-013

Figure 7. Synchronous Mode Initialization Configurations

A reset/preset swapping feature in each macrocell allows for reset and preset to be exchanged, providing flexibility. In asynchronous mode (Figure 8), a single individual product term is provided for initialization. It can be selected to control reset or preset.

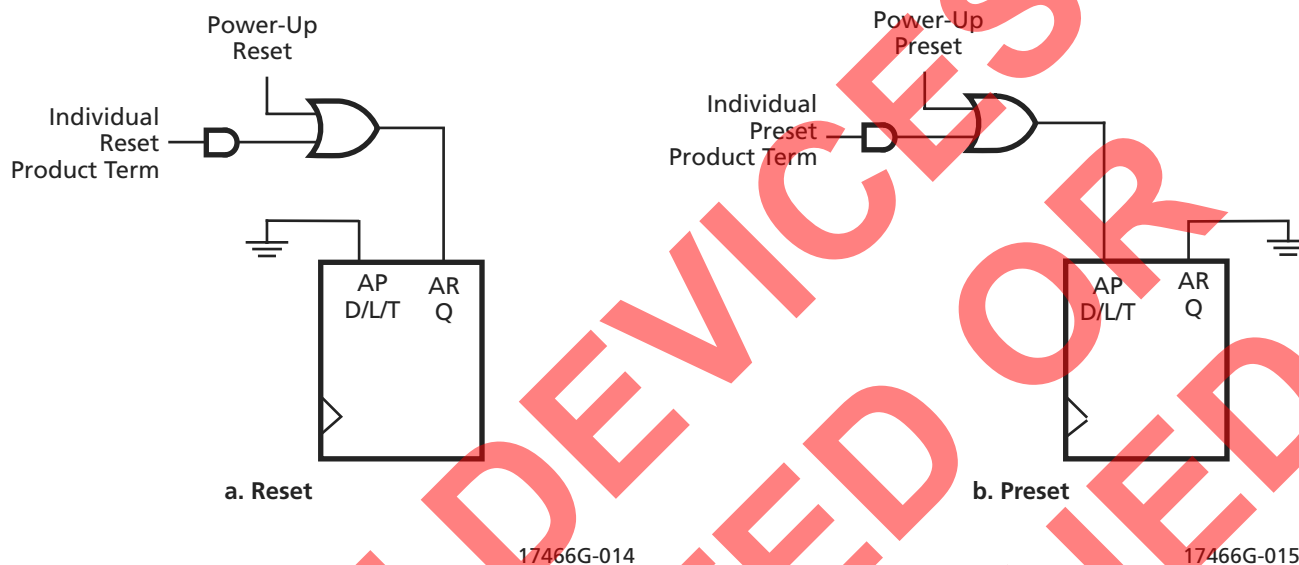


Figure 8. Asynchronous Mode Initialization Configurations

Note that the reset/preset swapping selection feature effects power-up reset as well. The initialization functionality of the flip-flops is illustrated in Table 9. The macrocell sends its data to the output switch matrix and the input switch matrix. The output switch matrix can route this data to an output if so desired. The input switch matrix can send the signal back to the central switch matrix as feedback.

Table 9. Asynchronous Reset/Preset Operation

AR	AP	CLK/LE ¹	Q+
0	0	X	See Table 8
0	1	X	1
1	0	X	0
1	1	X	0

Note:

1. Transparent latch is unaffected by AR, AP

I/O Cell

The I/O cell (Figures 10 and 11) simply consists of a programmable output enable, a feedback path, and flip-flop (except MACH 4 devices with 1:1 macrocell-I/O cell ratio.) An individual output enable product term is provided for each I/O cell. The feedback signal drives the input switch matrix.

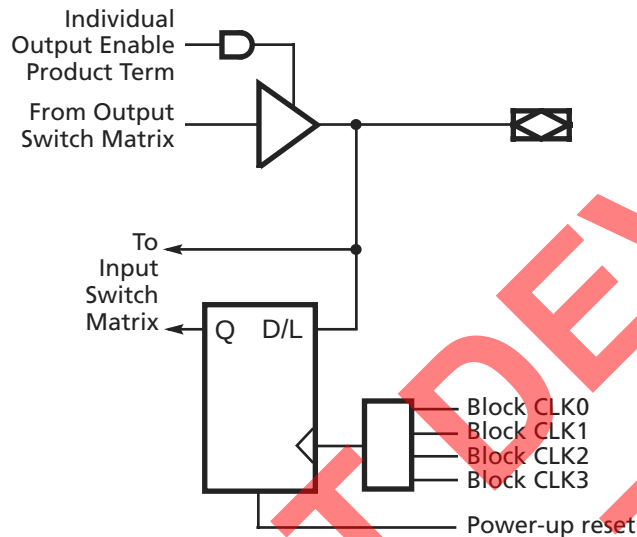


Figure 10. I/O Cell for MACH 4 Devices with 2:1 Macrocell-I/O Cell Ratio

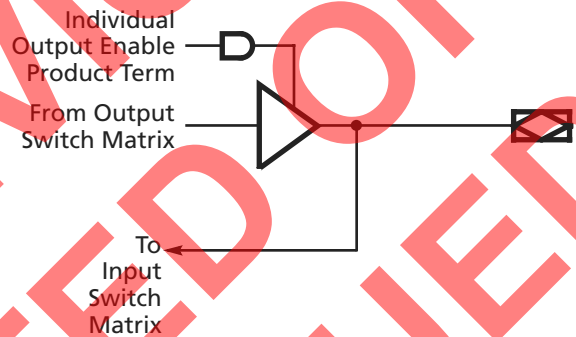


Figure 11. I/O Cell for MACH 4 Devices with 1:1 Macrocell-I/O Cell Ratio

The I/O cell (Figure 10) contains a flip-flop, which provides the capability for storing the input in a D-type register or latch. The clock can be any of the PAL block clocks. Both the direct and registered versions of the input are sent to the input switch matrix. This allows for such functions as “time-domain-multiplexed” data comparison, where the first data value is stored, and then the second data value is put on the I/O pin and compared with the previous stored value.

Note that the flip-flop used in the MACH 4 I/O cell is independent of the flip-flops in the macrocells. It powers up to a logic low.

Zero-Hold-Time Input Register

The MACH 4 devices have a zero-hold-time (ZHT) fuse which controls the time delay associated with loading data into all I/O cell registers and latches. When programmed, the ZHT fuse increases the data path setup delays to input storage elements, matching equivalent delays in the clock path. When the fuse is erased, the setup time to the input storage element is minimized. This feature facilitates doing worst-case designs for which data is loaded from sources which have low (or zero) minimum output propagation delays from clock edges.

Input Switch Matrix

The input switch matrix (Figures 12 and 13) optimizes routing of inputs to the central switch matrix. Without the input switch matrix, each input and feedback signal has only one way to enter the central switch matrix. The input switch matrix provides additional ways for these signals to enter the central switch matrix.



Table 12. PAL Block Clock Combinations¹

Block CLK0	Block CLK1	Block CLK2	Block CLK3
$\overline{\text{GCLK0}}$	$\overline{\text{GCLK1}}$	X	X
$\overline{\text{GCLK1}}$	$\overline{\text{GCLK1}}$	X	X
$\overline{\text{GCLK0}}$	$\overline{\text{GCLK0}}$	X	X
$\overline{\text{GCLK1}}$	$\overline{\text{GCLK0}}$	X	X
X	X	$\overline{\text{GCLK2}} (\text{GCLK0})$	$\overline{\text{GCLK3}} (\text{GCLK1})$
X	X	$\overline{\text{GCLK3}} (\text{GCLK1})$	$\overline{\text{GCLK3}} (\text{GCLK1})$
X	X	$\overline{\text{GCLK2}} (\text{GCLK0})$	$\overline{\text{GCLK2}} (\text{GCLK0})$
X	X	$\overline{\text{GCLK3}} (\text{GCLK1})$	$\overline{\text{GCLK2}} (\text{GCLK0})$

Note:

1. Values in parentheses are for the M4(LV)-32/32 and M4(LV)-64/32.

This feature provides high flexibility for partitioning state machines and dual-phase clocks. It also allows latches to be driven with either polarity of latch enable, and in a master-slave configuration.

MACH 4 TIMING MODEL

The primary focus of the MACH 4 timing model is to accurately represent the timing in a MACH 4 device, and at the same time, be easy to understand. This model accurately describes all combinatorial and registered paths through the device, making a distinction between internal feedback and external feedback. A signal uses internal feedback when it is fed back into the switch matrix or block without having to go through the output buffer. The input register specifications are also reported as internal feedback. When a signal is fed back into the switch matrix after having gone through the output buffer, it is using external feedback.

The parameter, t_{BUF} , is defined as the time it takes to go from feedback through the output buffer to the I/O pad. If a signal goes to the internal feedback rather than to the I/O pad, the parameter designator is followed by an "i". By adding t_{BUF} to this internal parameter, the external parameter is derived. For example, $t_{PD} = t_{PDi} + t_{BUF}$. A diagram representing the modularized MACH 4 timing model is shown in Figure 15. Refer to the Technical Note entitled *MACH 4 Timing and High Speed Design* for a more detailed discussion about the timing parameters.



17466G-025

Figure 15. MACH 4 Timing Model

SPEEDLOCKING FOR GUARANTEED FIXED TIMING

The MACH 4 architecture allows allocation of up to 20 product terms to an individual macrocell with the assistance of an XOR gate without incurring additional timing delays.

The design of the switch matrix and PAL blocks guarantee a fixed pin-to-pin delay that is independent of the logic required by the design. Other competitive CPLDs incur serious timing delays as product terms expand beyond their typical 4 or 5 product term limits. Speed and SpeedLocking combine to give designs easy access to the performance required in today's designs.

POWER MANAGEMENT

Each individual PAL block in MACH 4 devices features a programmable low-power mode, which results in power savings of up to 50%. The signal speed paths in the low-power PAL block will be slower than those in the non-low-power PAL block. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in the low-power mode.

PROGRAMMABLE SLEW RATE

Each MACH 4 device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3 V/ns) or for the lower noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

POWER-UP RESET/SET

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

SECURITY BIT

A programmable security bit is provided on the MACH 4 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

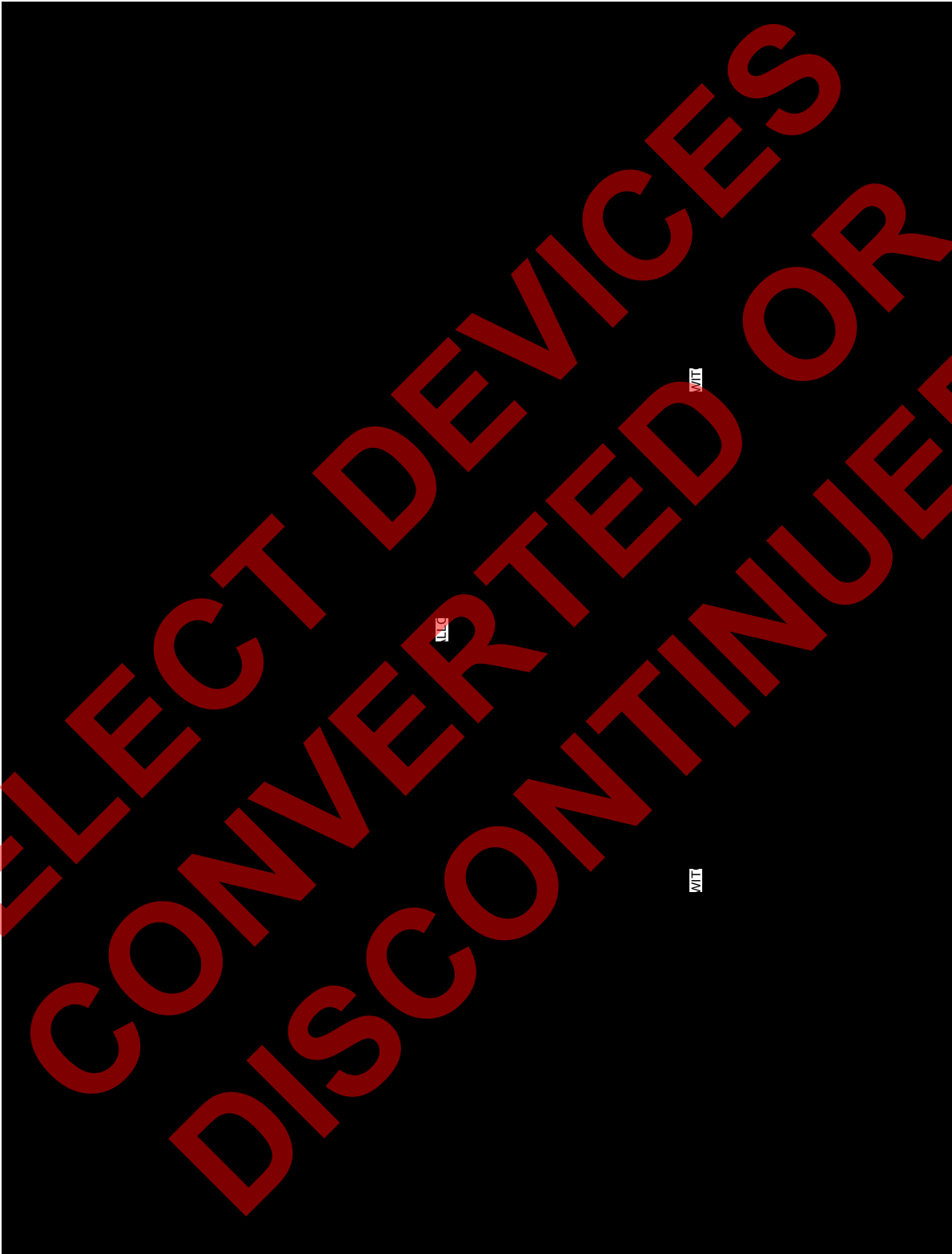
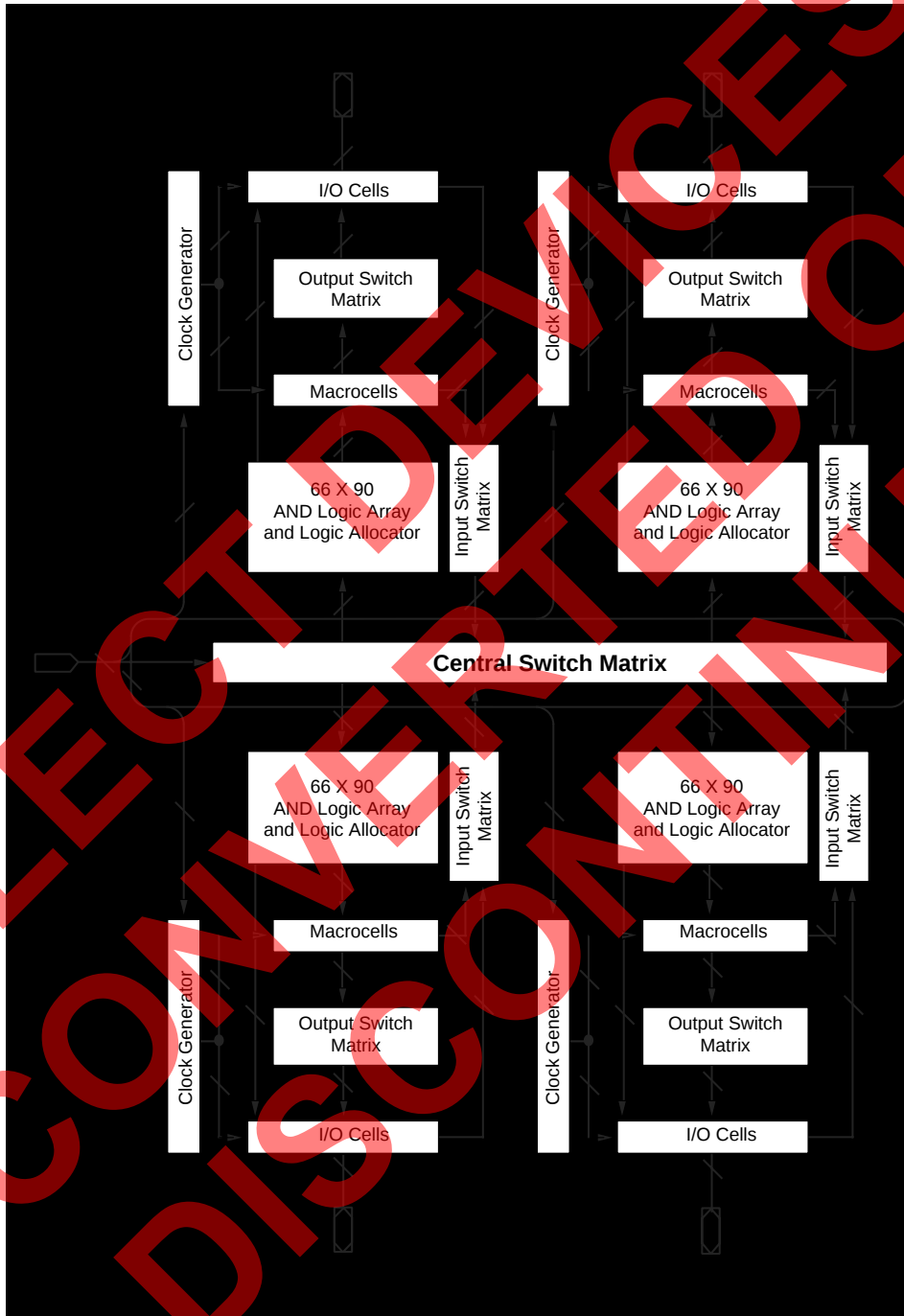


Figure 17. PAL Block for M4(LV)-32/32

17466H-042

BLOCK DIAGRAM – M4(LV)-64/32



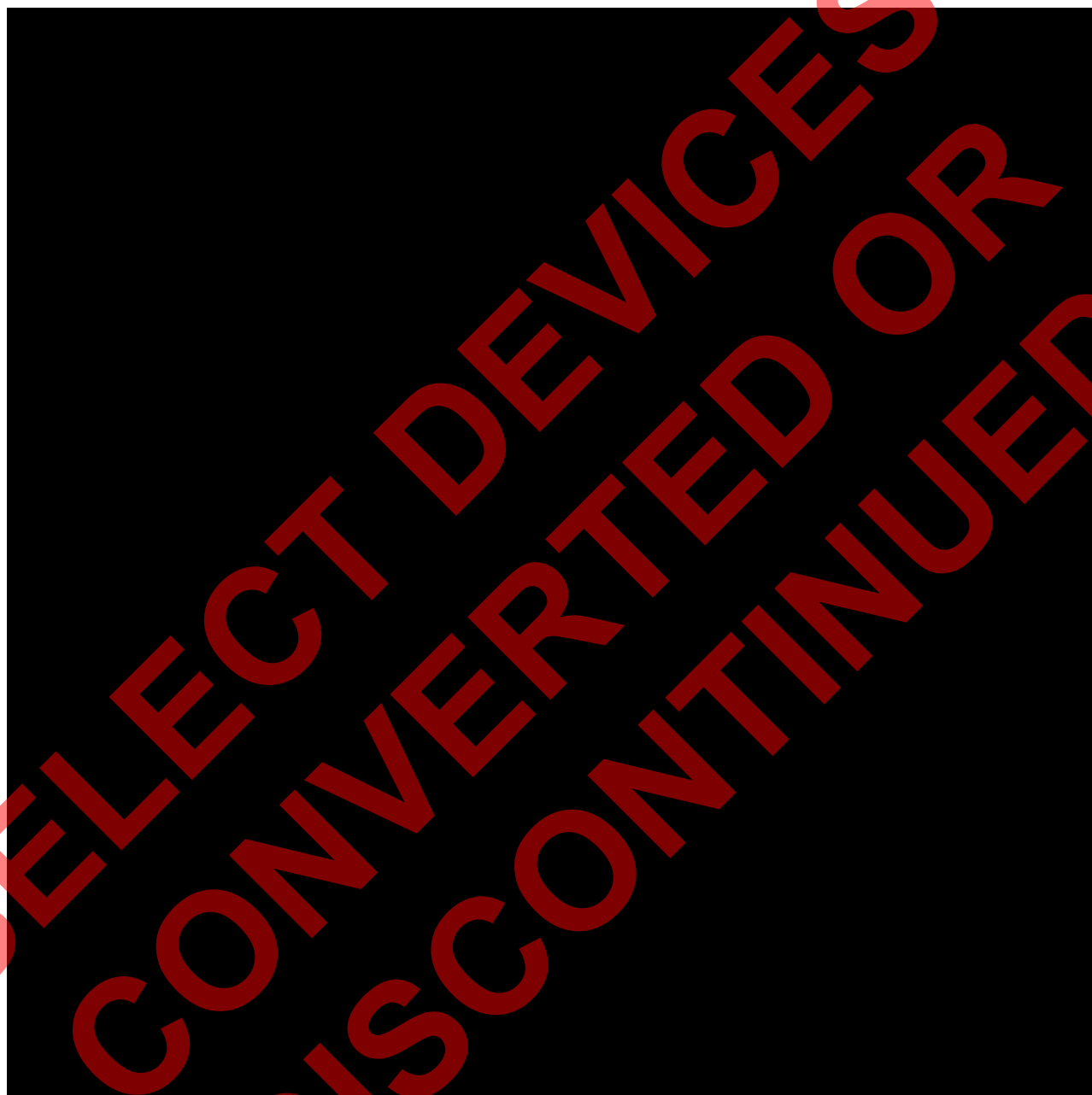
17466H-020

BLOCK DIAGRAM – M4(LV)-128N/64 AND M4(LV)-128/64



17466H-022

BLOCK DIAGRAM – M4(LV)-192/96



17466G-067

ABSOLUTE MAXIMUM RATINGS

M4

Storage Temperature -65°C to +150°C
 Ambient Temperature
 with Power Applied -55°C to +100°C
 Device Junction Temperature +130°C
 Supply Voltage
 with Respect to Ground -0.5 V to +7.0 V
 DC Input Voltage -0.5 V to $V_{CC} + 0.5$ V
 Static Discharge Voltage 2000 V
 Latchup Current ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$) 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
 Operating in Free Air 0°C to +70°C
 Supply Voltage (V_{CC})
 with Respect to Ground +4.75 V to +5.25 V

Industrial (I) Devices

Ambient Temperature (T_A)
 Operating in Free Air -40°C to +85°C
 Supply Voltage (V_{CC})
 with Respect to Ground +4.50 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

5-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -3.2$ mA, $V_{CC} = \text{Min}$, $V_{IN} = V_{IH}$ or V_{IL}	2.4			V
		$I_{OH} = 0$ mA, $V_{CC} = \text{Max}$, $V_{IN} = V_{IH}$ or V_{IL}			3.3	V
V_{OL}	Output LOW Voltage	$I_{OL} = 24$ mA, $V_{CC} = \text{Min}$, $V_{IN} = V_{IH}$ or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	$V_{IN} = 5.25$ V, $V_{CC} = \text{Max}$ (Note 3)			10	μA
I_{IL}	Input LOW Leakage Current	$V_{IN} = 0$ V, $V_{CC} = \text{Max}$ (Note 3)			-10	μA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 5.25$ V, $V_{CC} = \text{Max}$, $V_{IN} = V_{IH}$ or V_{IL} (Note 3)			10	μA
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = 0$ V, $V_{CC} = \text{Max}$, $V_{IN} = V_{IH}$ or V_{IL} (Note 3)			-10	μA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max}$ (Note 4)	-30		-160	mA

Notes:

1. Total I_{OL} for one PAL block should not exceed 64 mA.
2. These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.
3. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
4. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
 $V_{OUT} = 0.5$ V has been chosen to avoid test problems caused by tester ground degradation.

ABSOLUTE MAXIMUM RATINGS

M4LV

Storage Temperature -65°C to +150°C
 Ambient Temperature
 with Power Applied -55°C to +100°C
 Device Junction Temperature +130°C
 Supply Voltage
 with Respect to Ground -0.5 V to +4.5 V
 DC Input Voltage -0.5 V to 6.0 V
 Static Discharge Voltage 2000 V
 Latchup Current ($T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$) 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
 Operating in Free Air 0°C to +70°C
 Supply Voltage (V_{CC})
 with Respect to Ground +3.0 V to +3.6 V

Industrial (I) Devices

Ambient Temperature (T_A)
 Operating in Free Air -40°C to +85°C
 Supply Voltage (V_{CC})
 with Respect to Ground +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

3.3-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -100\ \mu\text{A}$	$V_{CC} - 0.2$		V
			$I_{OH} = -3.2\ \text{mA}$	2.4		V
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 1)	$I_{OL} = 100\ \mu\text{A}$		0.2	V
			$I_{OL} = 24\ \text{mA}$		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs	2.0		5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs	-0.3		0.8	V
I_{IH}	Input HIGH Leakage Current	$V_{IN} = 3.6\ \text{V}$, $V_{CC} = \text{Max}$ (Note 2)			5	μA
I_{IL}	Input LOW Leakage Current	$V_{IN} = 0\ \text{V}$, $V_{CC} = \text{Max}$ (Note 2)			-5	μA
I_{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 3.6\ \text{V}$, $V_{CC} = \text{Max}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 2)			5	μA
I_{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = 0\ \text{V}$, $V_{CC} = \text{Max}$ $V_{IN} = V_{IH}$ or V_{IL} (Note 2)			-5	μA
I_{SC}	Output Short-Circuit Current	$V_{OUT} = 0.5\ \text{V}$, $V_{CC} = \text{Max}$ (Note 3)	-15		-160	mA

Notes:

1. Total I_{OL} for one PAL block should not exceed 64 mA.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

44-PIN TQFP CONNECTION DIAGRAM (M4(LV)-32/32 AND M4(LV)-64/32)

Top View

44-Pin TQFP



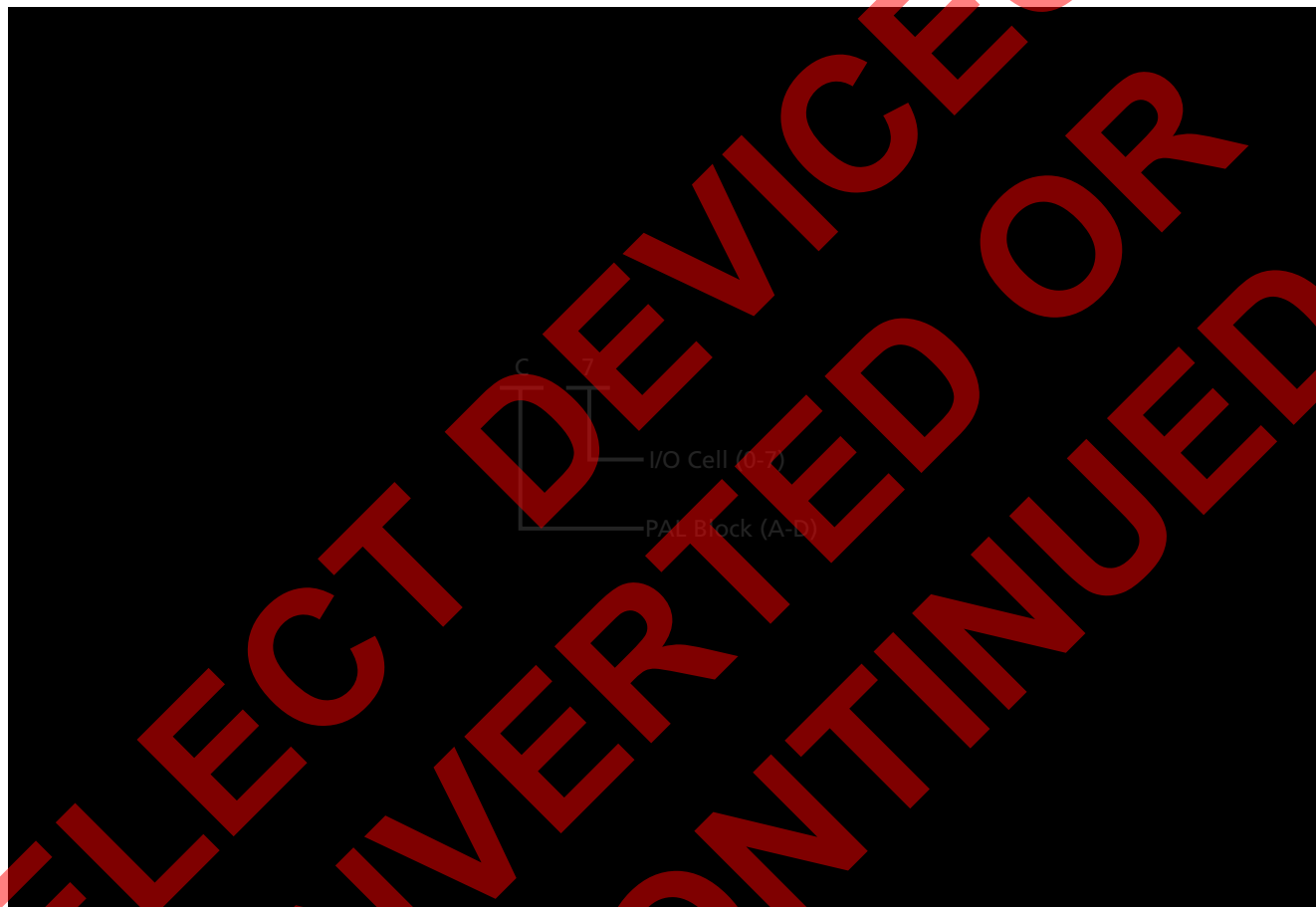
PIN DESIGNATIONS

CLK/I	=	Clock or Input
GND	=	Ground
I/O	=	Input/Output
V _{CC}	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out

48-PIN TQFP CONNECTION DIAGRAM (M4(LV)-32/32 AND M4(LV)-64/32)

Top View

48-Pin TQFP



17466G-028

PIN DESIGNATIONS

CLK/I	=	Clock or Input
GND	=	Ground
I/O	=	Input/Output
V _{CC}	=	Supply Voltage
NC	=	No Connect
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out

144-PIN TQFP CONNECTION DIAGRAM (M4(LV)-192/96)

Top View

144-Pin TQFP



17466G-033

PIN DESIGNATIONS

- CLK = Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- V_{CC} = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out

17466G-044