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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	10 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	128
Number of Gates	-
Number of I/O	64
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m4-128n-64-10ji



Product Line	Ordering Part Number	Product Status	Reference PCN
M4LV-256/128	M4LV-256/128-7YC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-256/128-10YC		
	M4LV-256/128-12YC		
	M4LV-256/128-15YC		
	M4LV-256/128-10YI		
	M4LV-256/128-12YI		
	M4LV-256/128-14YI		
	M4LV-256/128-18YI		
	M4LV-256/128-7AC		
	M4LV-256/128-10AC		
	M4LV-256/128-12AC		
	M4LV-256/128-15AC		
	M4LV-256/128-10AI		
	M4LV-256/128-12AI		
	M4LV-256/128-14AI		
	M4LV-256/128-18AI		

GENERAL DESCRIPTION

The MACH[®] 4 family from Lattice offers an exceptionally flexible architecture and delivers a superior Complex Programmable Logic Device (CPLD) solution of easy-to-use silicon products and software tools. The overall benefits for users are a guaranteed and predictable CPLD solution, faster time-to-market, greater flexibility and lower cost. The MACH 4 devices offer densities ranging from 32 to 256 macrocells with 100% utilization and 100% pin-out retention. The MACH 4 family offer 5-V (M4-xxx) and 3.3-V (M4LV-xxx) operation.

MACH 4 products are 5-V or 3.3-V in-system programmable through the JTAG (IEEE Std. 1149.1) interface. JTAG boundary scan testing also allows product testability on automated test equipment for device connectivity.

All MACH 4 family members deliver First-Time-Fit and easy system integration with pin-out retention after any design change and refit. For both 3.3-V and 5-V operation, MACH 4 products can deliver guaranteed fixed timing as fast as 7.5 ns t_{PD} and 111 MHz f_{CNT} through the SpeedLocking feature when using up to 20 product terms per output (Table 2).

Table 2. MACH 4 Speed Grades

Device	Speed Grade ¹					
	-7	-10	-12	-14	-15	-18
M4-32/32	C	C, I	C, I	I	C	I
M4LV-32/32						
M4-64/32	C	C, I	C, I	I	C	I
M4LV-64/32						
M4-96/48	C	C, I	C, I	I	C	I
M4LV-96/48						
M4-128/64	C	C, I	C, I	I	C	I
M4LV-128/64						
M4-128N/64	C	C, I	C, I	I	C	I
M4LV-128N/64						
M4-192/96	C	C, I	C, I	I	C	I
M4LV-192/96						
M4-256/128	C	C, I	C, I	I	C	I
M4LV-256/128						

Note:

1. C = Commercial, I = Industrial

The MACH 4 family offers numerous density-I/O combinations in Thin Quad Flat Pack (TQFP), Plastic Quad Flat Pack (PQFP), Plastic Leaded Chip Carrier (PLCC), and Ball Grid Array (BGA) packages ranging from 44 to 256 pins (Table 3). It also offers I/O safety features for mixed-voltage designs so that the 3.3-V devices can accept 5-V inputs, and 5-V devices do not overdrive 3.3-V inputs. Additional features include Bus-Friendly inputs and I/Os, a programmable power-down mode for extra power savings and individual output slew rate control for the highest speed transition or for the lowest noise transition.

Table 4. Architectural Summary of MACH 4 devices

	MACH 4 Devices	
	M4-64/32, M4LV-64/32 M4-96/48, M4LV-96/48 M4-128/64, M4LV-128/64 M4-128N/64, M4LV-128N/64 M4-192/96, M4LV-192/96 M4-256/128, M4LV-256/128	M4-32/32 M4LV-32/32
Macrocell-I/O Cell Ratio	2:1	1:1
Input Switch Matrix	Yes	Yes
Input Registers	Yes	No
Central Switch Matrix	Yes	Yes
Output Switch Matrix	Yes	Yes

The Macrocell-I/O cell ratio is defined as the number of macrocells versus the number of I/O cells internally in a PAL block (Table 4).

The central switch matrix takes all dedicated inputs and signals from the input switch matrices and routes them as needed to the PAL blocks. Feedback signals that return to the same PAL block still must go through the central switch matrix. This mechanism ensures that PAL blocks in MACH 4 devices communicate with each other with consistent, predictable delays.

The central switch matrix makes a MACH 4 device more advanced than simply several PAL devices on a single chip. It allows the designer to think of the device not as a collection of blocks, but as a single programmable device; the software partitions the design into PAL blocks through the central switch matrix so that the designer does not have to be concerned with the internal architecture of the device.

Each PAL block consists of:

- ◆ Product-term array
- ◆ Logic allocator
- ◆ Macrocells
- ◆ Output switch matrix
- ◆ I/O cells
- ◆ Input switch matrix
- ◆ Clock generator

Table 6. Logic Allocator for All MACH 4 Devices (except M4(LV)-32/32)

Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M ₀	C ₀ , C ₁ , C ₂	M ₈	C ₇ , C ₈ , C ₉ , C ₁₀
M ₁	C ₀ , C ₁ , C ₂ , C ₃	M ₉	C ₈ , C ₉ , C ₁₀ , C ₁₁
M ₂	C ₁ , C ₂ , C ₃ , C ₄	M ₁₀	C ₉ , C ₁₀ , C ₁₁ , C ₁₂
M ₃	C ₂ , C ₃ , C ₄ , C ₅	M ₁₁	C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃
M ₄	C ₃ , C ₄ , C ₅ , C ₆	M ₁₂	C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄
M ₅	C ₄ , C ₅ , C ₆ , C ₇	M ₁₃	C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₆	C ₅ , C ₆ , C ₇ , C ₈	M ₁₄	C ₁₃ , C ₁₄ , C ₁₅
M ₇	C ₆ , C ₇ , C ₈ , C ₉	M ₁₅	C ₁₄ , C ₁₅

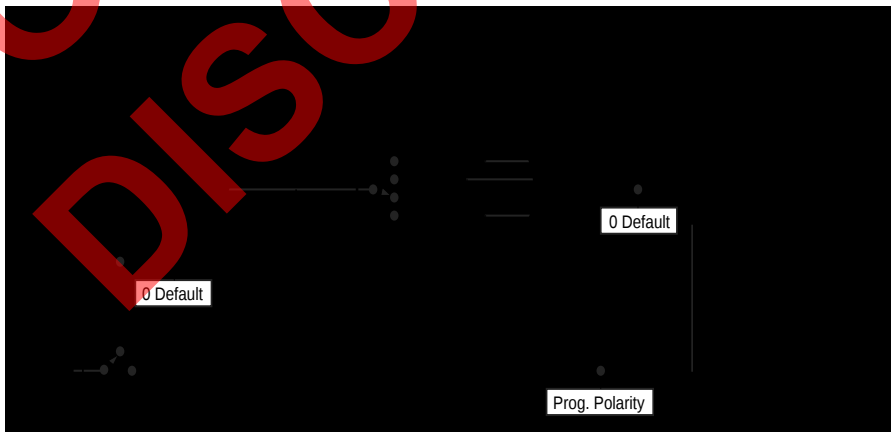
Table 7. Logic Allocator for M4(LV)-32/32

Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M ₀	C ₀ , C ₁ , C ₂	M ₈	C ₈ , C ₉ , C ₁₀
M ₁	C ₀ , C ₁ , C ₂ , C ₃	M ₉	C ₈ , C ₉ , C ₁₀ , C ₁₁
M ₂	C ₁ , C ₂ , C ₃ , C ₄	M ₁₀	C ₉ , C ₁₀ , C ₁₁ , C ₁₂
M ₃	C ₂ , C ₃ , C ₄ , C ₅	M ₁₁	C ₁₀ , C ₁₁ , C ₁₂ , C ₁₃
M ₄	C ₃ , C ₄ , C ₅ , C ₆	M ₁₂	C ₁₁ , C ₁₂ , C ₁₃ , C ₁₄
M ₅	C ₄ , C ₅ , C ₆ , C ₇	M ₁₃	C ₁₂ , C ₁₃ , C ₁₄ , C ₁₅
M ₆	C ₅ , C ₆ , C ₇	M ₁₄	C ₁₃ , C ₁₄ , C ₁₅
M ₇	C ₆ , C ₇	M ₁₅	C ₁₄ , C ₁₅



a. Synchronous Mode

17466G-005



b. Asynchronous Mode

17466G-006

Figure 2. Logic Allocator: Configuration of Cluster "n" Set by Mode of Macrocell "n"

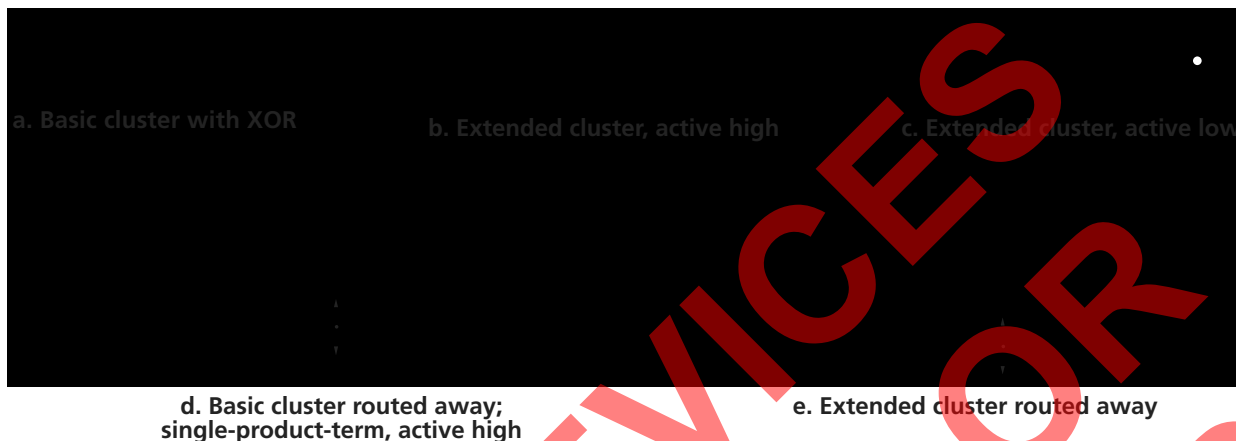


Figure 3. Logic Allocator Configurations: Synchronous Mode

17466G-007



Figure 4. Logic Allocator Configurations: Asynchronous Mode

17466G-008

Note that the configuration of the logic allocator has absolutely no impact on the speed of the signal. All configurations have the same delay. This means that designers do not have to decide between optimizing resources or speed; both can be optimized.

If not used in the cluster, the extra product term can act in conjunction with the basic cluster to provide XOR logic for such functions as data comparison, or it can work with the D-,T-type flip-flop to provide for J-K, and S-R register operation. In addition, if the basic cluster is routed to another macrocell, the extra product term is still available for logic. In this case, the first XOR input will be a logic 0. This circuit has the flexibility to route product terms elsewhere without giving up the use of the macrocell.

Product term clusters do not “wrap” around a PAL block. This means that the macrocells at the ends of the block have fewer product terms available.

The flip-flop can be configured as a D-type or T-type latch. J-K or S-R registers can be synthesized. The primary flip-flop configurations are shown in Figure 6, although others are possible. Flip-flop functionality is defined in Table 8. Note that a J-K latch is inadvisable as it will cause oscillation if both J and K inputs are HIGH.



Figure 6. Primary Macrocell Configurations

17466G-011

Table 10. Output Switch Matrix Combinations for MACH 4 Devices with 2:1 Macrocell-I/O Cell Ratio

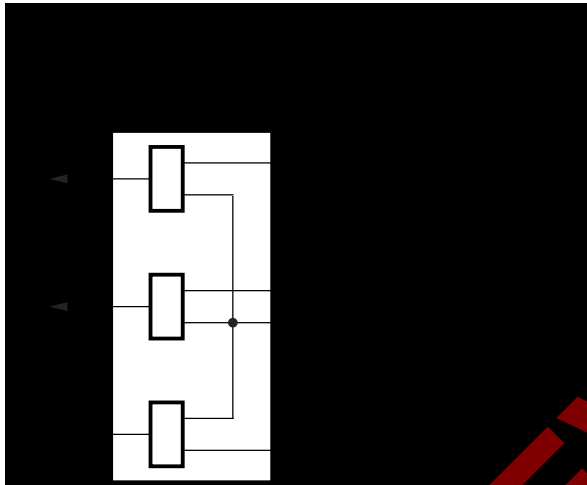
Macrocell	Routable to I/O Cells
M0, M1	I/O0, I/O5, I/O6, I/O7
M2, M3	I/O0, I/O1, I/O6, I/O7
M4, M5	I/O0, I/O1, I/O2, I/O7
M6, M7	I/O0, I/O1, I/O2, I/O3
M8, M9	I/O1, I/O2, I/O3, I/O4
M10, M11	I/O2, I/O3, I/O4, I/O5
M12, M13	I/O3, I/O4, I/O5, I/O6
M14, M15	I/O4, I/O5, I/O6, I/O7

I/O Cell	Available Macrocells
I/O0	M0, M1, M2, M3, M4, M5, M6, M7
I/O1	M2, M3, M4, M5, M6, M7, M8, M9
I/O2	M4, M5, M6, M7, M8, M9, M10, M11
I/O3	M6, M7, M8, M9, M10, M11, M12, M13
I/O4	M8, M9, M10, M11, M12, M13, M14, M15
I/O5	M0, M1, M10, M11, M12, M13, M14, M15
I/O6	M0, M1, M2, M3, M12, M13, M14, M15
I/O7	M0, M1, M2, M3, M4, M5, M14, M15

Table 11. Output Switch Matrix Combinations for M4(LV)-32/32

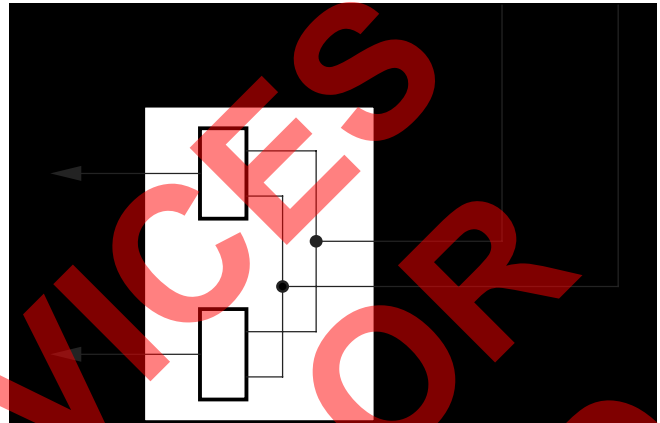
Macrocell	Routable to I/O Cells
M0, M1, M2, M3, M4, M5, M6, M7	I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7
M8, M9, M10, M11, M12, M13, M14, M15	I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15

I/O Cell	Available Macrocells
I/O0, I/O1, I/O2, I/O3, I/O4, I/O5, I/O6, I/O7	M0, M1, M2, M3, M4, M5, M6, M7
I/O8, I/O9, I/O10, I/O11, I/O12, I/O13, I/O14, I/O15	M8, M9, M10, M11, M12, M13, M14, M15



17466G-002

Figure 12. MACH 4 with 2:1 Macrocell-I/O Cell Ratio - Input Switch Matrix



17466G-003

Figure 13. MACH 4 with 1:1 Macrocell-I/O Cell Ratio - Input Switch Matrix

PAL Block Clock Generation

Each MACH 4 device has four clock pins that can also be used as inputs. These pins drive a clock generator in each PAL block (Figure 14). The clock generator provides four clock signals that can be used anywhere in the PAL block. These four PAL block clock signals can consist of a large number of combinations of the true and complement edges of the global clock signals. Table 12 lists the possible combinations.



17466G-004

Figure 14. PAL Block Clock Generator ¹

Note:

1. M4(LV)-32/32 and M4(LV)-64/32 have only two clock pins, GCLK0 and GCLK1. GCLK2 is tied to GCLK0, and GCLK3 is tied to GCLK1.

IEEE 1149.1-COMPLIANT BOUNDARY SCAN TESTABILITY

All MACH 4 devices, except the M4(LV)-128N/64, have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more complete board-level testing.

IEEE 1149.1-COMPLIANT IN-SYSTEM PROGRAMMING

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality, and the ability to make in-field modifications. All MACH 4 devices provide In-System Programming (ISP) capability through their Boundary ScanTest Access Ports. This capability has been implemented in a manner that ensures that the port remains compliant to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

MACH 4 devices can be programmed across the commercial temperature and voltage range. The PC-based LatticePRO software facilitates in-system programming of MACH 4 devices. LatticePRO takes the JEDEC file output produced by the design implementation software, along with information about the JTAG chain, and creates a set of vectors that are used to drive the JTAG chain. LatticePRO software can use these vectors to drive a JTAG chain via the parallel port of a PC. Alternatively, LatticePRO software can output files in formats understood by common automated test equipment. This equipment can then be used to program MACH 4 devices during the testing of a circuit board.

PCI COMPLIANT

MACH 4 devices in the -7/-10/-12 speed grades are compliant with the *PCI Local Bus Specification* version 2.1, published by the PCI Special Interest Group (SIG). The 5-V devices are fully PCI-compliant. The 3.3-V devices are mostly compliant but do not meet the PCI condition to clamp the inputs as they rise above V_{CC} because of their 5-V input tolerant feature.

SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS

Both the 3.3-V and 5-V V_{CC} MACH 4 devices are safe for mixed supply voltage system designs. The 5-V devices will not overdrive 3.3-V devices above the output voltage of 3.3 V, while they accept inputs from other 3.3-V devices. The 3.3-V device will accept inputs up to 5.5 V. Both the 5-V and 3.3-V versions have the same high-speed performance and provide easy-to-use mixed-voltage design capability.

BUS-FRIENDLY INPUTS AND I/OS

All MACH 4 devices have inputs and I/Os which feature the Bus-Friendly circuitry incorporating two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state. While it is good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from the input threshold voltage where noise can cause high-frequency switching. At power-up, the Bus-Friendly latches are reset to a logic level "1." For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice/Vantis Data Book CD-ROM or Lattice web site.

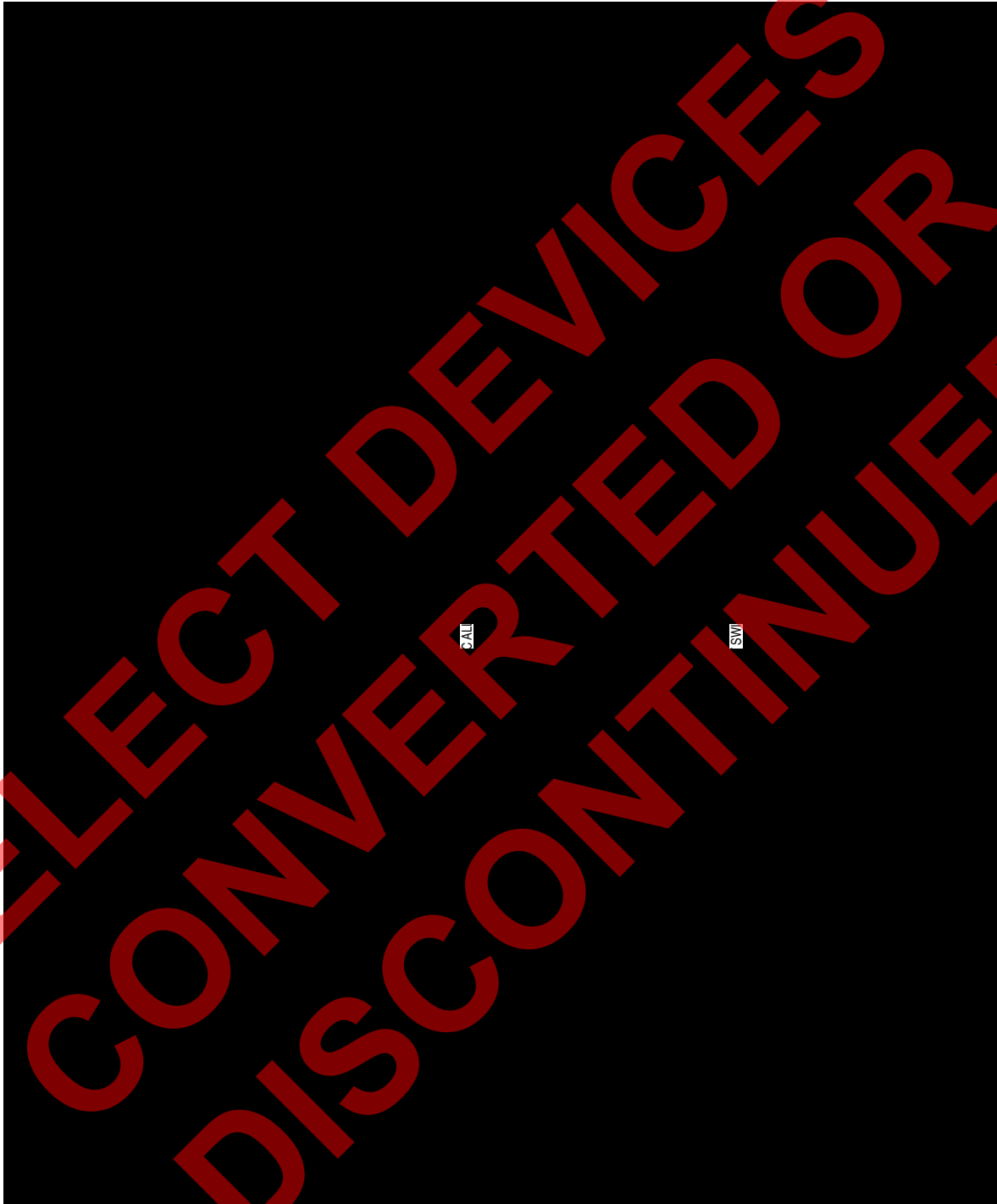
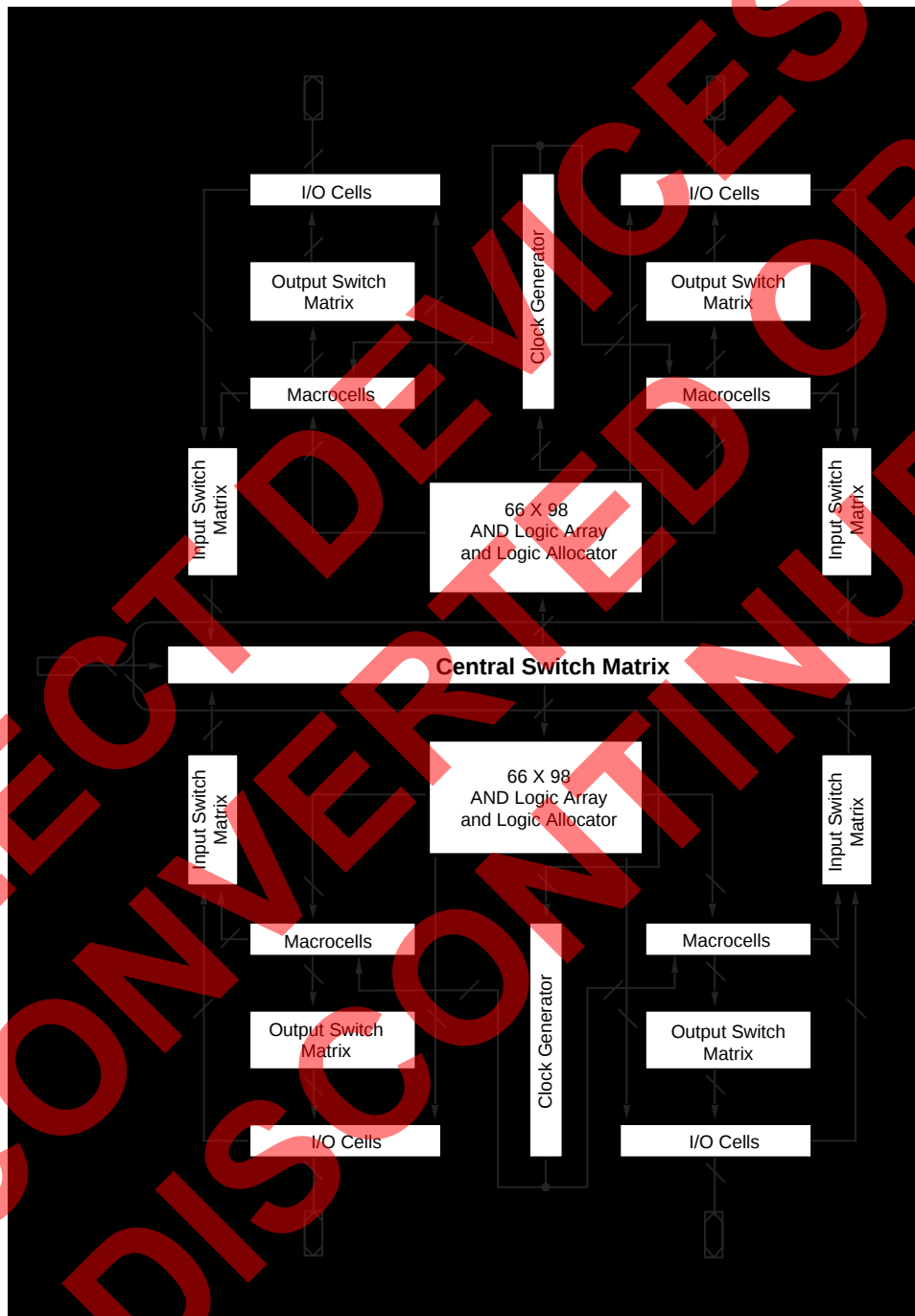


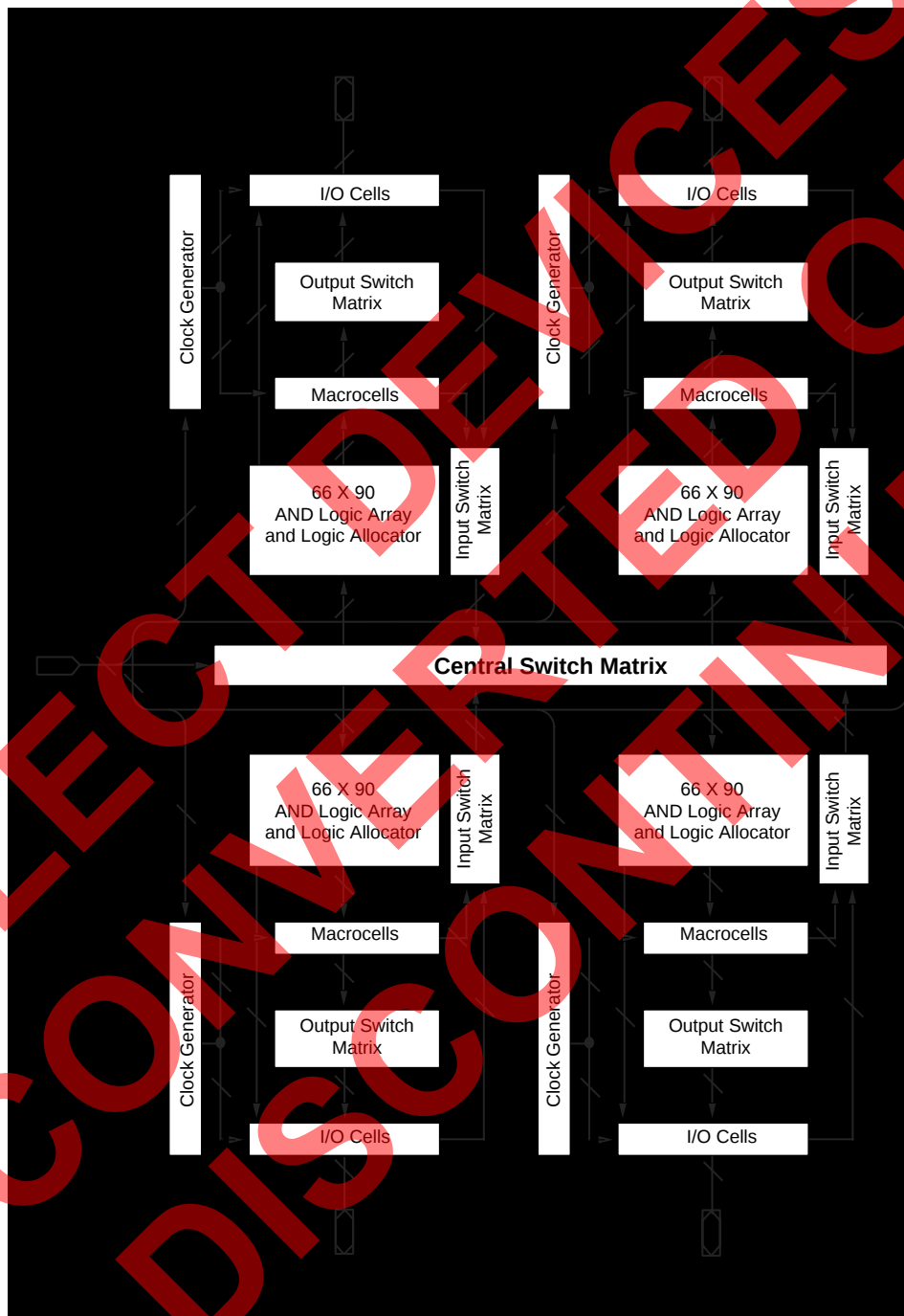
Figure 16. PAL Block for MACH 4 with 2:1 Macrocell - I/O Cell Ratio

BLOCK DIAGRAM – M4(LV)-32/32



17466H-019

BLOCK DIAGRAM – M4(LV)-64/32



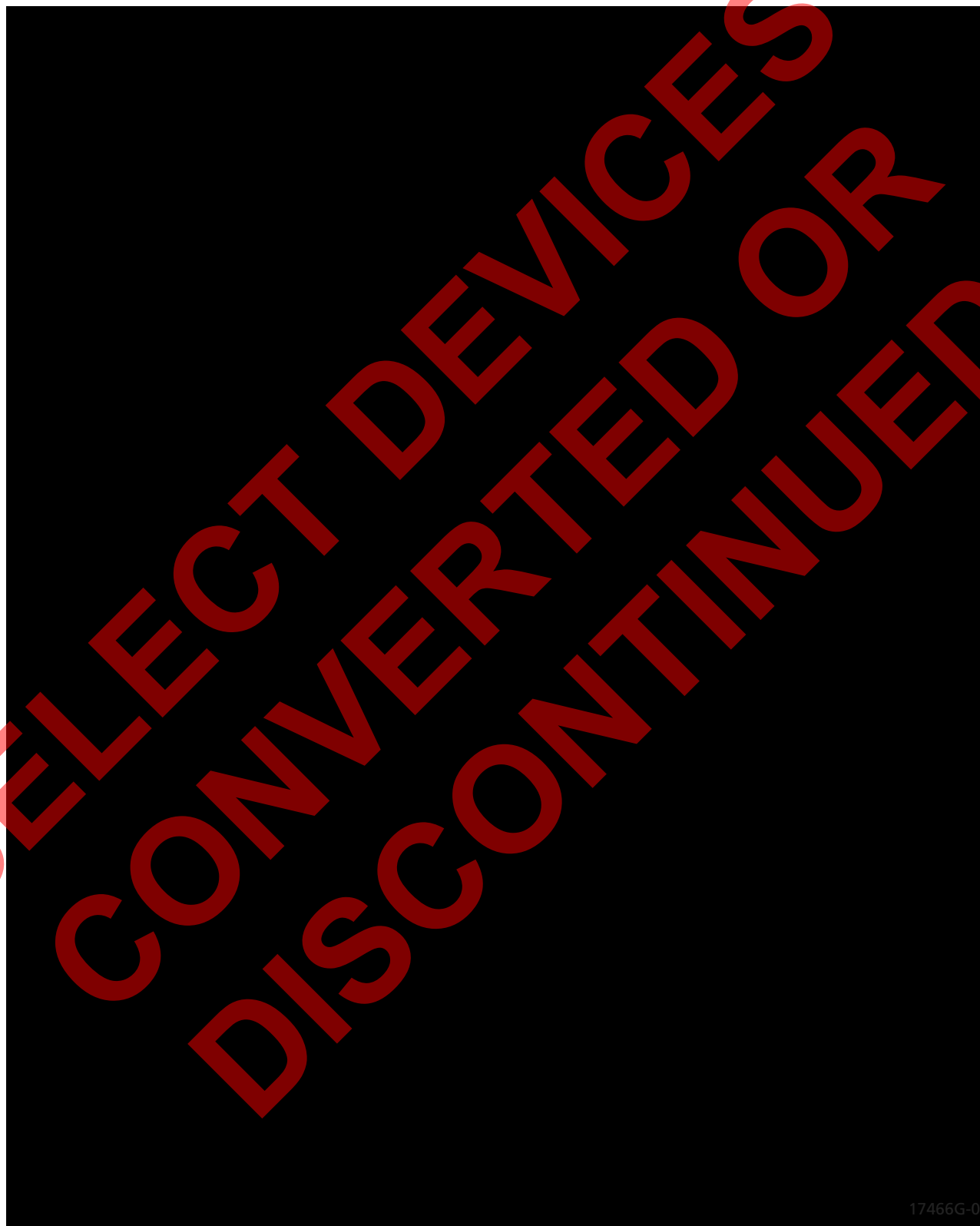
17466H-020

BLOCK DIAGRAM – M4(LV)-128N/64 AND M4(LV)-128/64



17466H-022

BLOCK DIAGRAM – M4(LV)-256/128



MACH 4 TIMING PARAMETERS OVER OPERATING RANGES¹ (CONTINUED)

		-7		-10		-12		-14		-15		-18		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Input Latch Delays with ZHT Option:														
t _{SILZ}	Input latch setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0		ns
t _{HILZ}	Input latch hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0		ns
t _{PDILZi}	Transparent input latch to internal feedback - ZHT		6.0		6.0		6.0		6.0		6.0		6.0	ns
Output Delays:														
t _{BUF}	Output buffer delay		2.0		2.0		2.0		2.0		2.0		2.0	ns
t _{SLW}	Slow slew rate delay adder		2.5		2.5		2.5		2.5		2.5		2.5	ns
t _{EA}	Output enable time		9.5		10.0		12.0		15.0		15.0		17.0	ns
t _{ER}	Output disable time		9.5		10.0		12.0		15.0		15.0		17.0	ns
Power Delay:														
t _{PL}	Power-down mode delay adder		2.5		2.5		2.5		2.5		2.5		2.5	ns
Reset and Preset Delays:														
t _{SRi}	Asynchronous reset or preset to internal register output		10.0		12.0		14.0		18.0		18.0		20.0	ns
t _{SR}	Asynchronous reset or preset to register output		12.0		14.0		16.0		20.0		20.0		22.0	ns
t _{SRR}	Asynchronous reset and preset register recovery time	8.0		8.0		10.0		15.0		15.0		17.0		ns
t _{SRW}	Asynchronous reset or preset width	10.0		10.0		12.0		15.0		15.0		17.0		ns
Clock/LE Width:														
t _{WLS}	Global clock width low	3.0		5.0		6.0		6.0		6.0		7.0		ns
t _{WHS}	Global clock width high	3.0		5.0		6.0		6.0		6.0		7.0		ns
t _{WLA}	Product term clock width low	4.0		5.0		8.0		9.0		9.0		10.0		ns
t _{WHA}	Product term clock width high	4.0		5.0		8.0		9.0		9.0		10.0		ns
t _{GWS}	Global gate width low (for low transparent) or high (for high transparent)	5.0		5.0		6.0		6.0		6.0		7.0		ns
t _{GWA}	Product term gate width low (for low transparent) or high (for high transparent)	4.0		5.0		6.0		9.0		9.0		11.0		ns
t _{WIRL}	Input register clock width low	4.5		5.0		6.0		6.0		6.0		7.0		ns
t _{WIRH}	Input register clock width high	4.5		5.0		6.0		6.0		6.0		7.0		ns
t _{WIL}	Input latch gate width	5.0		5.0		6.0		6.0		6.0		7.0		ns

I_{CC} vs. FREQUENCY

These curves represent the typical power consumption for a particular device at system frequency. The selected “typical” pattern is a 16-bit up-down counter. This pattern fills the device and exercises every macrocell. Maximum frequency shown uses internal feedback and a D-type register. Power/Speed are optimized to obtain the highest counter frequency and the lowest power. The highest frequency (LSBs) is placed in common PAL blocks, which are set to high power. The lowest frequency signals (MSBs) are placed in a common PAL block and set to lowest power.

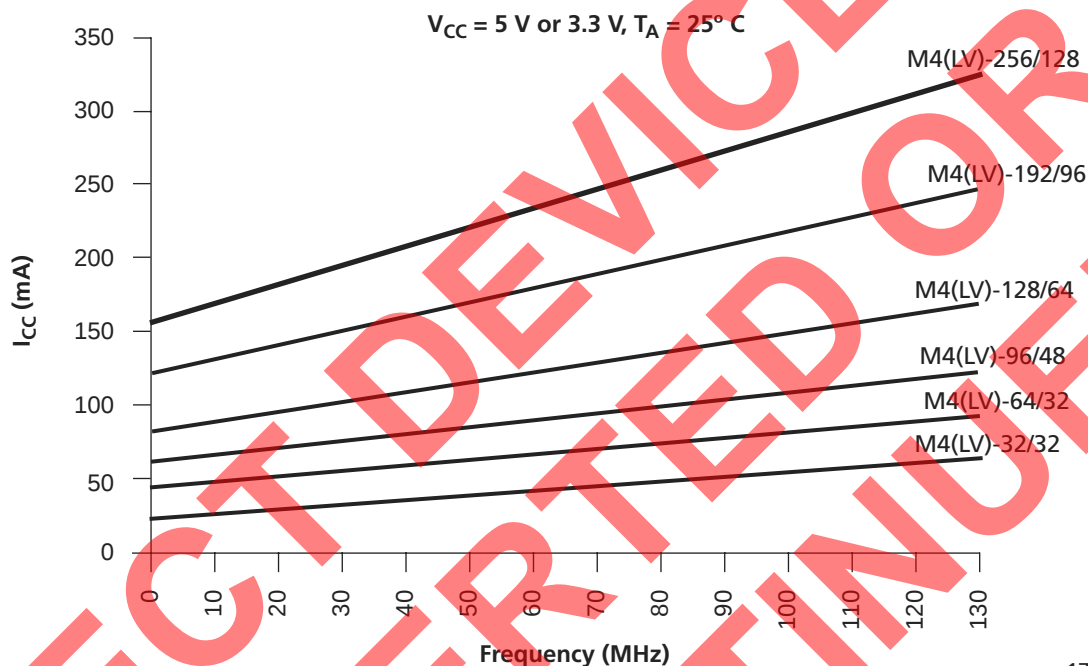


Figure 18. MACH 4 I_{CC} Curves at High Speed Mode

17466G-066

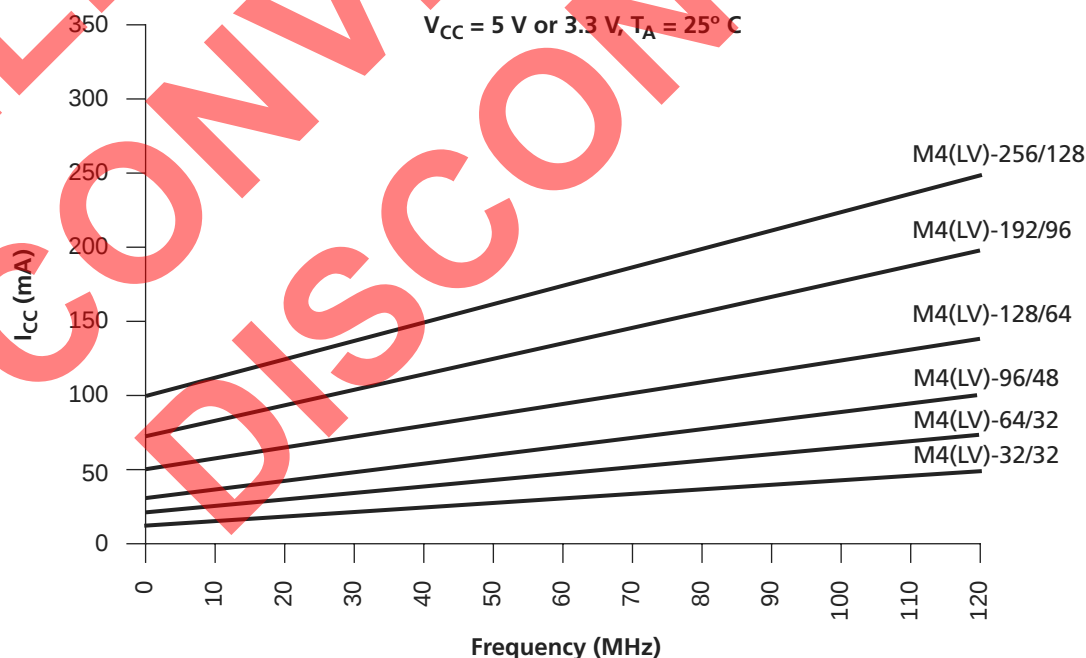


Figure 19. MACH 4 I_{CC} Curves at Low Power Mode

17466G-065

44-PIN TQFP CONNECTION DIAGRAM (M4(LV)-32/32 AND M4(LV)-64/32)

Top View

44-Pin TQFP



PIN DESIGNATIONS

CLK/I	=	Clock or Input
GND	=	Ground
I/O	=	Input/Output
V _{CC}	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out

100-PIN PQFP CONNECTION DIAGRAM (M4(LV)-128/64)

Top View



Note:

The numbers in parentheses reflect compatible pin numbers for 84-pin PLCC.

PIN DESIGNATIONS

- I/CLK = Input or Clock
- GND = Ground
- I = Input
- I/O = Input/Output
- V_{CC} = Supply Voltage
- TDI = Test Data In
- TCK = Test Clock
- TMS = Test Mode Select
- TDO = Test Data Out
- TRST = Test Reset
- ENABLE = Program

208-PIN PQFP CONNECTION DIAGRAM (M4(LV)-256/128)

Top View

208-Pin PQFP



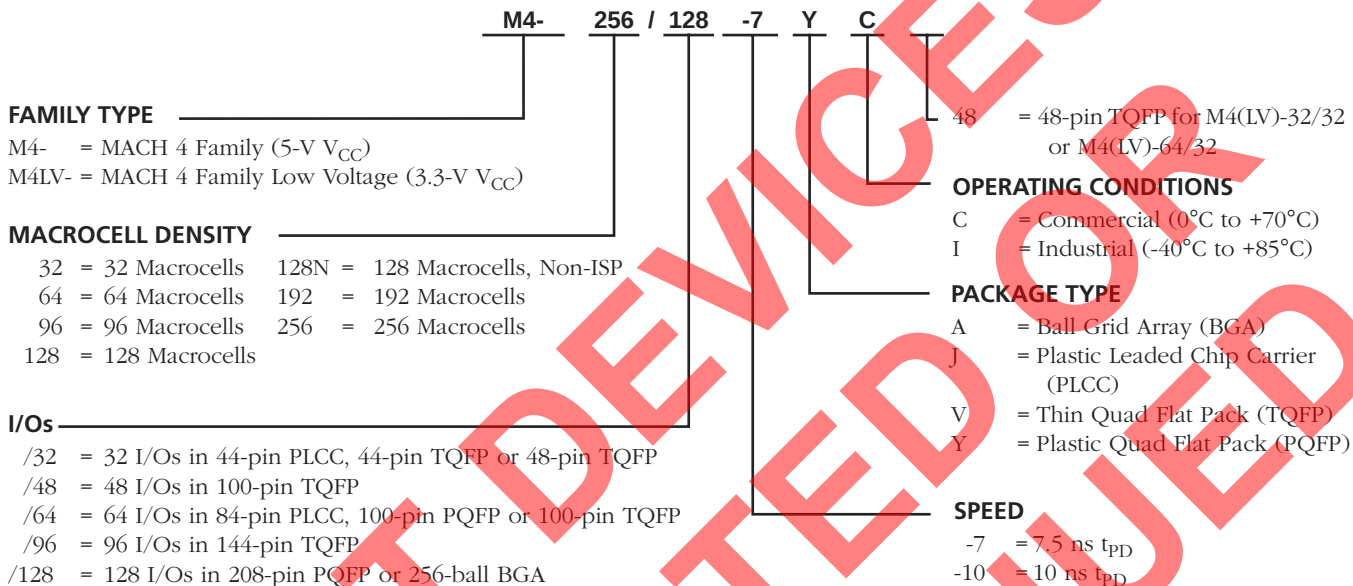
17466G-044

17466H-066

MACH 4 PRODUCT ORDERING INFORMATION

MACH 4 Devices Commercial & Industrial - 3.3V and 5V

Lattice/Vantis programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
M4-32/32	-7, -10, -12, -15	JC, VC, VC48
M4LV-32/32		JC, VC, VC48
M4-64/32		JC, VC, VC48
M4LV-64/32		JC, VC, VC48
M4-96/48		VC
M4LV-96/48		VC
M4-128/64		YC, VC
M4LV-128/64		YC, VC
M4-128N/64		JC
M4LV-128N/64		JC
M4-192/96		VC
M4LV-192/96		VC
M4-256/128		YC
M4LV-256/128		YC, AC

All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial speed grade is slower, i.e., M4-256/128-7YC-10YI

Valid Combinations		
M4-32/32	-10, -12, -14, -18	JL, VI, VI48
M4LV-32/32		JL, VI, VI48
M4-64/32		JL, VI, VI48
M4LV-64/32		JL, VI, VI48
M4-96/48		VI
M4LV-96/48		VI
M4-128/64		YI, VI
M4LV-128/64		YI, VI
M4-128N/64		JL
M4LV-128N/64		JL
M4-192/96		VI
M4LV-192/96		VI
M4-256/128		YI
M4LV-256/128		YI, AI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.