Lattice Semiconductor Corporation - M4-128N/64-12JC Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	12 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	-
Number of Macrocells	128
Number of Gates	-
Number of I/O	64
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m4-128n-64-12jc

GENERAL DESCRIPTION

The MACH® 4 family from Lattice offers an exceptionally flexible architecture and delivers a superior Complex Programmable Logic Device (CPLD) solution of easy-to-use silicon products and software tools. The overall benefits for users are a guaranteed and predictable CPLD solution, faster time-to-market, greater flexibility and lower cost. The MACH 4 devices offer densities ranging from 32 to 256 macrocells with 100% utilization and 100% pin-out retention. The MACH 4 family offer 5-V (M4-xxx) and 3.3-V (M4LV-xxx) operation.

MACH 4 products are 5-V or 3.3-V in-system programmable through the JTAG (IEEE Std. 1149.1) interface. JTAG boundary scan testing also allows product testability on automated test equipment for device connectivity.

All MACH 4 family members deliver First-Time-Fit and easy system integration with pin-out retention after any design change and refit. For both 3.3-V and 5-V operation, MACH 4 products can deliver guaranteed fixed timing as fast as 7.5 ns t_{PD} and 111 MHz f_{CNT} through the SpeedLocking feature when using up to 20 product terms per output (Table 2).

Table 2. MACH 4 Speed Grades

Device	Speed Grade[1]					
	-7	-10	-12	-14	-15	-18
M4-32/32 M4LV-32/32	C	C, I	C, I	I	C	I
M4-64/32 M4LV-64/32	C	C, I	C, I	I	C	I
M4-96/48 M4LV-96/48	C	C, I	C, I	I	C	I
M4-128/64 M4LV-128/64	C	C, I	C, I	I	C	I
M4-128N/64 M4LV-128N/64	C	C, I	C, I	I	C	I
M4-192/96 M4LV-192/96	C	C, I	C, I	I	C	I
M4-256/128 M4LV-256/128	C	C, I	C, I	I	C	I

Note:

1. C = Commercial, I = Industrial

The MACH 4 family offers numerous density-I/O combinations in Thin Quad Flat Pack (TQFP), Plastic Quad Flat Pack (PQFP), Plastic Leaded Chip Carrier (PLCC), and Ball Grid Array (BGA) packages ranging from 44 to 256 pins (Table 3). It also offers I/O safety features for mixed-voltage designs so that the 3.3-V devices can accept 5-V inputs, and 5-V devices do not overdrive 3.3-V inputs. Additional features include Bus-Friendly inputs and I/Os, a programmable power-down mode for extra power savings and individual output slew rate control for the highest speed transition or for the lowest noise transition.

Table 4. Architectural Summary of MACH 4 devices

	MACH 4 Devices	
	M4-64/32, M4LV-64/32 M4-96/48, M4LV-96/48 M4-128/64, M4LV-128/64 M4-128N/64, M4LV-128N/64 M4-192/96, M4LV-192/96 M4-256/128, M4LV-256/128	M4-32/32 M4LV-32/32
Macrocell-I/O Cell Ratio	2:1	1:1
Input Switch Matrix	Yes	Yes
Input Registers	Yes	No
Central Switch Matrix	Yes	Yes
Output Switch Matrix	Yes	Yes

The Macrocell-I/O cell ratio is defined as the number of macrocells versus the number of I/O cells internally in a PAL block (Table 4).

The central switch matrix takes all dedicated inputs and signals from the input switch matrices and routes them as needed to the PAL blocks. Feedback signals that return to the same PAL block still must go through the central switch matrix. This mechanism ensures that PAL blocks in MACH 4 devices communicate with each other with consistent, predictable delays.

The central switch matrix makes a MACH 4 device more advanced than simply several PAL devices on a single chip. It allows the designer to think of the device not as a collection of blocks, but as a single programmable device; the software partitions the design into PAL blocks through the central switch matrix so that the designer does not have to be concerned with the internal architecture of the device.

Each PAL block consists of:

- Product-term array
- Logic allocator
- Macrocells
- Output switch matrix
- I/O cells
- Input switch matrix
- Clock generator

Product-Term Array

The product-term array consists of a number of product terms that form the basis of the logic being implemented. The inputs to the AND gates come from the central switch matrix (Table 5), and are provided in both true and complement forms for efficient logic implementation.

Table 5. PAL Block Inputs

Device	Number of Inputs to PAL Block
M4-32/32 and M4LV-32/32	33
M4-64/32 and M4LV-64/32	33
M4-96/48 and M4LV-96/48	33
M4-128/64 and M4LV-128/64	33
M4-128N/64 and M4LV-128N/64	33
M4-192/96 and M4LV-192/96	34
M4-256/128 and M4LV-256/128	34

Logic Allocator

Within the logic allocator, product terms are allocated to macrocells in "product term clusters." The availability and distribution of product term clusters are automatically considered by the software as it fits functions within a PAL block. The size of a product term cluster has been optimized to provide high utilization of product terms, making complex functions using many product terms possible. Yet when few product terms are used, there will be a minimal number of unused—or wasted—product terms left over. The product term clusters available to each macrocell within a PAL block are shown in Tables 6 and 7.

Each product term cluster is associated with a macrocell. The size of a cluster depends on the configuration of the associated macrocell. When the macrocell is used in synchronous mode (Figure 2a), the basic cluster has 4 product terms. When the associated macrocell is used in asynchronous mode (Figure 2b), the cluster has 2 product terms. Note that if the product term cluster is routed to a different macrocell, the allocator configuration is not determined by the mode of the macrocell actually being driven. The configuration is always set by the mode of the macrocell that the cluster will drive if not routed away, regardless of the actual routing.

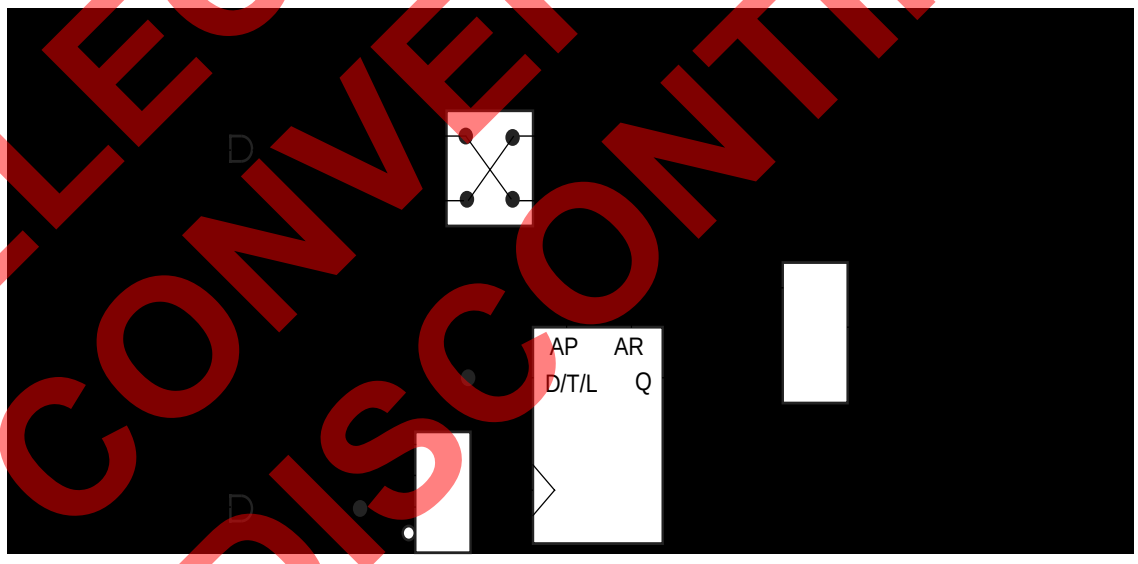
In addition, there is an extra product term that can either join the basic cluster to give an extended cluster, or drive the second input of an exclusive-OR gate in the signal path. If included with the basic cluster, this provides for up to 20 product terms on a synchronous function that uses four extended 5-product-term clusters. A similar asynchronous function can have up to 18 product terms.

When the extra product term is used to extend the cluster, the value of the second XOR input can be programmed as a 0 or a 1, giving polarity control. The possible configurations of the logic allocator are shown in Figures 3 and 4.

Macrocell

The macrocell consists of a storage element, routing resources, a clock multiplexer, and initialization control. The macrocell has two fundamental modes: synchronous and asynchronous (Figure 5). The mode chosen only affects clocking and initialization in the macrocell.

a. Synchronous mode



b. Asynchronous mode

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Figure 5. Macrocell

In either mode, a combinatorial path can be used. For combinatorial logic, the synchronous mode will generally be used, since it provides more product terms in the allocator.

The flip-flop can be configured as a D-type or T-type latch. J-K or S-R registers can be synthesized. The primary flip-flop configurations are shown in Figure 6, although others are possible. Flip-flop functionality is defined in Table 8. Note that a J-K latch is inadvisable as it will cause oscillation if both J and K inputs are HIGH.

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Figure 6. Primary Macrocell Configurations

Table 8. Register/Latch Operation

Configuration	Input(s)	CLK/LE [1]	Q+
D-type Register	D=X	0, 1, ↓ (↑)	Q
	D=0	↑ (↓)	0
	D=1	↑ (↓)	1
T-type Register	T=X	0, 1, ↓ (↑)	Q
	T=0	↑ (↓)	Q
	T=1	↑ (↓)	$\overline{Q}$
D-type Latch	D=X	1 (0)	Q
	D=0	0 (1)	0
	D=1	0 (1)	1

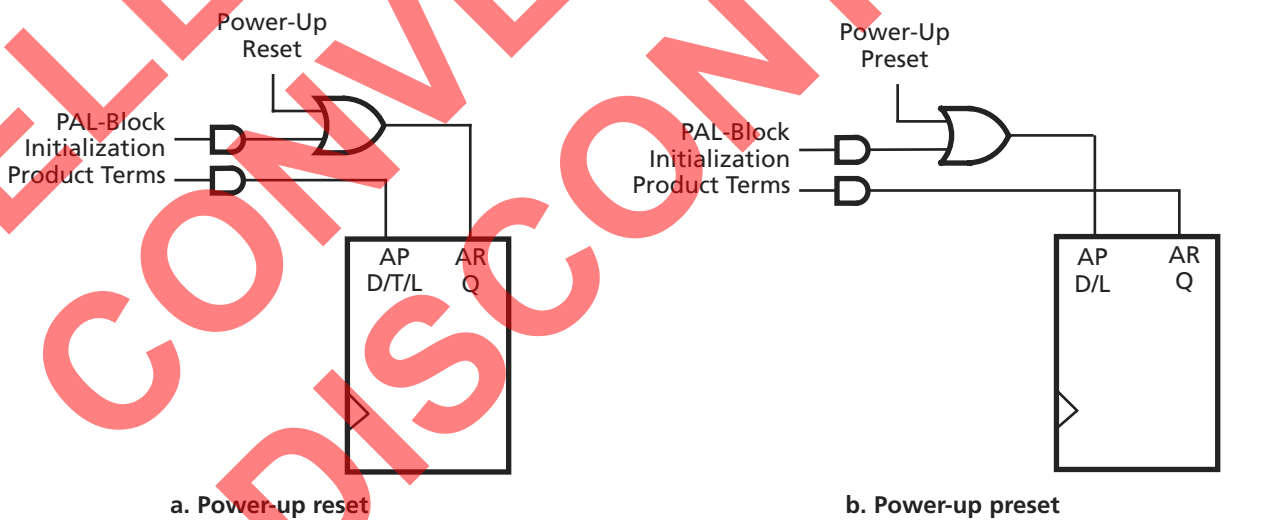
Note:

1. Polarity of CLK/LE can be programmed

Although the macrocell shows only one input to the register, the XOR gate in the logic allocator allows the D-, T-type register to emulate J-K, and S-R behavior. In this case, the available product terms are divided between J and K (or S and R). When configured as J-K, S-R, or T-type, the extra product term must be used on the XOR gate input for flip-flop emulation. In any register type, the polarity of the inputs can be programmed.

The clock input to the flip-flop can select any of the four PAL block clocks in synchronous mode, with the additional choice of either polarity of an individual product term clock in the asynchronous mode.

The initialization circuit depends on the mode. In synchronous mode (Figure 7), asynchronous reset and preset are provided, each driven by a product term common to the entire PAL block.



a. Power-up reset

b. Power-up preset

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Figure 7. Synchronous Mode Initialization Configurations

Output Switch Matrix

The output switch matrix allows macrocells to be connected to any of several I/O cells within a PAL block. This provides high flexibility in determining pinout and allows design changes to occur without effecting pinout.

In MACH 4 devices with 2:1 Macrocell-I/O cell ratio, each PAL block has twice as many macrocells as I/O cells. The MACH 4 output switch matrix allows for half of the macrocells to drive I/O cells within a PAL block, in combinations according to Figure 9. Each I/O cell can choose from eight macrocells; each macrocell has a choice of four I/O cells. The MACH 4 devices with 1:1 Macrocell-I/O cell ratio allow each macrocell to drive one of eight I/O cells (Figure 9).

Figure 9. MACH 4 Output Switch Matrix

I/O Cell

The I/O cell (Figures 10 and 11) simply consists of a programmable output enable, a feedback path, and flip-flop (except MACH 4 devices with 1:1 macrocell-I/O cell ratio.) An individual output enable product term is provided for each I/O cell. The feedback signal drives the input switch matrix.

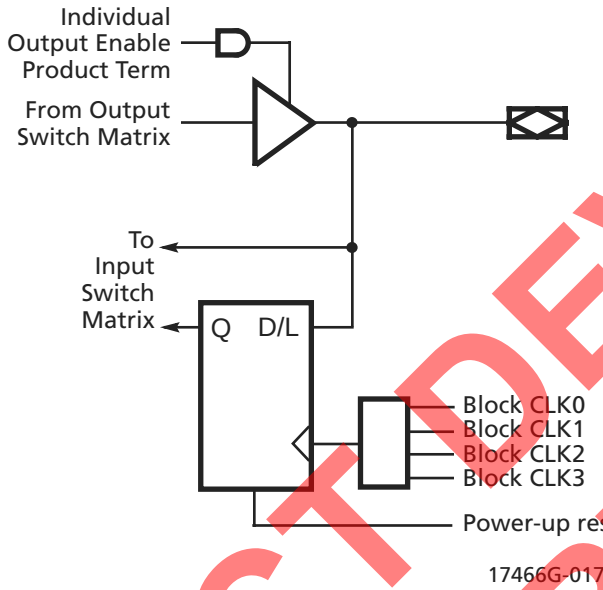

Figure 10. I/O Cell for MACH 4 Devices with 2:1 Macrocell-I/O Cell Ratio

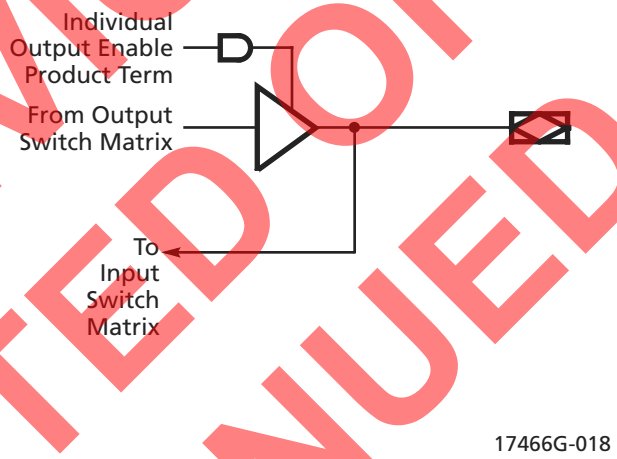

Figure 11. I/O Cell for MACH 4 Devices with 1:1 Macrocell-I/O Cell Ratio

The I/O cell (Figure 10) contains a flip-flop, which provides the capability for storing the input in a D-type register or latch. The clock can be any of the PAL block clocks. Both the direct and registered versions of the input are sent to the input switch matrix. This allows for such functions as "time-domain-multiplexed" data comparison, where the first data value is stored, and then the second data value is put on the I/O pin and compared with the previous stored value.

Note that the flip-flop used in the MACH 4 I/O cell is independent of the flip-flops in the macrocells. It powers up to a logic low.

Zero-Hold-Time Input Register

The MACH 4 devices have a zero-hold-time (ZHT) fuse which controls the time delay associated with loading data into all I/O cell registers and latches. When programmed, the ZHT fuse increases the data path setup delays to input storage elements, matching equivalent delays in the clock path. When the fuse is erased, the setup time to the input storage element is minimized. This feature facilitates doing worst-case designs for which data is loaded from sources which have low (or zero) minimum output propagation delays from clock edges.

Input Switch Matrix

The input switch matrix (Figures 12 and 13) optimizes routing of inputs to the central switch matrix. Without the input switch matrix, each input and feedback signal has only one way to enter the central switch matrix. The input switch matrix provides additional ways for these signals to enter the central switch matrix.

Table 12. PAL Block Clock Combinations[1]

Block CLK0	Block CLK1	Block CLK2	Block CLK3
GCLK0	GCLK1	X	X
$\overline{\text{GCLK1}}$	GCLK1	X	X
GCLK0	$\overline{\text{GCLK0}}$	X	X
$\overline{\text{GCLK1}}$	$\overline{\text{GCLK0}}$	X	X
X	X	GCLK2 (GCLK0)	GCLK3 (GCLK1)
X	X	$\overline{\text{GCLK3}}$ ($\overline{\text{GCLK1}}$)	GCLK3 (GCLK1)
X	X	GCLK2 (GCLK0)	$\overline{\text{GCLK2}}$ ($\overline{\text{GCLK0}}$)
X	X	$\overline{\text{GCLK3}}$ ($\overline{\text{GCLK1}}$)	$\overline{\text{GCLK2}}$ ($\overline{\text{GCLK0}}$)

Note:

1. Values in parentheses are for the M4(LV)-32/32 and M4(LV)-64/32.

This feature provides high flexibility for partitioning state machines and dual-phase clocks. It also allows latches to be driven with either polarity of latch enable, and in a master-slave configuration.

MACH 4 TIMING MODEL

The primary focus of the MACH 4 timing model is to accurately represent the timing in a MACH 4 device, and at the same time, be easy to understand. This model accurately describes all combinatorial and registered paths through the device, making a distinction between internal feedback and external feedback. A signal uses internal feedback when it is fed back into the switch matrix or block without having to go through the output buffer. The input register specifications are also reported as internal feedback. When a signal is fed back into the switch matrix after having gone through the output buffer, it is using external feedback.

The parameter, t_{BUF}, is defined as the time it takes to go from feedback through the output buffer to the I/O pad. If a signal goes to the internal feedback rather than to the I/O pad, the parameter designator is followed by an "i". By adding t_{BUF} to this internal parameter, the external parameter is derived. For example, $t_{PD} = t_{PDi} + t_{BUF}$. A diagram representing the modularized MACH 4 timing model is shown in Figure 15. Refer to the Technical Note entitled *MACH 4 Timing and High Speed Design* for a more detailed discussion about the timing parameters.

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Figure 15. MACH 4 Timing Model

SPEEDLOCKING FOR GUARANTEED FIXED TIMING

The MACH 4 architecture allows allocation of up to 20 product terms to an individual macrocell with the assistance of an XOR gate without incurring additional timing delays.

The design of the switch matrix and PAL blocks guarantee a fixed pin-to-pin delay that is independent of the logic required by the design. Other competitive CPLDs incur serious timing delays as product terms expand beyond their typical 4 or 5 product term limits. Speed *and* SpeedLocking combine to give designs easy access to the performance required in today's designs.

IEEE 1149.1-COMPLIANT BOUNDARY SCAN TESTABILITY

All MACH 4 devices, except the M4(LV)-128N/64, have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more complete board-level testing.

IEEE 1149.1-COMPLIANT IN-SYSTEM PROGRAMMING

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality, and the ability to make in-field modifications. All MACH 4 devices provide In-System Programming (ISP) capability through their Boundary ScanTest Access Ports. This capability has been implemented in a manner that ensures that the port remains compliant to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

MACH 4 devices can be programmed across the commercial temperature and voltage range. The PC-based LatticePRO software facilitates in-system programming of MACH 4 devices. LatticePRO takes the JEDEC file output produced by the design implementation software, along with information about the JTAG chain, and creates a set of vectors that are used to drive the JTAG chain. LatticePRO software can use these vectors to drive a JTAG chain via the parallel port of a PC. Alternatively, LatticePRO software can output files in formats understood by common automated test equipment. This equpment can then be used to program MACH 4 devices during the testing of a circuit board.

PCI COMPLIANT

MACH 4 devices in the -7/-10/-12 speed grades are compliant with the *PCI Local Bus Specification* version 2.1, published by the PCI Special Interest Group (SIG). The 5-V devices are fully PCI-compliant. The 3.3-V devices are mostly compliant but do not meet the PCI condition to clamp the inputs as they rise above V_{CC} because of their 5-V input tolerant feature.

SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS

Both the 3.3-V and 5-V V_{CC} MACH 4 devices are safe for mixed supply voltage system designs. The 5-V devices will not overdrive 3.3-V devices above the output voltage of 3.3 V, while they accept inputs from other 3.3-V devices. The 3.3-V device will accept inputs up to 5.5 V. Both the 5-V and 3.3-V versions have the same high-speed performance and provide easy-to-use mixed-voltage design capability.

BUS-FRIENDLY INPUTS AND I/OS

All MACH 4 devices have inputs and I/Os which feature the Bus-Friendly circuitry incorporating two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state. While it is good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from the input threshold voltage where noise can cause high-frequency switching. At power-up, the Bus-Friendly latches are reset to a logic level "1." For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice/Vantis Data Book CD-ROM or Lattice web site.

POWER MANAGEMENT

Each individual PAL block in MACH 4 devices features a programmable low-power mode, which results in power savings of up to 50%. The signal speed paths in the low-power PAL block will be slower than those in the non-low-power PAL block. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in the low-power mode.

PROGRAMMABLE SLEW RATE

Each MACH 4 device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3 V/ns) or for the lower noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

POWER-UP RESET/SET

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

SECURITY BIT

A programmable security bit is provided on the MACH 4 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

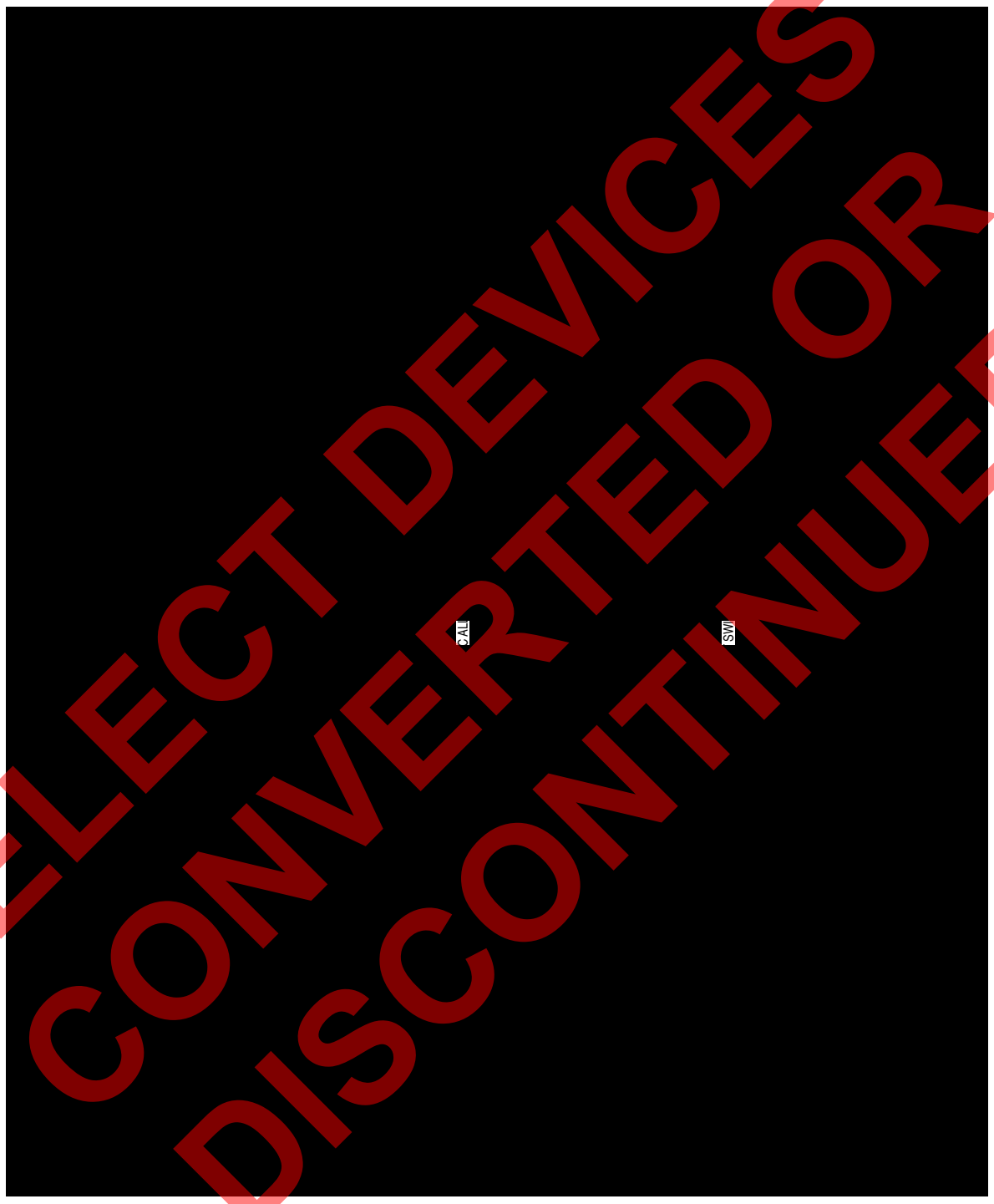
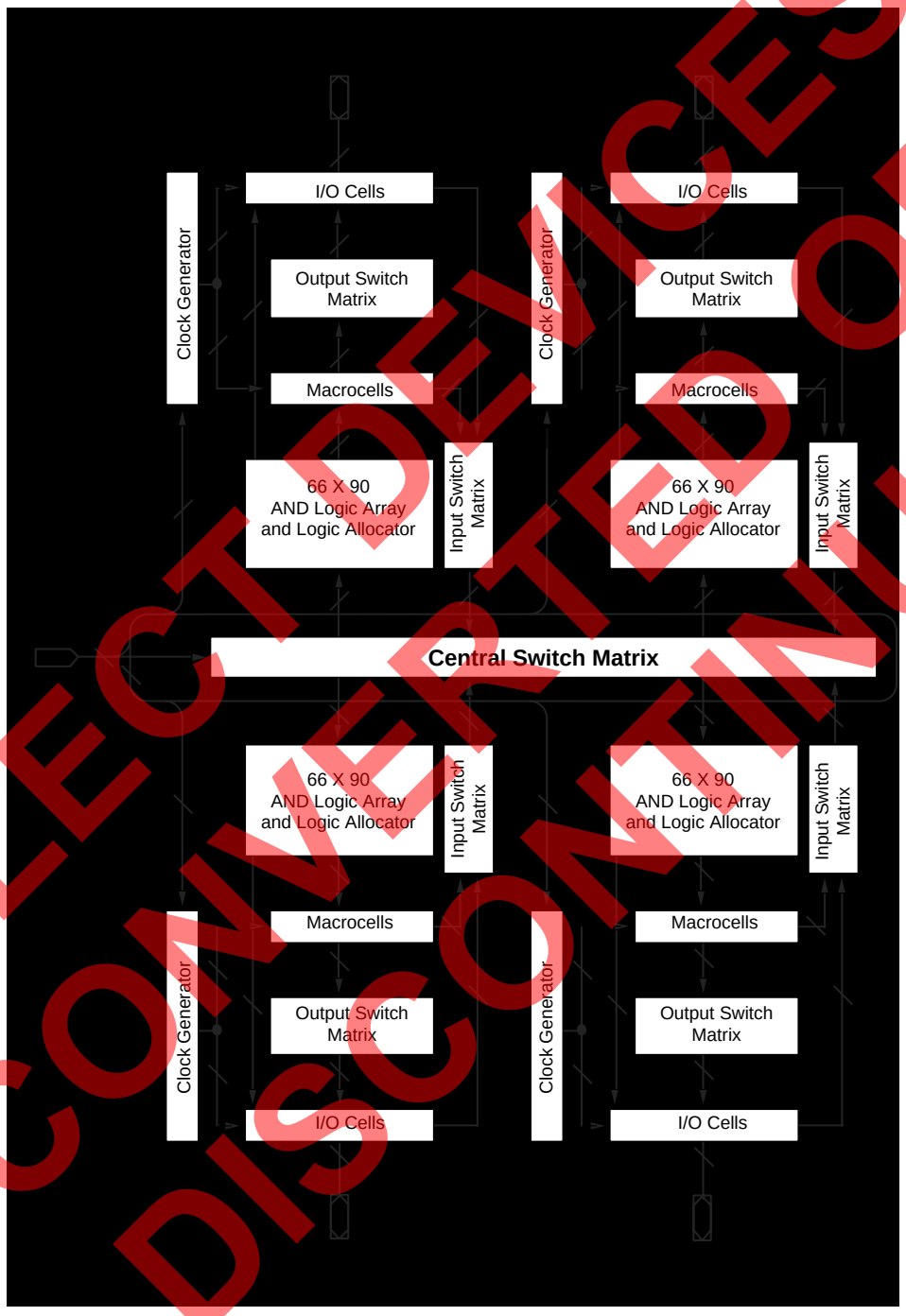


Figure 16. PAL Block for MACH 4 with 2:1 Macrocell - I/O Cell Ratio

BLOCK DIAGRAM – M4(LV)-64/32



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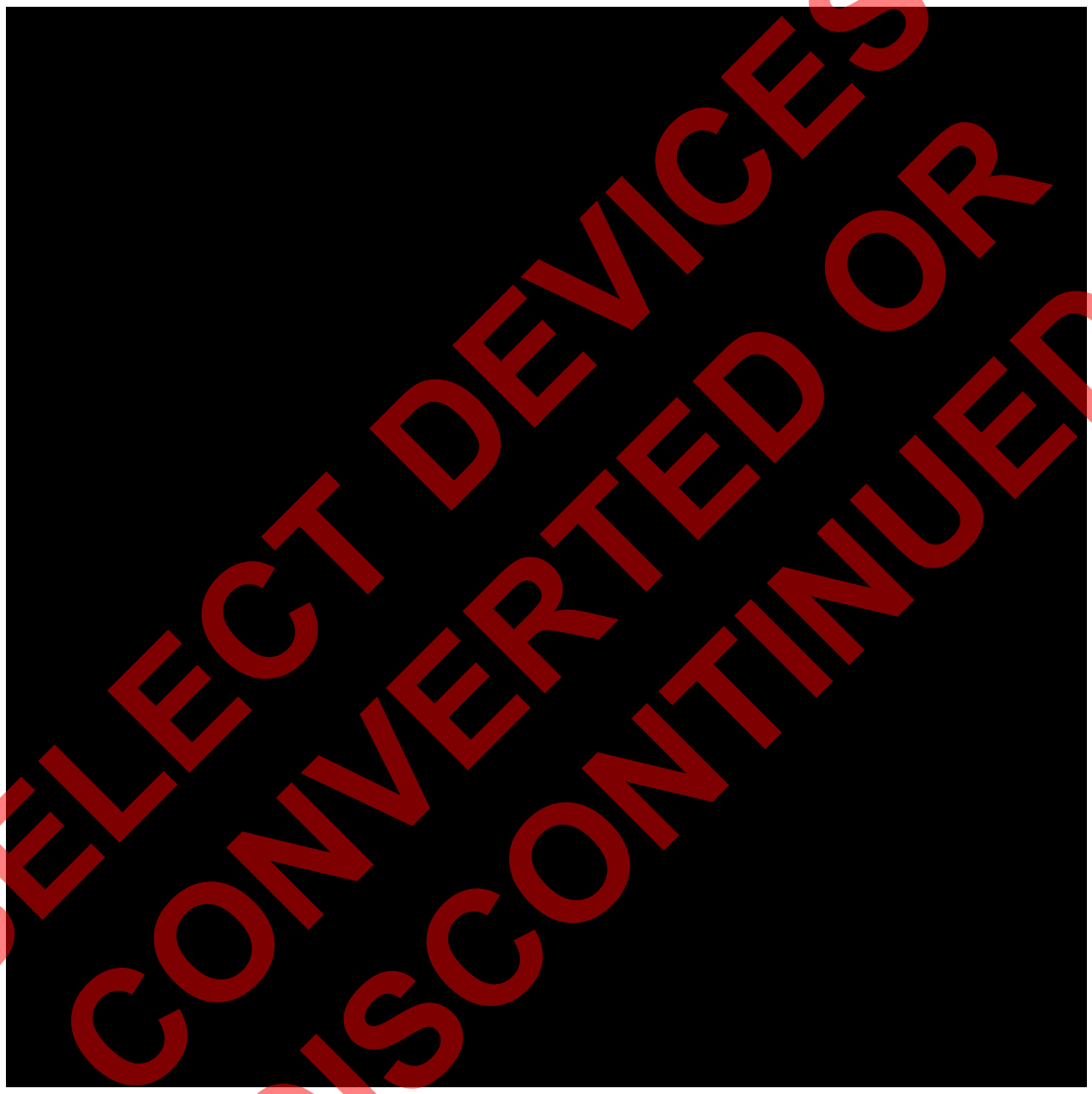
BLOCK DIAGRAM – M4(LV)-192/96



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44-PIN PLCC CONNECTION DIAGRAM (M4(LV)-32/32 AND M4(LV)-64/32)

Top View

44-Pin PLCC

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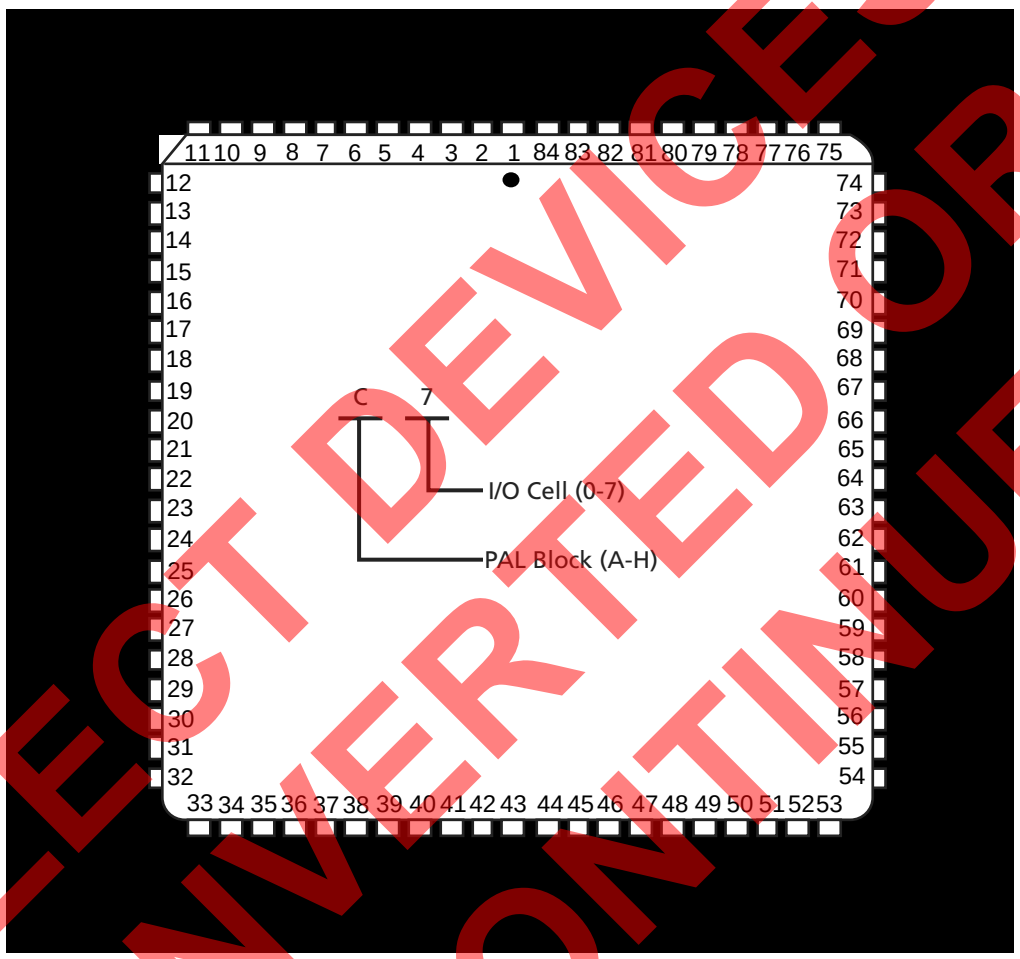
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

84-PIN PLCC CONNECTION DIAGRAM (M4(LV)-128N/64)

Top View

84-Pin PLCC



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Note:
Pin-compatible with the MACH131, MACH231, MACH435.

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

I/O = Input/Output

V_{CC} = Supply Voltage

100-PIN TQFP CONNECTION DIAGRAM (M4(LV)-128/64)

Top View

100-Pin TQFP

17466G-032

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out
TRST = Test Reset
ENABLE = Program

208-PIN PQFP CONNECTION DIAGRAM (M4(LV)-256/128)

Top View

208-Pin PQFP

17466G-044

17466H-066

MACH 4 PRODUCT ORDERING INFORMATION

MACH 4 Devices Commercial & Industrial - 3.3V and 5V

Lattice/Vantis programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

M4- / 256 / 128 -7 Y C

FAMILY TYPE

M4- = MACH 4 Family (5-V V_{CC})
M4LV- = MACH 4 Family Low Voltage (3.3-V V_{CC})

MACROCELL DENSITY

32 = 32 Macrocells
64 = 64 Macrocells
96 = 96 Macrocells
128 = 128 Macrocells
128N = 128 Macrocells, Non-ISP
192 = 192 Macrocells
256 = 256 Macrocells

I/Os

/32 = 32 I/Os in 44-pin PLCC, 44-pin TQFP or 48-pin TQFP
/48 = 48 I/Os in 100-pin TQFP
/64 = 64 I/Os in 84-pin PLCC, 100-pin PQFP or 100-pin TQFP
/96 = 96 I/Os in 144-pin TQFP
/128 = 128 I/Os in 208-pin PQFP or 256-ball BGA

SPEED

-7 = 7.5 ns t_{PD}
-10 = 10 ns t_{PD}
-12 = 12 ns t_{PD}
-14 = 14 ns t_{PD}
-15 = 15 ns t_{PD}
-18 = 18 ns t_{PD}

PACKAGE TYPE

A = Ball Grid Array (BGA)
J = Plastic Leaded Chip Carrier (PLCC)
V = Thin Quad Flat Pack (TQFP)
Y = Plastic Quad Flat Pack (PQFP)

OPERATING CONDITIONS

C = Commercial (0°C to +70°C)
I = Industrial (-40°C to +85°C)

48 = 48-pin TQFP for M4(LV)-32/32 or M4(LV)-64/32

Valid Combinations		
M4-32/32	-7, -10, -12, -15	JC, VC, VC48
M4LV-32/32		JC, VC, VC48
M4-64/32		JC, VC, VC48
M4LV-64/32		JC, VC, VC48
M4-96/48		VC
M4LV-96/48		VC
M4-128/64		YC, VC
M4LV-128/64		YC, VC
M4-128N/64		JC
M4LV-128N/64		JC
M4-192/96		VC
M4LV-192/96		VC
M4-256/128		YC
M4LV-256/128		YC, AC

All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial speed grade is slower, i.e., M4-256/128-7YC-10YI

Valid Combinations		
M4-32/32	-10, -12, -14, -18	JI, VI, VI48
M4LV-32/32		JI, VI, VI48
M4-64/32		JI, VI, VI48
M4LV-64/32		JI, VI, VI48
M4-96/48		VI
M4LV-96/48		VI
M4-128/64		YI, VI
M4LV-128/64		YI, VI
M4-128N/64		JI
M4LV-128N/64		JI
M4-192/96		VI
M4LV-192/96		VI
M4-256/128		YI
M4LV-256/128		YI, AI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.