Lattice Semiconductor Corporation - M4-128N/64-12JI Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	12 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	128
Number of Gates	-
Number of I/O	64
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m4-128n-64-12ji

Product Line	Ordering Part Number	Product Status	Reference PCN
M4-128/64 (Cont'd)	M4-128/64-7VC	Convert to M4A5	Contact pcn@latticesemi.com for more info.
	M4-128/64-10VC		
	M4-128/64-12VC		
	M4-128/64-15VC		
	M4-128/64-10VI		
	M4-128/64-12VI		
	M4-128/64-14VI		
	M4-128/64-18VI		
M4-128N/64	M4-128N/64-7JC	Active / Orderable	
	M4-128N/64-10JC		
	M4-128N/64-12JC		
	M4-128N/64-15JC		
	M4-128N/64-10JI		
	M4-128N/64-12JI		
	M4-128N/64-14JI		
	M4-128N/64-18JI		
M4-192/96	M4-192/96-7VC	Convert to M4A5	Contact pcn@latticesemi.com for more info.
	M4-192/96-10VC		
	M4-192/96-12VC		
	M4-192/96-15VC		
	M4-192/96-10VI		
	M4-192/96-12VI		
	M4-192/96-14VI		
	M4-192/96-18VI		
M4-256/128	M4-256/128-7YC	Convert to M4A5	Contact pcn@latticesemi.com for more info.
	M4-256/128-10YC		
	M4-256/128-12YC		
	M4-256/128-15YC		
	M4-256/128-10YI		
	M4-256/128-12YI		
	M4-256/128-14YI		
	M4-256/128-18YI		
M4LV-32/32	M4LV-32/32-7JC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-32/32-10JC		
	M4LV-32/32-12JC		
	M4LV-32/32-15JC		
	M4LV-32/32-10JI		
	M4LV-32/32-12JI		
	M4LV-32/32-14JI		
	M4LV-32/32-18JI		

5555 N.E. Moore Ct. ● Hillsboro, Oregon 97124-6421 ● Phone (503) 268-8000 ● FAX (503) 268-8347
Internet: http://www.latticesemi.com

Product Line	Ordering Part Number	Product Status	Reference PCN
M4LV-96/48	M4LV-96/48-7VC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-96/48-10VC		
	M4LV-96/48-12VC		
	M4LV-96/48-15VC		
	M4LV-96/48-10VI		
	M4LV-96/48-12VI		
	M4LV-96/48-14VI		
	M4LV-96/48-18VI		
M4LV-128/64	M4LV-128/64-7YC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-128/64-10YC		
	M4LV-128/64-12YC		
	M4LV-128/64-15YC		
	M4LV-128/64-10YI		
	M4LV-128/64-12YI		
	M4LV-128/64-14YI		
	M4LV-128/64-18YI		
	M4LV-128/64-7VC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-128/64-10VC		
	M4LV-128/64-12VC		
	M4LV-128/64-15VC		
	M4LV-128/64-10VI		
	M4LV-128/64-12VI		
	M4LV-128/64-14VI		
	M4LV-128/64-18VI		
M4LV-128N/64	M4LV-128N/64-7JC	**Discontinued**	PCN#09-10
	M4LV-128N/64-10JC		
	M4LV-128N/64-12JC		
	M4LV-128N/64-15JC		
	M4LV-128N/64-10JI		
	M4LV-128N/64-12JI		
	M4LV-128N/64-14JI		
	M4LV-128N/64-18JI		
M4LV-192/96	M4LV-192/96-7VC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-192/96-10VC		
	M4LV-192/96-12VC		
	M4LV-192/96-15VC		
	M4LV-192/96-10VI		
	M4LV-192/96-12VI		
	M4LV-192/96-14VI		
	M4LV-192/96-18VI		

MACH 4 CPLD Family

High Performance E^{2}CMOS® In-System Programmable Logic

FEATURES

- **High-performance, E^{2}CMOS 3.3-V & 5-V CPLD families**
- **Flexible architecture for rapid logic designs**
  - — Excellent First-Time-Fit™ and refit feature
  - — SpeedLocking™ performance for guaranteed fixed timing
  - — Central, input and output switch matrices for 100% routability and 100% pin-out retention
- **High speed**
  - — 7.5ns t_{PD} Commercial and 10ns t_{PD} Industrial
  - — 111.1MHz f_{CNT}
- **32 to 256 macrocells; 32 to 384 registers**
- **44 to 256 pins in PLCC, PQFP, TQFP and BGA packages**
- **Flexible architecture for a wide range of design styles**
  - — D/T registers and latches
  - — Synchronous or asynchronous mode
  - — Dedicated input registers
  - — Programmable polarity
  - — Reset/ preset swapping
- **Advanced capabilities for easy system integration**
  - — 3.3-V & 5-V JEDEC-compliant operations
  - — JTAG (IEEE 1149.1) compliant for boundary scan testing
  - — 3.3-V & 5-V JTAG in-system programming
  - — PCI compliant (-7/-10/-12 speed grades)
  - — Safe for mixed supply voltage system designs
  - — Bus-Friendly™ inputs and I/Os
  - — Programmable security bit
  - — Individual output slew rate control
- **Advanced E^{2}CMOS process provides high-performance, cost-effective solutions**
- **Supported by ispDesignEXPERT™ software for rapid logic development**
  - — Supports HDL design methodologies with results optimized for MACH 4
  - — Flexibility to adapt to user requirements
  - — Software partnerships that ensure customer success
- **Lattice and third-party hardware programming support**
  - — LatticePRO™ software for in-system programmability support on PCs and automated test equipment
  - — Programming support on all major programmers including Data I/O, BP Microsystems, Advin, and System General

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Table 1. MACH 4 Device Features[1, 2]

Feature	M4-32/32 M4LV-32/32	M4-64/32 M4LV-64/32	M4-96/48 M4LV-96/48	M4-128/64 M4LV-128/64	M4-128N/64 M4LV-128N/64	M4-192/96 M4LV-192/96	M4-256/128 M4LV-256/128
Macrocells	32	64	96	128	128	192	256
Maximum User I/O Pins	32	32	48	64	64	96	128
t_{PD} (ns)	7.5	7.5	7.5	7.5	7.5	7.5	7.5
f_{CNT} (MHz)	111	111	111	111	111	111	111
t_{COS} (ns)	5.5	5.5	5.5	5.5	5.5	5.5	5.5
t_{SS} (ns)	5.5	5.5	5.5	5.5	5.5	5.5	5.5
Static Power (mA)	25	25	50	70	70	85	100
JTAG Compliant	Yes	Yes	Yes	Yes	No	Yes	Yes
PCI Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Notes:

1. *For information on the M4-96/96 device, please refer to the M4-96/96 data sheet at www.latticesemi.com.*
2. *"M4-xxx" is for 5-V devices. "M4LV-xxx" is for 3.3-V devices.*

GENERAL DESCRIPTION

The MACH® 4 family from Lattice offers an exceptionally flexible architecture and delivers a superior Complex Programmable Logic Device (CPLD) solution of easy-to-use silicon products and software tools. The overall benefits for users are a guaranteed and predictable CPLD solution, faster time-to-market, greater flexibility and lower cost. The MACH 4 devices offer densities ranging from 32 to 256 macrocells with 100% utilization and 100% pin-out retention. The MACH 4 family offer 5-V (M4-xxx) and 3.3-V (M4LV-xxx) operation.

MACH 4 products are 5-V or 3.3-V in-system programmable through the JTAG (IEEE Std. 1149.1) interface. JTAG boundary scan testing also allows product testability on automated test equipment for device connectivity.

All MACH 4 family members deliver First-Time-Fit and easy system integration with pin-out retention after any design change and refit. For both 3.3-V and 5-V operation, MACH 4 products can deliver guaranteed fixed timing as fast as 7.5 ns t_{PD} and 111 MHz f_{CNT} through the SpeedLocking feature when using up to 20 product terms per output (Table 2).

Table 2. MACH 4 Speed Grades

Device	Speed Grade[1]					
	-7	-10	-12	-14	-15	-18
M4-32/32 M4LV-32/32	C	C, I	C, I	I	C	I
M4-64/32 M4LV-64/32	C	C, I	C, I	I	C	I
M4-96/48 M4LV-96/48	C	C, I	C, I	I	C	I
M4-128/64 M4LV-128/64	C	C, I	C, I	I	C	I
M4-128N/64 M4LV-128N/64	C	C, I	C, I	I	C	I
M4-192/96 M4LV-192/96	C	C, I	C, I	I	C	I
M4-256/128 M4LV-256/128	C	C, I	C, I	I	C	I

Note:

1. C = Commercial, I = Industrial

The MACH 4 family offers numerous density-I/O combinations in Thin Quad Flat Pack (TQFP), Plastic Quad Flat Pack (PQFP), Plastic Leaded Chip Carrier (PLCC), and Ball Grid Array (BGA) packages ranging from 44 to 256 pins (Table 3). It also offers I/O safety features for mixed-voltage designs so that the 3.3-V devices can accept 5-V inputs, and 5-V devices do not overdrive 3.3-V inputs. Additional features include Bus-Friendly inputs and I/Os, a programmable power-down mode for extra power savings and individual output slew rate control for the highest speed transition or for the lowest noise transition.

Product-Term Array

The product-term array consists of a number of product terms that form the basis of the logic being implemented. The inputs to the AND gates come from the central switch matrix (Table 5), and are provided in both true and complement forms for efficient logic implementation.

Table 5. PAL Block Inputs

Device	Number of Inputs to PAL Block
M4-32/32 and M4LV-32/32	33
M4-64/32 and M4LV-64/32	33
M4-96/48 and M4LV-96/48	33
M4-128/64 and M4LV-128/64	33
M4-128N/64 and M4LV-128N/64	33
M4-192/96 and M4LV-192/96	34
M4-256/128 and M4LV-256/128	34

Logic Allocator

Within the logic allocator, product terms are allocated to macrocells in "product term clusters." The availability and distribution of product term clusters are automatically considered by the software as it fits functions within a PAL block. The size of a product term cluster has been optimized to provide high utilization of product terms, making complex functions using many product terms possible. Yet when few product terms are used, there will be a minimal number of unused—or wasted—product terms left over. The product term clusters available to each macrocell within a PAL block are shown in Tables 6 and 7.

Each product term cluster is associated with a macrocell. The size of a cluster depends on the configuration of the associated macrocell. When the macrocell is used in synchronous mode (Figure 2a), the basic cluster has 4 product terms. When the associated macrocell is used in asynchronous mode (Figure 2b), the cluster has 2 product terms. Note that if the product term cluster is routed to a different macrocell, the allocator configuration is not determined by the mode of the macrocell actually being driven. The configuration is always set by the mode of the macrocell that the cluster will drive if not routed away, regardless of the actual routing.

In addition, there is an extra product term that can either join the basic cluster to give an extended cluster, or drive the second input of an exclusive-OR gate in the signal path. If included with the basic cluster, this provides for up to 20 product terms on a synchronous function that uses four extended 5-product-term clusters. A similar asynchronous function can have up to 18 product terms.

When the extra product term is used to extend the cluster, the value of the second XOR input can be programmed as a 0 or a 1, giving polarity control. The possible configurations of the logic allocator are shown in Figures 3 and 4.

MACH 4 TIMING MODEL

The primary focus of the MACH 4 timing model is to accurately represent the timing in a MACH 4 device, and at the same time, be easy to understand. This model accurately describes all combinatorial and registered paths through the device, making a distinction between internal feedback and external feedback. A signal uses internal feedback when it is fed back into the switch matrix or block without having to go through the output buffer. The input register specifications are also reported as internal feedback. When a signal is fed back into the switch matrix after having gone through the output buffer, it is using external feedback.

The parameter, t_{BUF}, is defined as the time it takes to go from feedback through the output buffer to the I/O pad. If a signal goes to the internal feedback rather than to the I/O pad, the parameter designator is followed by an "i". By adding t_{BUF} to this internal parameter, the external parameter is derived. For example, $t_{PD} = t_{PDi} + t_{BUF}$. A diagram representing the modularized MACH 4 timing model is shown in Figure 15. Refer to the Technical Note entitled *MACH 4 Timing and High Speed Design* for a more detailed discussion about the timing parameters.

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Figure 15. MACH 4 Timing Model

SPEEDLOCKING FOR GUARANTEED FIXED TIMING

The MACH 4 architecture allows allocation of up to 20 product terms to an individual macrocell with the assistance of an XOR gate without incurring additional timing delays.

The design of the switch matrix and PAL blocks guarantee a fixed pin-to-pin delay that is independent of the logic required by the design. Other competitive CPLDs incur serious timing delays as product terms expand beyond their typical 4 or 5 product term limits. Speed *and* SpeedLocking combine to give designs easy access to the performance required in today's designs.

IEEE 1149.1-COMPLIANT BOUNDARY SCAN TESTABILITY

All MACH 4 devices, except the M4(LV)-128N/64, have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more complete board-level testing.

IEEE 1149.1-COMPLIANT IN-SYSTEM PROGRAMMING

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality, and the ability to make in-field modifications. All MACH 4 devices provide In-System Programming (ISP) capability through their Boundary ScanTest Access Ports. This capability has been implemented in a manner that ensures that the port remains compliant to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

MACH 4 devices can be programmed across the commercial temperature and voltage range. The PC-based LatticePRO software facilitates in-system programming of MACH 4 devices. LatticePRO takes the JEDEC file output produced by the design implementation software, along with information about the JTAG chain, and creates a set of vectors that are used to drive the JTAG chain. LatticePRO software can use these vectors to drive a JTAG chain via the parallel port of a PC. Alternatively, LatticePRO software can output files in formats understood by common automated test equipment. This equpment can then be used to program MACH 4 devices during the testing of a circuit board.

PCI COMPLIANT

MACH 4 devices in the -7/-10/-12 speed grades are compliant with the *PCI Local Bus Specification* version 2.1, published by the PCI Special Interest Group (SIG). The 5-V devices are fully PCI-compliant. The 3.3-V devices are mostly compliant but do not meet the PCI condition to clamp the inputs as they rise above V_{CC} because of their 5-V input tolerant feature.

SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS

Both the 3.3-V and 5-V V_{CC} MACH 4 devices are safe for mixed supply voltage system designs. The 5-V devices will not overdrive 3.3-V devices above the output voltage of 3.3 V, while they accept inputs from other 3.3-V devices. The 3.3-V device will accept inputs up to 5.5 V. Both the 5-V and 3.3-V versions have the same high-speed performance and provide easy-to-use mixed-voltage design capability.

BUS-FRIENDLY INPUTS AND I/OS

All MACH 4 devices have inputs and I/Os which feature the Bus-Friendly circuitry incorporating two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state. While it is good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from the input threshold voltage where noise can cause high-frequency switching. At power-up, the Bus-Friendly latches are reset to a logic level "1." For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice/Vantis Data Book CD-ROM or Lattice web site.

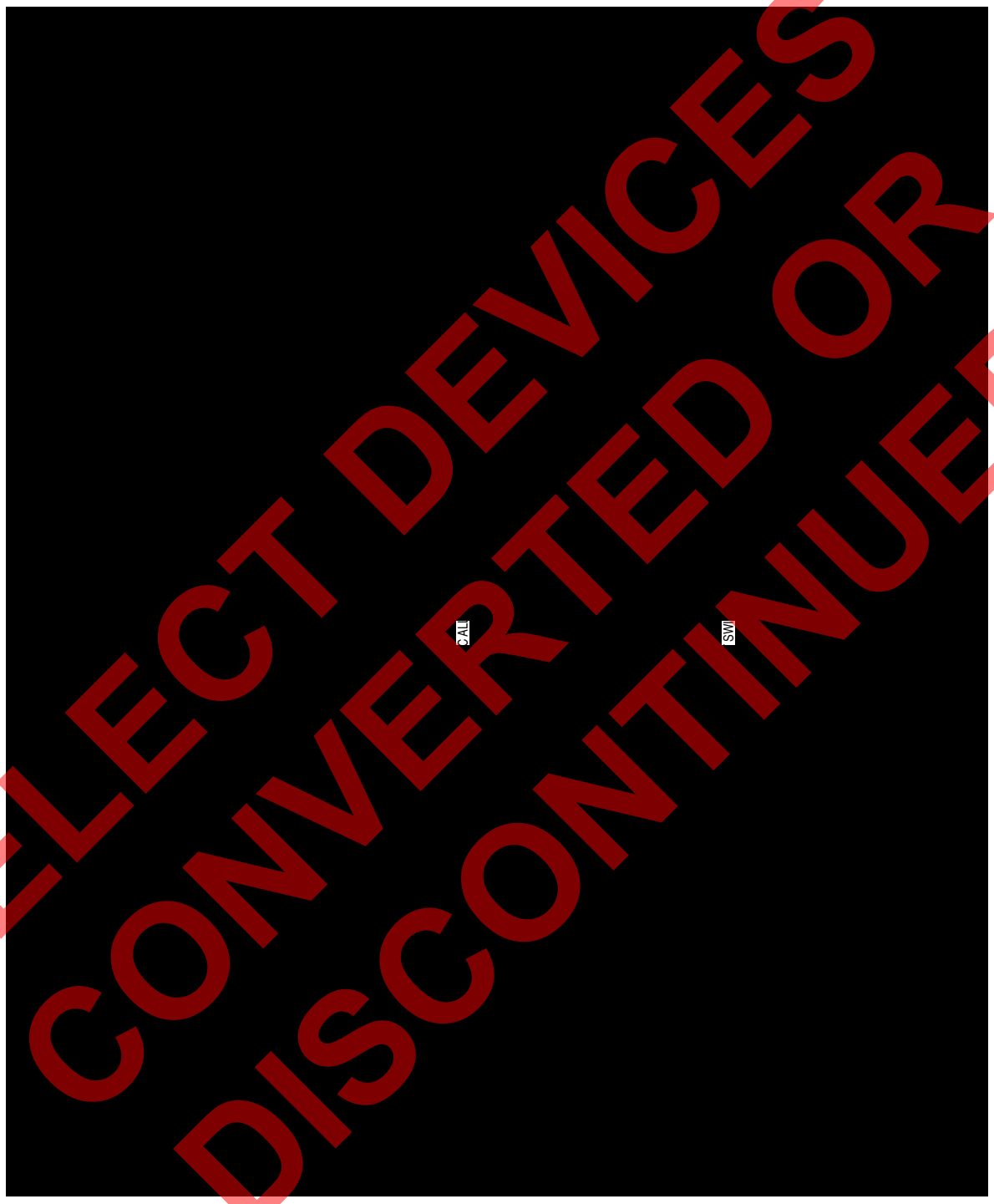
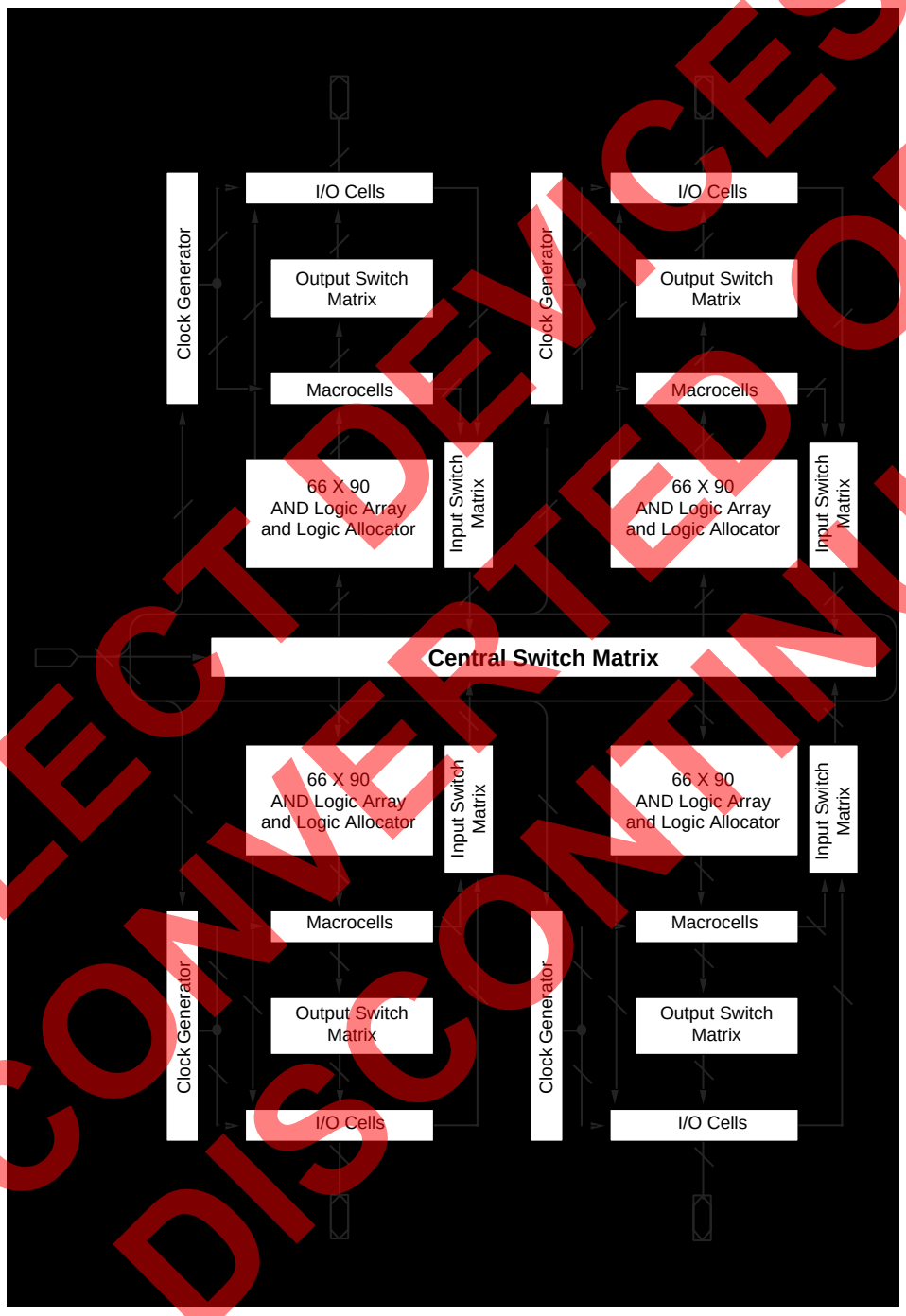


Figure 16. PAL Block for MACH 4 with 2:1 Macrocell - I/O Cell Ratio

BLOCK DIAGRAM – M4(LV)-64/32



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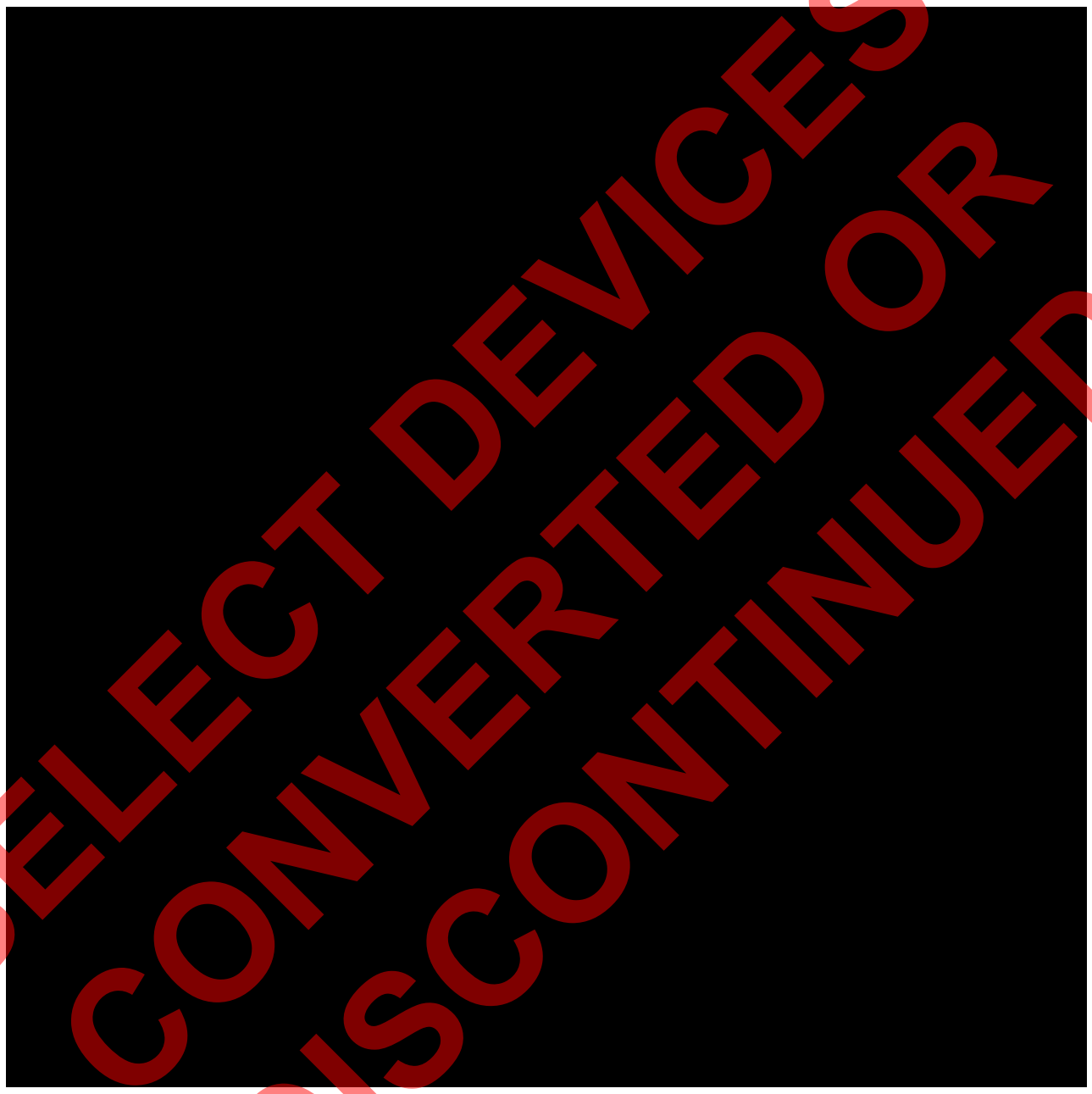
BLOCK DIAGRAM – M4(LV)-96/48

17466G-021

BLOCK DIAGRAM – M4(LV)-192/96



17466G-067

ABSOLUTE MAXIMUM RATINGS

M4

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature
with Power Applied . . . . . -55°C to +100°C

Device Junction Temperature . . . . . +130°C

Supply Voltage
with Respect to Ground . . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . . -0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (T_A = -40°C to +85°C). . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air. . . . . 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.75 V to +5.25 V

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air. . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +4.50 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

5-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	2.4			V
		I_{OH} = 0 mA, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL}			3.3	V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} (Note 1)			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 2)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 2)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 3)			–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max , V_{IN} = V_{IH} or V_{IL} (Note 3)			–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 4)	–30		–160	mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 64 mA.*
2. *These are absolute values with respect to device ground, and all overshoots due to system or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
4. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

44-PIN TQFP CONNECTION DIAGRAM (M4(LV)-32/32 AND M4(LV)-64/32)

Top View

44-Pin TQFP

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

100-PIN TQFP CONNECTION DIAGRAM (M4(LV)-96/48)

Top View

100-Pin TQFP

17466G-029

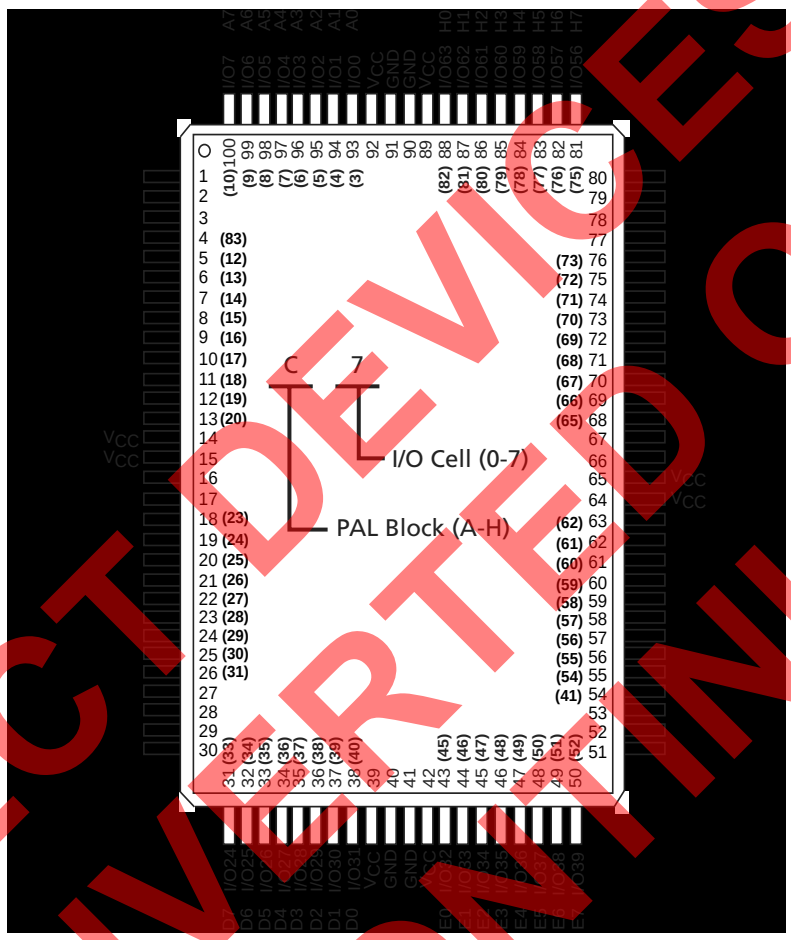
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
NC = No Connect
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

100-PIN PQFP CONNECTION DIAGRAM (M4(LV)-128/64)

Top View

100-Pin PQFP



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Note:
The numbers in parentheses reflect compatible pin numbers for 84-pin PLCC.

PIN DESIGNATIONS

I/CLK = Input or Clock
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out
TRST = Test Reset
ENABLE = Program

144-PIN TQFP CONNECTION DIAGRAM (M4(LV)-192/96)

Top View

144-Pin TQFP

17466G-033

PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

17466G-044

208-PIN PQFP CONNECTION DIAGRAM (M4(LV)-256/128)

Top View

208-Pin PQFP

17466G-044

17466H-066

256-BALL BGA CONNECTION DIAGRAM (M4LV-256/128)

Bottom View

256-Ball BGA

17466G-045

MACH 4 PRODUCT ORDERING INFORMATION

MACH 4 Devices Commercial & Industrial - 3.3V and 5V

Lattice/Vantis programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

M4- / 256 / 128 -7 Y C

FAMILY TYPE

M4- = MACH 4 Family (5-V V_{CC})
M4LV- = MACH 4 Family Low Voltage (3.3-V V_{CC})

MACROCELL DENSITY

32 = 32 Macrocells
64 = 64 Macrocells
96 = 96 Macrocells
128 = 128 Macrocells
128N = 128 Macrocells, Non-ISP
192 = 192 Macrocells
256 = 256 Macrocells

I/Os

/32 = 32 I/Os in 44-pin PLCC, 44-pin TQFP or 48-pin TQFP
/48 = 48 I/Os in 100-pin TQFP
/64 = 64 I/Os in 84-pin PLCC, 100-pin PQFP or 100-pin TQFP
/96 = 96 I/Os in 144-pin TQFP
/128 = 128 I/Os in 208-pin PQFP or 256-ball BGA

SPEED

-7 = 7.5 ns t_{PD}
-10 = 10 ns t_{PD}
-12 = 12 ns t_{PD}
-14 = 14 ns t_{PD}
-15 = 15 ns t_{PD}
-18 = 18 ns t_{PD}

PACKAGE TYPE

A = Ball Grid Array (BGA)
J = Plastic Leaded Chip Carrier (PLCC)
V = Thin Quad Flat Pack (TQFP)
Y = Plastic Quad Flat Pack (PQFP)

OPERATING CONDITIONS

C = Commercial (0°C to +70°C)
I = Industrial (-40°C to +85°C)

48 = 48-pin TQFP for M4(LV)-32/32 or M4(LV)-64/32

Valid Combinations		
M4-32/32	-7, -10, -12, -15	JC, VC, VC48
M4LV-32/32		JC, VC, VC48
M4-64/32		JC, VC, VC48
M4LV-64/32		JC, VC, VC48
M4-96/48		VC
M4LV-96/48		VC
M4-128/64		YC, VC
M4LV-128/64		YC, VC
M4-128N/64		JC
M4LV-128N/64		JC
M4-192/96		VC
M4LV-192/96		VC
M4-256/128		YC
M4LV-256/128		YC, AC

All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial speed grade is slower, i.e., M4-256/128-7YC-10YI

Valid Combinations		
M4-32/32	-10, -12, -14, -18	JI, VI, VI48
M4LV-32/32		JI, VI, VI48
M4-64/32		JI, VI, VI48
M4LV-64/32		JI, VI, VI48
M4-96/48		VI
M4LV-96/48		VI
M4-128/64		YI, VI
M4LV-128/64		YI, VI
M4-128N/64		JI
M4LV-128N/64		JI
M4-192/96		VI
M4LV-192/96		VI
M4-256/128		YI
M4LV-256/128		YI, AI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.