Lattice Semiconductor Corporation - M4-128N/64-14JI Datasheet

Welcome to E-XFL.COM

Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	14 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	128
Number of Gates	-
Number of I/O	64
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m4-128n-64-14ji

Product Line	Ordering Part Number	Product Status	Reference PCN
M4-64/32	M4-64/32-7JC	Converted to M4A5	Contact pcn@latticesemi.com for more info.
	M4-64/32-10JC		
	M4-64/32-12JC		
	M4-64/32-15JC		
	M4-64/32-10JI		
	M4-64/32-12JI		
	M4-64/32-14JI		
	M4-64/32-18JI		
	M4-64/32-7VC		
	M4-64/32-10VC		
	M4-64/32-12VC		
	M4-64/32-15VC		
	M4-64/32-10VI		
	M4-64/32-12VI		
	M4-64/32-14VI		
	M4-64/32-18VI		
	M4-64/32-7VC48		
	M4-64/32-10VC48		
	M4-64/32-12VC48		
	M4-64/32-15VC48		
	M4-64/32-10VI48		
	M4-64/32-12VI48		
	M4-64/32-14VI48		
	M4-64/32-18VI48		
M4-96/48	M4-96/48-7VC	Convert to M4A5	Contact pcn@latticesemi.com for more info.
	M4-96/48-10VC		
	M4-96/48-12VC		
	M4-96/48-15VC		
	M4-96/48-10VI		
	M4-96/48-12VI		
	M4-96/48-14VI		
	M4-96/48-18VI		
M4-128/64	M4-128/64-7YC	Convert to M4A5	Contact pcn@latticesemi.com for more info.
	M4-128/64-10YC		
	M4-128/64-12YC		
	M4-128/64-15YC		
	M4-128/64-10YI		
	M4-128/64-12YI		
	M4-128/64-14YI		
	M4-128/64-18YI		

5555 N.E. Moore Ct. ● Hillsboro, Oregon 97124-6421 ● Phone (503) 268-8000 ● FAX (503) 268-8347
Internet: http://www.latticesemi.com

Product Line	Ordering Part Number	Product Status	Reference PCN
M4LV-32/32 (Cont'd)	M4LV-32/32-7VC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-32/32-10VC		
	M4LV-32/32-12VC		
	M4LV-32/32-15VC		
	M4LV-32/32-10VI		
	M4LV-32/32-12VI		
	M4LV-32/32-14VI		
	M4LV-32/32-18VI		
	M4LV-32/32-7VC48		
	M4LV-32/32-10VC48		
	M4LV-32/32-12VC48		
	M4LV-32/32-15VC48		
	M4LV-32/32-10VI48		
	M4LV-32/32-12VI48		
	M4LV-32/32-14VI48		
	M4LV-32/32-18VI48		
M4LV-64/32	M4LV-64/32-7JC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-64/32-10JC		
	M4LV-64/32-12JC		
	M4LV-64/32-15JC		
	M4LV-64/32-10JI		
	M4LV-64/32-12JI		
	M4LV-64/32-14JI		
	M4LV-64/32-18JI		
	M4LV-64/32-7VC		
	M4LV-64/32-10VC		
	M4LV-64/32-12VC		
	M4LV-64/32-15VC		
	M4LV-64/32-10VI		
	M4LV-64/32-12VI		
	M4LV-64/32-14VI		
	M4LV-64/32-18VI		
	M4LV-64/32-7VC48		
	M4LV-64/32-10VC48		
	M4LV-64/32-12VC48		
	M4LV-64/32-15VC48		
	M4LV-64/32-10VI48		
	M4LV-64/32-12VI48		
	M4LV-64/32-14VI48		
	M4LV-64/32-18VI48		

Product Line	Ordering Part Number	Product Status	Reference PCN
M4LV-96/48	M4LV-96/48-7VC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-96/48-10VC		
	M4LV-96/48-12VC		
	M4LV-96/48-15VC		
	M4LV-96/48-10VI		
	M4LV-96/48-12VI		
	M4LV-96/48-14VI		
	M4LV-96/48-18VI		
M4LV-128/64	M4LV-128/64-7YC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-128/64-10YC		
	M4LV-128/64-12YC		
	M4LV-128/64-15YC		
	M4LV-128/64-10YI		
	M4LV-128/64-12YI		
	M4LV-128/64-14YI		
	M4LV-128/64-18YI		
	M4LV-128/64-7VC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-128/64-10VC		
	M4LV-128/64-12VC		
	M4LV-128/64-15VC		
	M4LV-128/64-10VI		
	M4LV-128/64-12VI		
	M4LV-128/64-14VI		
	M4LV-128/64-18VI		
M4LV-128N/64	M4LV-128N/64-7JC	**Discontinued**	PCN#09-10
	M4LV-128N/64-10JC		
	M4LV-128N/64-12JC		
	M4LV-128N/64-15JC		
	M4LV-128N/64-10JI		
	M4LV-128N/64-12JI		
	M4LV-128N/64-14JI		
	M4LV-128N/64-18JI		
M4LV-192/96	M4LV-192/96-7VC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-192/96-10VC		
	M4LV-192/96-12VC		
	M4LV-192/96-15VC		
	M4LV-192/96-10VI		
	M4LV-192/96-12VI		
	M4LV-192/96-14VI		
	M4LV-192/96-18VI		

FUNCTIONAL DESCRIPTION

The fundamental architecture of MACH 4 devices (Figure 1) consists of multiple, optimized PAL® blocks interconnected by a central switch matrix. The central switch matrix allows communication between PAL blocks and routes inputs to the PAL blocks. Together, the PAL blocks and central switch matrix allow the logic designer to create large designs in a single device instead of having to use multiple devices.

The key to being able to make effective use of these devices lies in the interconnect schemes. In MACH 4 architecture, the macrocells are flexibly coupled to the product terms through the logic allocator, and the I/O pins are flexibly coupled to the macrocells due to the output switch matrix. In addition, more input routing options are provided by the input switch matrix. These resources provide the flexibility needed to fit designs efficiently.

Figure 1. MACH 4 Block Diagram and PAL Block Structure

Notes:

1. *16 for MACH 4 devices with 1:1 macrocell-I/O cell ratio (see next page).*
2. *Block clocks do not go to I/O cells in M4(LV)-32/32.*
3. *M4(LV)-192/96 and M4(LV)-256/128 have dedicated clock pins which cannot be used as inputs and do not connect to the central switch matrix.*

Product-Term Array

The product-term array consists of a number of product terms that form the basis of the logic being implemented. The inputs to the AND gates come from the central switch matrix (Table 5), and are provided in both true and complement forms for efficient logic implementation.

Table 5. PAL Block Inputs

Device	Number of Inputs to PAL Block
M4-32/32 and M4LV-32/32	33
M4-64/32 and M4LV-64/32	33
M4-96/48 and M4LV-96/48	33
M4-128/64 and M4LV-128/64	33
M4-128N/64 and M4LV-128N/64	33
M4-192/96 and M4LV-192/96	34
M4-256/128 and M4LV-256/128	34

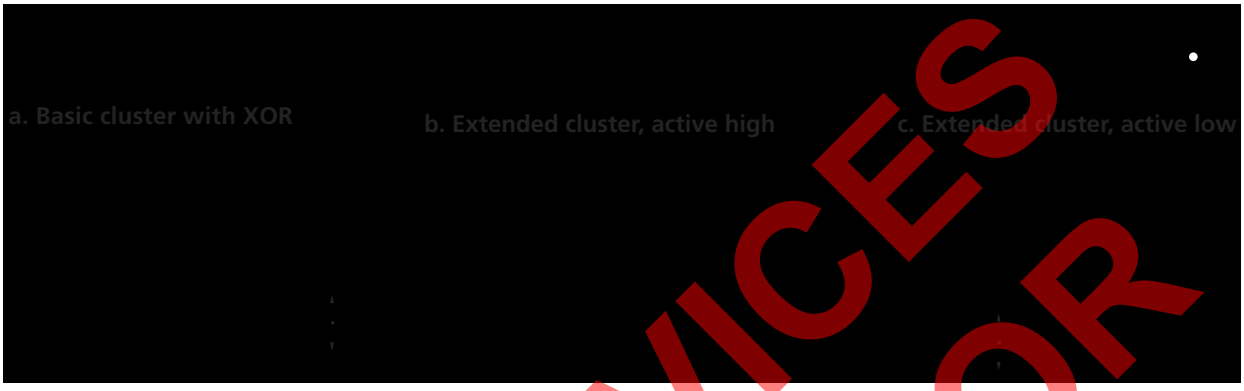
Logic Allocator

Within the logic allocator, product terms are allocated to macrocells in "product term clusters." The availability and distribution of product term clusters are automatically considered by the software as it fits functions within a PAL block. The size of a product term cluster has been optimized to provide high utilization of product terms, making complex functions using many product terms possible. Yet when few product terms are used, there will be a minimal number of unused—or wasted—product terms left over. The product term clusters available to each macrocell within a PAL block are shown in Tables 6 and 7.

Each product term cluster is associated with a macrocell. The size of a cluster depends on the configuration of the associated macrocell. When the macrocell is used in synchronous mode (Figure 2a), the basic cluster has 4 product terms. When the associated macrocell is used in asynchronous mode (Figure 2b), the cluster has 2 product terms. Note that if the product term cluster is routed to a different macrocell, the allocator configuration is not determined by the mode of the macrocell actually being driven. The configuration is always set by the mode of the macrocell that the cluster will drive if not routed away, regardless of the actual routing.

In addition, there is an extra product term that can either join the basic cluster to give an extended cluster, or drive the second input of an exclusive-OR gate in the signal path. If included with the basic cluster, this provides for up to 20 product terms on a synchronous function that uses four extended 5-product-term clusters. A similar asynchronous function can have up to 18 product terms.

When the extra product term is used to extend the cluster, the value of the second XOR input can be programmed as a 0 or a 1, giving polarity control. The possible configurations of the logic allocator are shown in Figures 3 and 4.



17466G-007

Figure 3. Logic Allocator Configurations: Synchronous Mode

17466G-008

Figure 4. Logic Allocator Configurations: Asynchronous Mode

Note that the configuration of the logic allocator has absolutely no impact on the speed of the signal. All configurations have the same delay. This means that designers do not have to decide between optimizing resources or speed; both can be optimized.

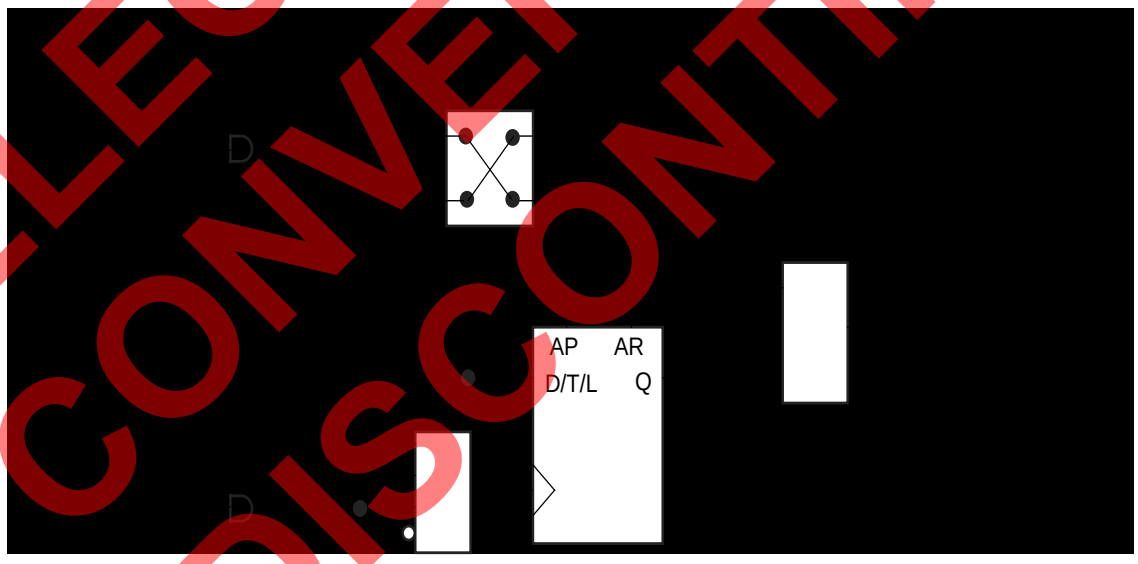
If not used in the cluster, the extra product term can act in conjunction with the basic cluster to provide XOR logic for such functions as data comparison, or it can work with the D-,T-type flip-flop to provide for J-K, and S-R register operation. In addition, if the basic cluster is routed to another macrocell, the extra product term is still available for logic. In this case, the first XOR input will be a logic 0. This circuit has the flexibility to route product terms elsewhere without giving up the use of the macrocell.

Product term clusters do not "wrap" around a PAL block. This means that the macrocells at the ends of the block have fewer product terms available.

Macrocell

The macrocell consists of a storage element, routing resources, a clock multiplexer, and initialization control. The macrocell has two fundamental modes: synchronous and asynchronous (Figure 5). The mode chosen only affects clocking and initialization in the macrocell.

a. Synchronous mode



b. Asynchronous mode

17466G-010

Figure 5. Macrocell

In either mode, a combinatorial path can be used. For combinatorial logic, the synchronous mode will generally be used, since it provides more product terms in the allocator.

Table 8. Register/Latch Operation

Configuration	Input(s)	CLK/LE [1]	Q+
D-type Register	D=X	0, 1, ↓ (↑)	Q
	D=0	↑ (↓)	0
	D=1	↑ (↓)	1
T-type Register	T=X	0, 1, ↓ (↑)	Q
	T=0	↑ (↓)	Q
	T=1	↑ (↓)	$\overline{Q}$
D-type Latch	D=X	1 (0)	Q
	D=0	0 (1)	0
	D=1	0 (1)	1

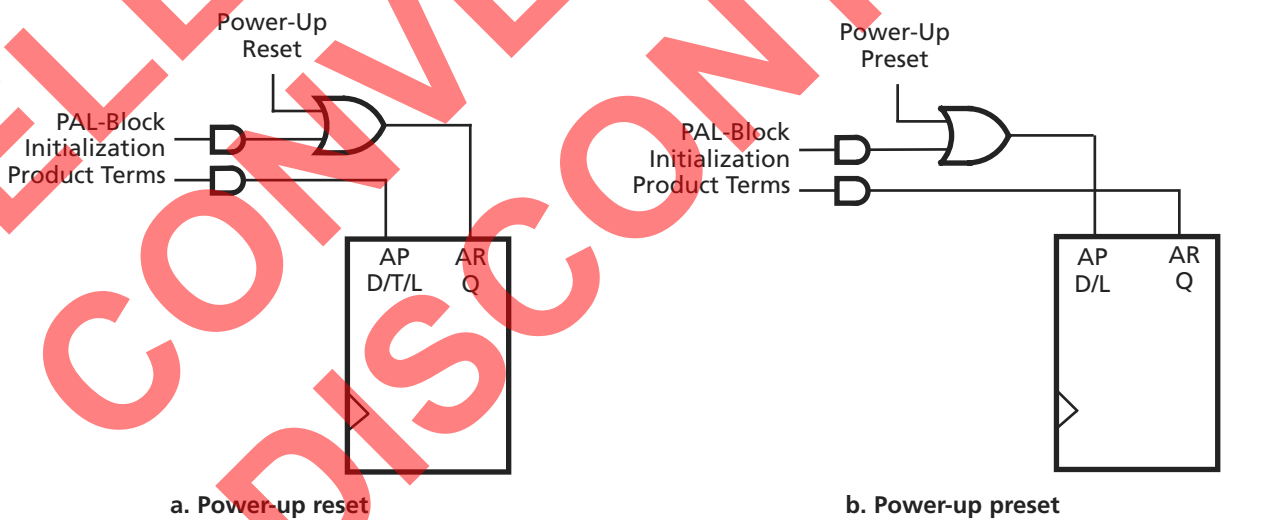
Note:

1. Polarity of CLK/LE can be programmed

Although the macrocell shows only one input to the register, the XOR gate in the logic allocator allows the D-, T-type register to emulate J-K, and S-R behavior. In this case, the available product terms are divided between J and K (or S and R). When configured as J-K, S-R, or T-type, the extra product term must be used on the XOR gate input for flip-flop emulation. In any register type, the polarity of the inputs can be programmed.

The clock input to the flip-flop can select any of the four PAL block clocks in synchronous mode, with the additional choice of either polarity of an individual product term clock in the asynchronous mode.

The initialization circuit depends on the mode. In synchronous mode (Figure 7), asynchronous reset and preset are provided, each driven by a product term common to the entire PAL block.



a. Power-up reset

b. Power-up preset

17466G-012

17466G-013

Figure 7. Synchronous Mode Initialization Configurations

Table 10. Output Switch Matrix Combinations for MACH 4 Devices with 2:1 Macrocell-I/O Cell Ratio

Macrocell	Routable to I/O Cells
M0, M1	I/00, I/05, I/06, I/07
M2, M3	I/00, I/01, I/06, I/07
M4, M5	I/00, I/01, I/02, I/07
M6, M7	I/00, I/01, I/02, I/03
M8, M9	I/01, I/02, I/03, I/04
M10, M11	I/02, I/03, I/04, I/05
M12, M13	I/03, I/04, I/05, I/06
M14, M15	I/04, I/05, I/06, I/07

I/O Cell	Available Macrocells
I/00	M0, M1, M2, M3, M4, M5, M6, M7
I/01	M2, M3, M4, M5, M6, M7, M8, M9
I/02	M4, M5, M6, M7, M8, M9, M10, M11
I/03	M6, M7, M8, M9, M10, M11, M12, M13
I/04	M8, M9, M10, M11, M12, M13, M14, M15
I/05	M0, M1, M10, M11, M12, M13, M14, M15
I/06	M0, M1, M2, M3, M12, M13, M14, M15
I/07	M0, M1, M2, M3, M4, M5, M14, M15

Table 11. Output Switch Matrix Combinations for M4(LV)-32/32

Macrocell	Routable to I/O Cells
M0, M1, M2, M3, M4, M5, M6, M7	I/00, I/01, I/02, I/03, I/04, I/05, I/06, I/07
M8, M9, M10, M11, M12, M13, M14, M15	I/08, I/09, I/010, I/011, I/012, I/013, I/014, I/015

I/O Cell	Available Macrocells
I/00, I/01, I/02, I/03, I/04, I/05, I/06, I/07	M0, M1, M2, M3, M4, M5, M6, M7
I/08, I/09, I/010, I/011, I/012, I/013, I/014, I/015	M8, M9, M10, M11, M12, M13, M14, M15

IEEE 1149.1-COMPLIANT BOUNDARY SCAN TESTABILITY

All MACH 4 devices, except the M4(LV)-128N/64, have boundary scan cells and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more complete board-level testing.

IEEE 1149.1-COMPLIANT IN-SYSTEM PROGRAMMING

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality, and the ability to make in-field modifications. All MACH 4 devices provide In-System Programming (ISP) capability through their Boundary ScanTest Access Ports. This capability has been implemented in a manner that ensures that the port remains compliant to the IEEE 1149.1 standard. By using IEEE 1149.1 as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

MACH 4 devices can be programmed across the commercial temperature and voltage range. The PC-based LatticePRO software facilitates in-system programming of MACH 4 devices. LatticePRO takes the JEDEC file output produced by the design implementation software, along with information about the JTAG chain, and creates a set of vectors that are used to drive the JTAG chain. LatticePRO software can use these vectors to drive a JTAG chain via the parallel port of a PC. Alternatively, LatticePRO software can output files in formats understood by common automated test equipment. This equpment can then be used to program MACH 4 devices during the testing of a circuit board.

PCI COMPLIANT

MACH 4 devices in the -7/-10/-12 speed grades are compliant with the *PCI Local Bus Specification* version 2.1, published by the PCI Special Interest Group (SIG). The 5-V devices are fully PCI-compliant. The 3.3-V devices are mostly compliant but do not meet the PCI condition to clamp the inputs as they rise above V_{CC} because of their 5-V input tolerant feature.

SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS

Both the 3.3-V and 5-V V_{CC} MACH 4 devices are safe for mixed supply voltage system designs. The 5-V devices will not overdrive 3.3-V devices above the output voltage of 3.3 V, while they accept inputs from other 3.3-V devices. The 3.3-V device will accept inputs up to 5.5 V. Both the 5-V and 3.3-V versions have the same high-speed performance and provide easy-to-use mixed-voltage design capability.

BUS-FRIENDLY INPUTS AND I/OS

All MACH 4 devices have inputs and I/Os which feature the Bus-Friendly circuitry incorporating two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state. While it is good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from the input threshold voltage where noise can cause high-frequency switching. At power-up, the Bus-Friendly latches are reset to a logic level "1." For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice/Vantis Data Book CD-ROM or Lattice web site.

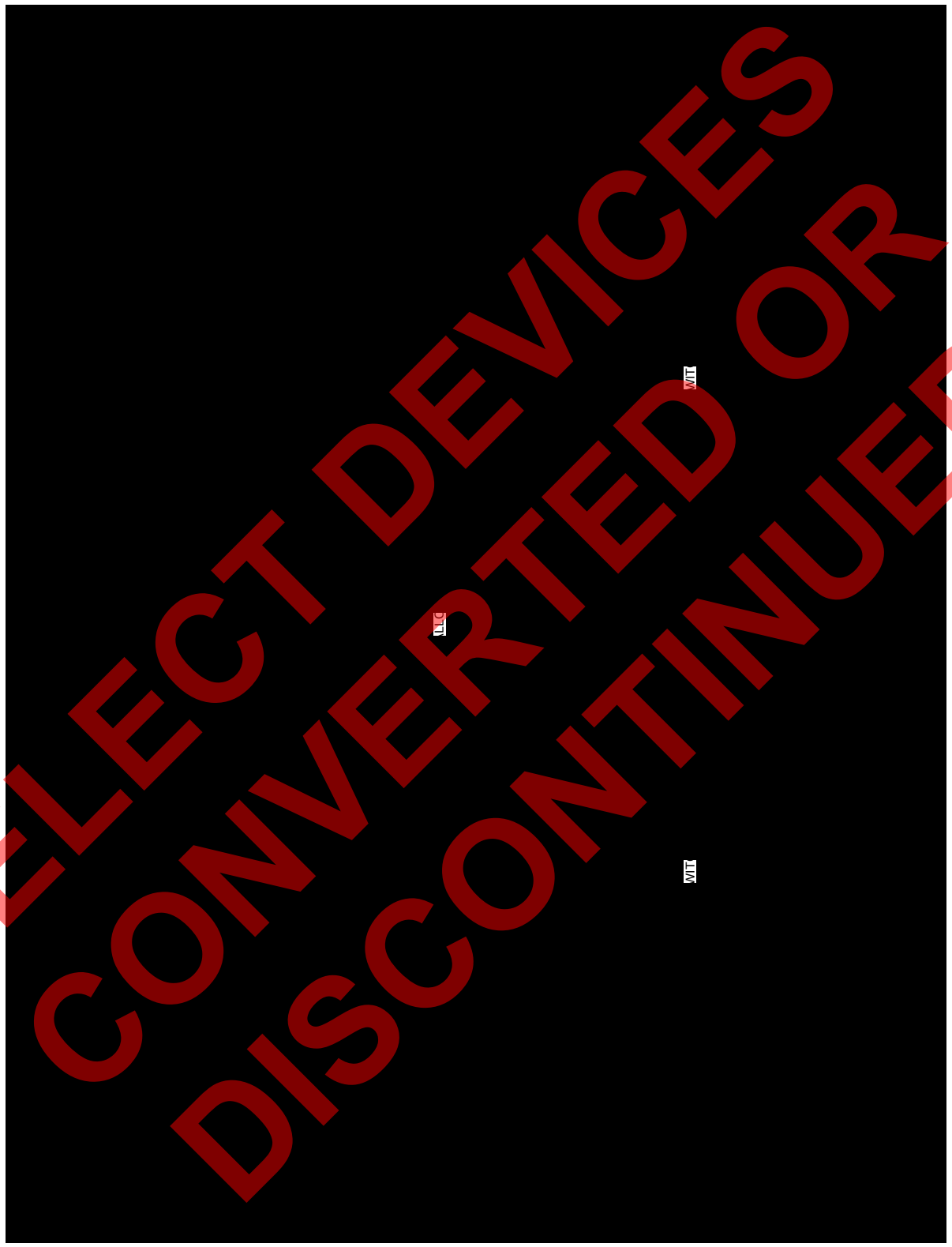
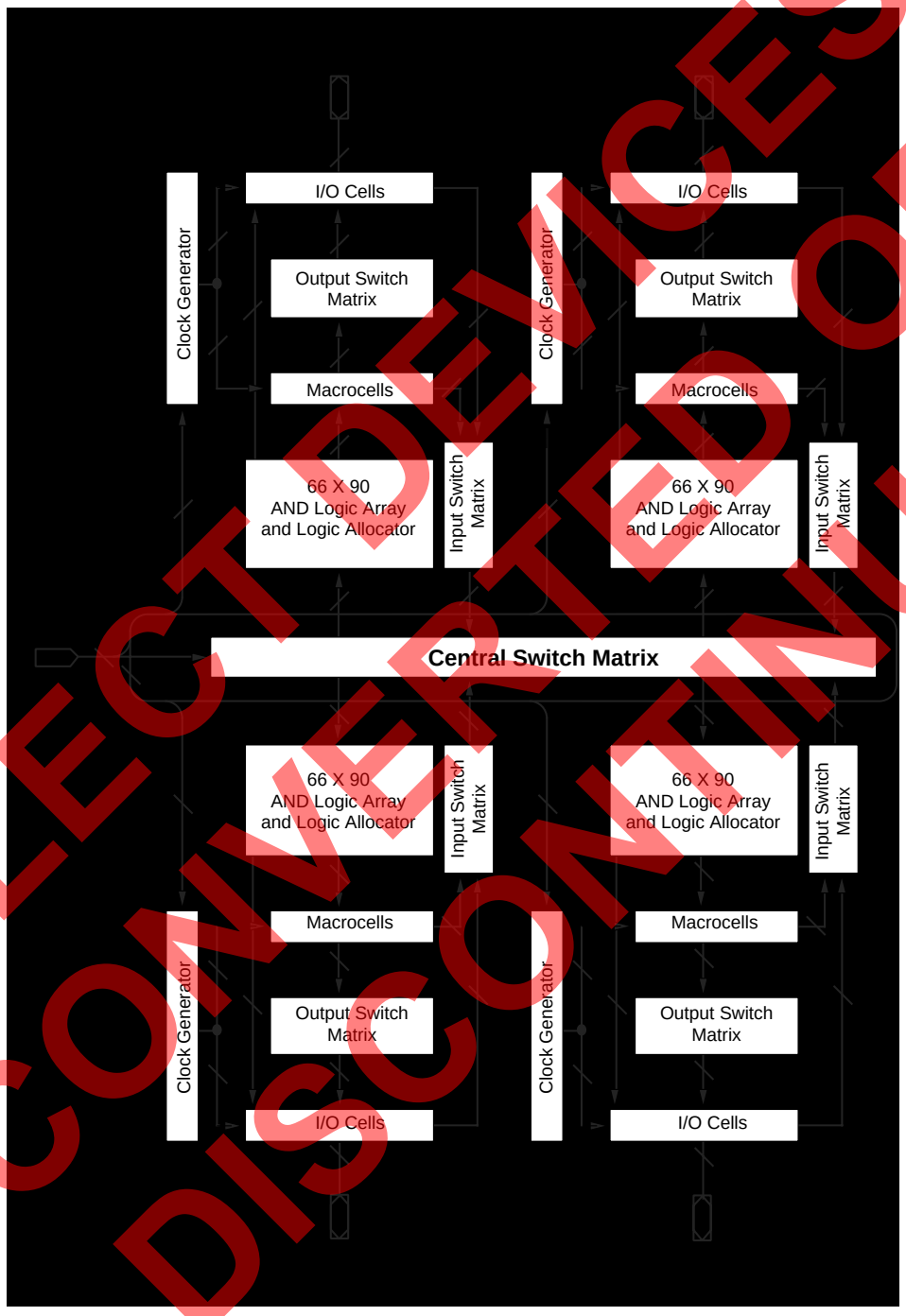


Figure 17. PAL Block for M4(LV)-32/32

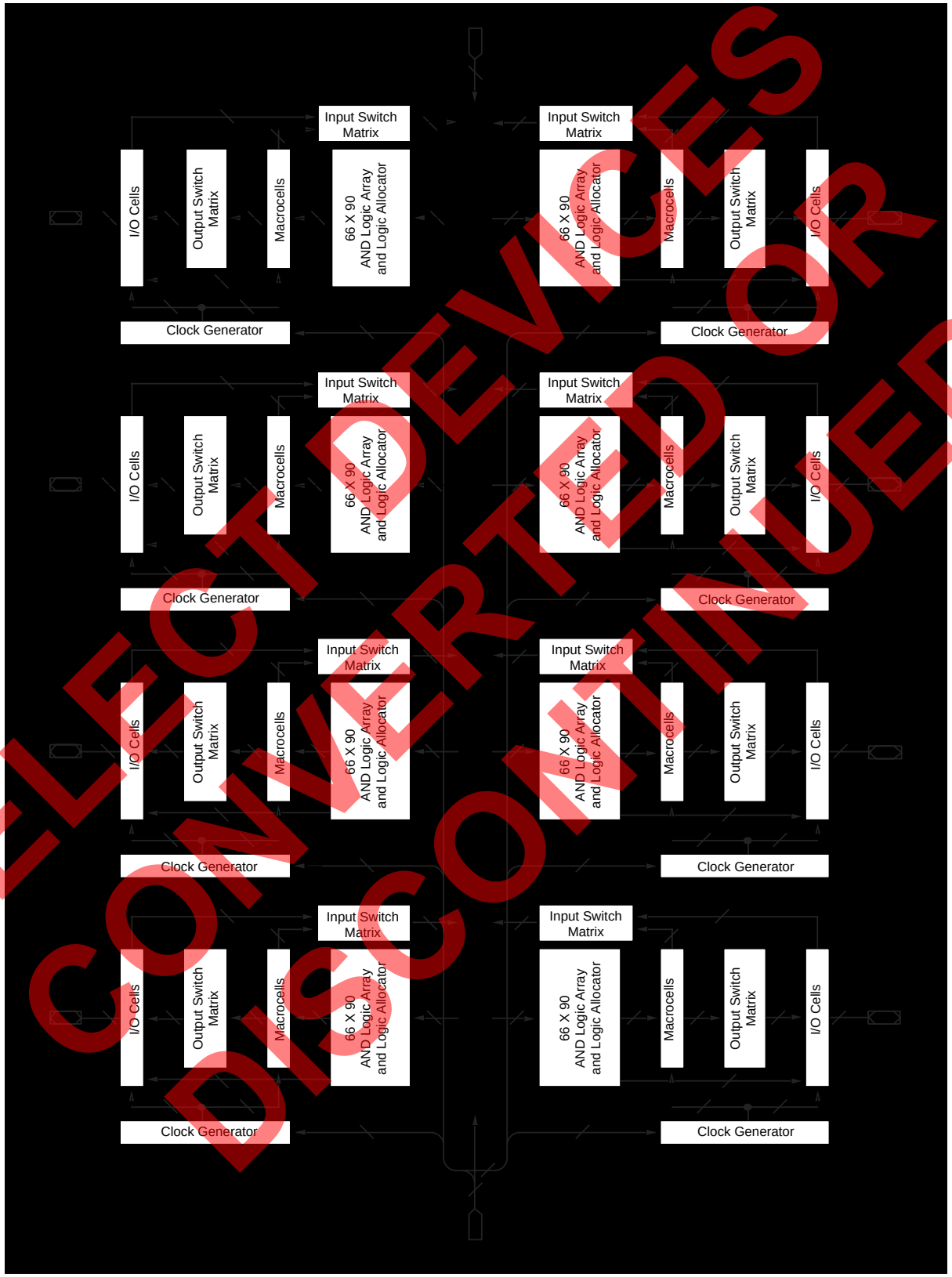
17466H-042

BLOCK DIAGRAM – M4(LV)-64/32



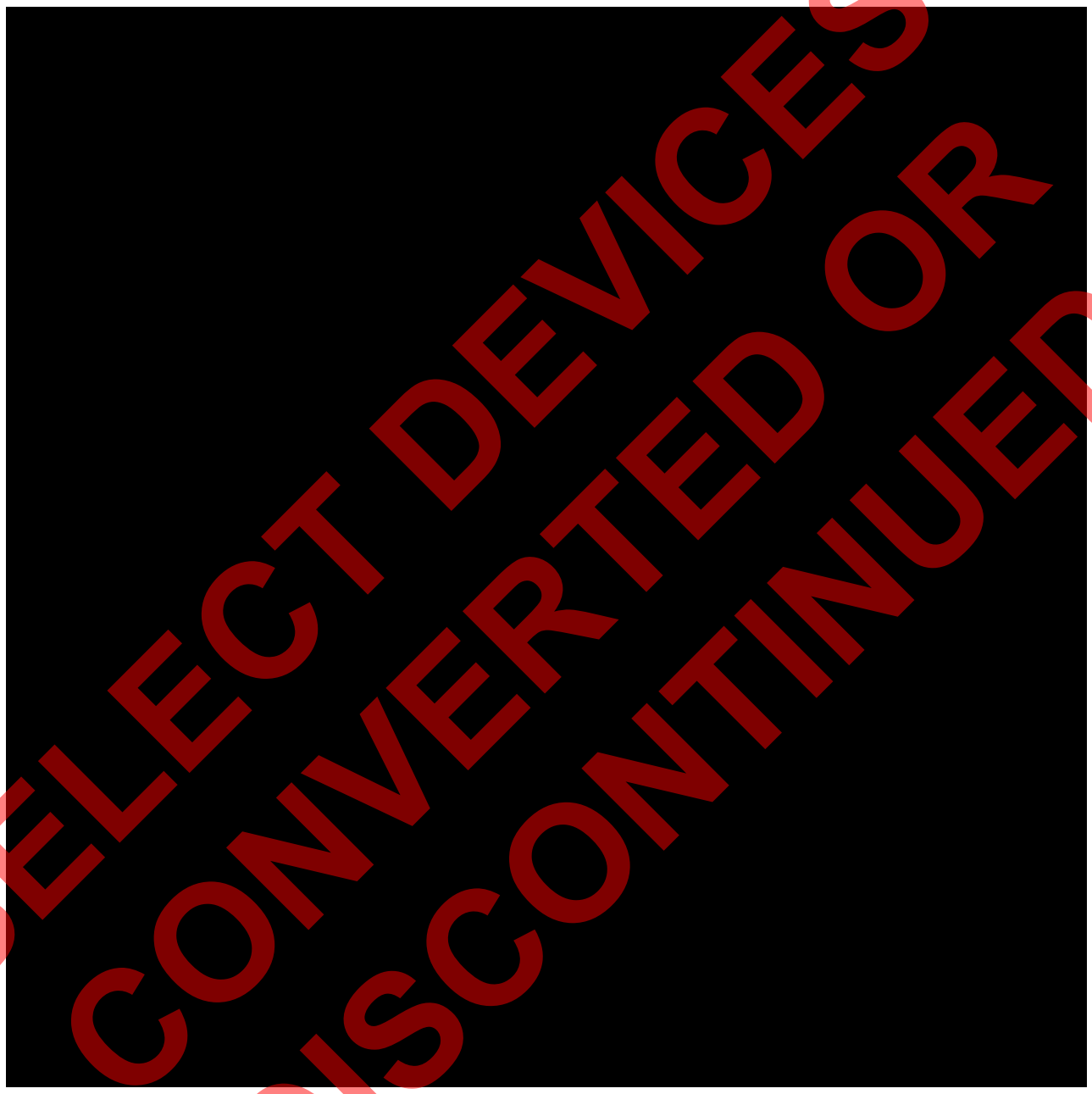
17466H-020

BLOCK DIAGRAM – M4(LV)-128N/64 AND M4(LV)-128/64



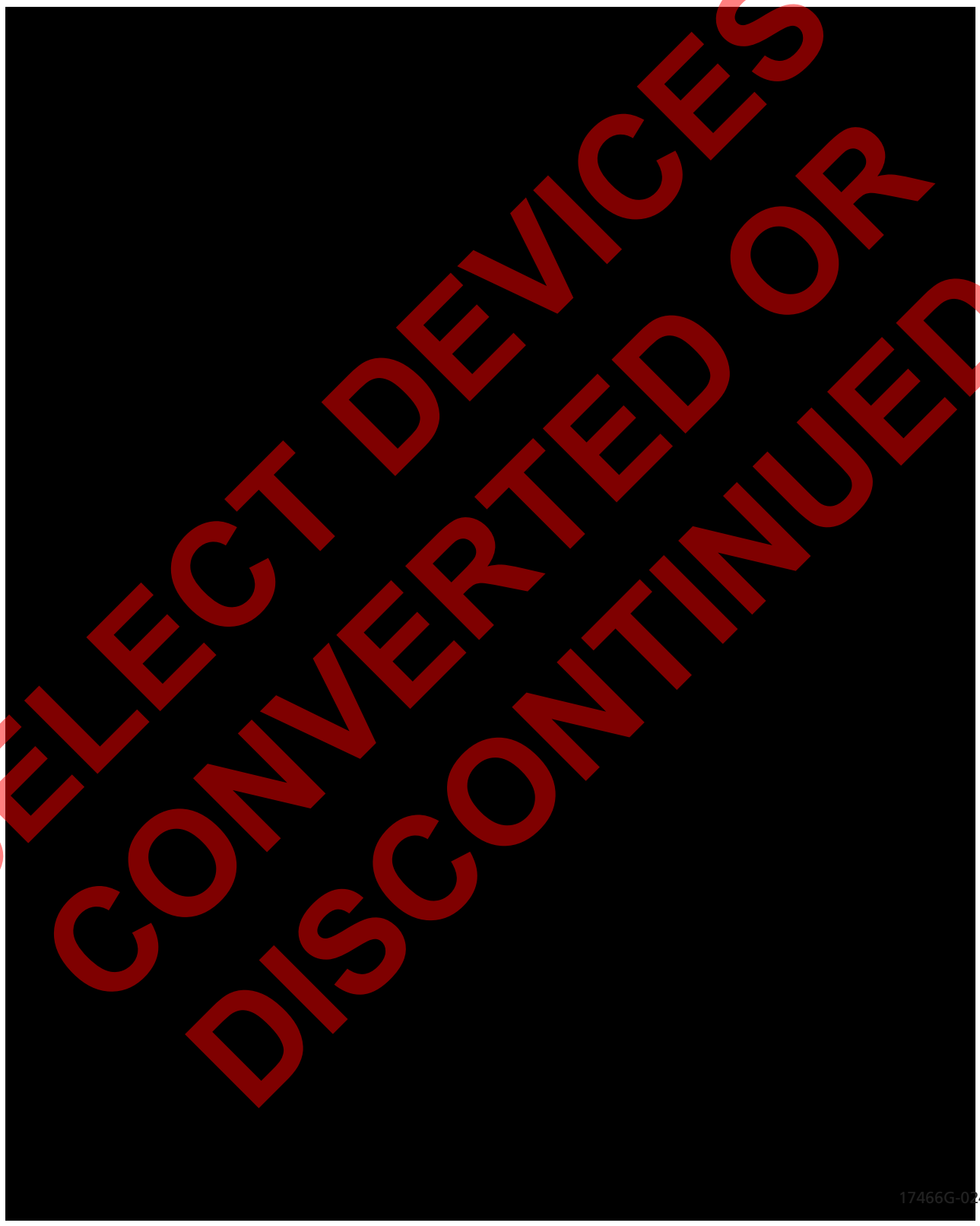
17466H-022

BLOCK DIAGRAM – M4(LV)-192/96



17466G-067

BLOCK DIAGRAM – M4(LV)-256/128



ABSOLUTE MAXIMUM RATINGS

M4LV

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature
with Power Applied . . . . . -55°C to +100°C

Device Junction Temperature . . . . . +130°C

Supply Voltage
with Respect to Ground . . . . . -0.5 V to +4.5 V

DC Input Voltage . . . . . -0.5 V to 6.0 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (T_A = -40°C to +85°C). . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +3.0 V to +3.6 V

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

3.3-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = –100 µA	V_{CC} – 0.2			V
			I_{OH} = –3.2 mA	2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} (Note 1)	I_{OL} = 100 µA			0.2	V
			I_{OL} = 24 mA			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs		2.0		5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs		–0.3		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 3.6 V, V_{CC} = Max (Note 2)				5	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)				–5	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 3.6 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)				5	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)				–5	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–15		–160	mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 64 mA.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.*

MACH 4 TIMING PARAMETERS OVER OPERATING RANGES[1]

		-7		-10		-12		-14		-15		-18		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Combinatorial Delay:														
t_{PDi}	Internal combinatorial propagation delay		5.5		8.0		10.0		12.0		13.0		16.0	ns
t_{PD}	Combinatorial propagation delay		7.5		10.0		12.0		14.0		15.0		18.0	ns
Registered Delays:														
t_{SS}	Synchronous clock setup time, D-type register	5.5		6.0		7.0		10.0		10.0		12.0		ns
t_{SST}	Synchronous clock setup time, T-type register	6.5		7.0		8.0		11.0		11.0		13.0		ns
t_{SA}	Asynchronous clock setup time, D-type register	3.5		4.0		5.0		8.0		8.0		10.0		ns
t_{SAT}	Asynchronous clock setup time, T-type register	4.5		5.0		6.0		9.0		9.0		11.0		ns
t_{HS}	Synchronous clock hold time	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{HA}	Asynchronous clock hold time	3.5		4.0		5.0		8.0		8.0		10.0		ns
t_{COSi}	Synchronous clock to internal output		3.5		4.5		6.0		8.0		8.0		10.0	ns
t_{COS}	Synchronous clock to output		5.5		6.5		8.0		10.0		10.0		12.0	ns
t_{COAi}	Asynchronous clock to internal output		7.5		10.0		12.0		16.0		16.0		18.0	ns
t_{COA}	Asynchronous clock to output		9.5		12.0		14.0		18.0		18.0		20.0	ns
Latched Delays:														
t_{SSL}	Synchronous Latch setup time	6.0		7.0		8.0		10.0		10.0		12.0		ns
t_{SAL}	Asynchronous Latch setup time	4.0		4.0		5.0		8.0		8.0		10.0		ns
t_{HSL}	Synchronous Latch hold time	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{HAL}	Asynchronous Latch hold time	4.0		4.0		5.0		8.0		8.0		10.0		ns
t_{PDLi}	Transparent latch to internal output		8.0		10.0		12.0		15.0		15.0		18.0	ns
t_{PDL}	Propagation delay through transparent latch to output		10.0		12.0		14.0		17.0		17.0		20.0	ns
t_{GOSi}	Synchronous Gate to internal output		4.0		5.5		8.0		9.0		9.0		10.0	ns
t_{GOS}	Synchronous Gate to output		6.0		7.5		10.0		11.0		11.0		12.0	ns
t_{GOAi}	Asynchronous Gate to internal output		9.0		11.0		14.0		17.0		17.0		20.0	ns
t_{GOA}	Asynchronous Gate to output		11.0		13.0		16.0		19.0		19.0		22.0	ns
Input Register Delays:														
t_{SIRS}	Input register setup time	2.0		2.0		2.0		2.0		2.0		2.0		ns
t_{HIRS}	Input register hold time	3.0		3.0		3.0		4.0		4.0		4.0		ns
t_{ICOSi}	Input register clock to internal feedback		3.5		4.5		6.0		6.0		6.0		6.0	ns
Input Latch Delays:														
t_{SIL}	Input latch setup time	2.0		2.0		2.0		2.0		2.0		2.0		ns
t_{HIL}	Input latch hold time	3.0		3.0		3.0		4.0		4.0		4.0		ns
t_{IGOSi}	Input latch gate to internal feedback		4.0		4.0		4.0		5.0		5.0		6.0	ns
t_{PDILi}	Transparent input latch to internal feedback		2.0		2.0		2.0		2.0		2.0		2.0	ns
Input Register Delays with ZHT Option:														
t_{SIRZ}	Input register setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0		ns
t_{HIRZ}	Input register hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0		ns

44-PIN TQFP CONNECTION DIAGRAM (M4(LV)-32/32 AND M4(LV)-64/32)

Top View

44-Pin TQFP

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

48-PIN TQFP CONNECTION DIAGRAM (M4(LV)-32/32 AND M4(LV)-64/32)

Top View

48-Pin TQFP

17466G-028

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I/O = Input/Output
V_{CC} = Supply Voltage
NC = No Connect
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

100-PIN TQFP CONNECTION DIAGRAM (M4(LV)-128/64)

Top View

100-Pin TQFP

17466G-032

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out
TRST = Test Reset
ENABLE = Program