Lattice Semiconductor Corporation - M4-128N/64-18JI Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	18 ns
Voltage Supply - Internal	4.5V ~ 5.5V
Number of Logic Elements/Blocks	-
Number of Macrocells	128
Number of Gates	-
Number of I/O	64
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m4-128n-64-18ji

Product Line	Ordering Part Number	Product Status	Reference PCN
M4LV-32/32 (Cont'd)	M4LV-32/32-7VC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-32/32-10VC		
	M4LV-32/32-12VC		
	M4LV-32/32-15VC		
	M4LV-32/32-10VI		
	M4LV-32/32-12VI		
	M4LV-32/32-14VI		
	M4LV-32/32-18VI		
	M4LV-32/32-7VC48		
	M4LV-32/32-10VC48		
	M4LV-32/32-12VC48		
	M4LV-32/32-15VC48		
	M4LV-32/32-10VI48		
	M4LV-32/32-12VI48		
	M4LV-32/32-14VI48		
	M4LV-32/32-18VI48		
M4LV-64/32	M4LV-64/32-7JC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-64/32-10JC		
	M4LV-64/32-12JC		
	M4LV-64/32-15JC		
	M4LV-64/32-10JI		
	M4LV-64/32-12JI		
	M4LV-64/32-14JI		
	M4LV-64/32-18JI		
	M4LV-64/32-7VC		
	M4LV-64/32-10VC		
	M4LV-64/32-12VC		
	M4LV-64/32-15VC		
	M4LV-64/32-10VI		
	M4LV-64/32-12VI		
	M4LV-64/32-14VI		
	M4LV-64/32-18VI		
	M4LV-64/32-7VC48		
	M4LV-64/32-10VC48		
	M4LV-64/32-12VC48		
	M4LV-64/32-15VC48		
	M4LV-64/32-10VI48		
	M4LV-64/32-12VI48		
	M4LV-64/32-14VI48		
	M4LV-64/32-18VI48		

FUNCTIONAL DESCRIPTION

The fundamental architecture of MACH 4 devices (Figure 1) consists of multiple, optimized PAL® blocks interconnected by a central switch matrix. The central switch matrix allows communication between PAL blocks and routes inputs to the PAL blocks. Together, the PAL blocks and central switch matrix allow the logic designer to create large designs in a single device instead of having to use multiple devices.

The key to being able to make effective use of these devices lies in the interconnect schemes. In MACH 4 architecture, the macrocells are flexibly coupled to the product terms through the logic allocator, and the I/O pins are flexibly coupled to the macrocells due to the output switch matrix. In addition, more input routing options are provided by the input switch matrix. These resources provide the flexibility needed to fit designs efficiently.

Figure 1. MACH 4 Block Diagram and PAL Block Structure

Notes:

1. *16 for MACH 4 devices with 1:1 macrocell-I/O cell ratio (see next page).*
2. *Block clocks do not go to I/O cells in M4(LV)-32/32.*
3. *M4(LV)-192/96 and M4(LV)-256/128 have dedicated clock pins which cannot be used as inputs and do not connect to the central switch matrix.*

Table 6. Logic Allocator for All MACH 4 Devices (except M4(LV)-32/32)

Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M_0	C_0, C_1, C_2	M_8	C_7, C_8, C_9, C_{10}
M_1	C_0, C_1, C_2, C_3	M_9	C_8, C_9, C_{10}, C_{11}
M_2	C_1, C_2, C_3, C_4	M_{10}	$C_9, C_{10}, C_{11}, C_{12}$
M_3	C_2, C_3, C_4, C_5	M_{11}	$C_{10}, C_{11}, C_{12}, C_{13}$
M_4	C_3, C_4, C_5, C_6	M_{12}	$C_{11}, C_{12}, C_{13}, C_{14}$
M_5	C_4, C_5, C_6, C_7	M_{13}	$C_{12}, C_{13}, C_{14}, C_{15}$
M_6	C_5, C_6, C_7, C_8	M_{14}	C_{13}, C_{14}, C_{15}
M_7	C_6, C_7, C_8, C_9	M_{15}	C_{14}, C_{15}

Table 7. Logic Allocator for M4(LV)-32/32

Output Macrocell	Available Clusters	Output Macrocell	Available Clusters
M_0	C_0, C_1, C_2	M_8	C_8, C_9, C_{10}
M_1	C_0, C_1, C_2, C_3	M_9	C_8, C_9, C_{10}, C_{11}
M_2	C_1, C_2, C_3, C_4	M_{10}	$C_9, C_{10}, C_{11}, C_{12}$
M_3	C_2, C_3, C_4, C_5	M_{11}	$C_{10}, C_{11}, C_{12}, C_{13}$
M_4	C_3, C_4, C_5, C_6	M_{12}	$C_{11}, C_{12}, C_{13}, C_{14}$
M_5	C_4, C_5, C_6, C_7	M_{13}	$C_{12}, C_{13}, C_{14}, C_{15}$
M_6	C_5, C_6, C_7	M_{14}	C_{13}, C_{14}, C_{15}
M_7	C_6, C_7	M_{15}	C_{14}, C_{15}

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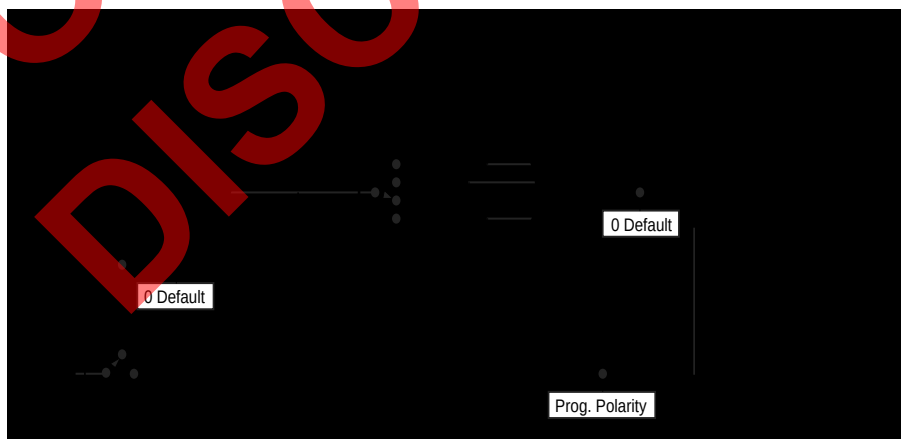
a. Synchronous Mode



b. Asynchronous Mode

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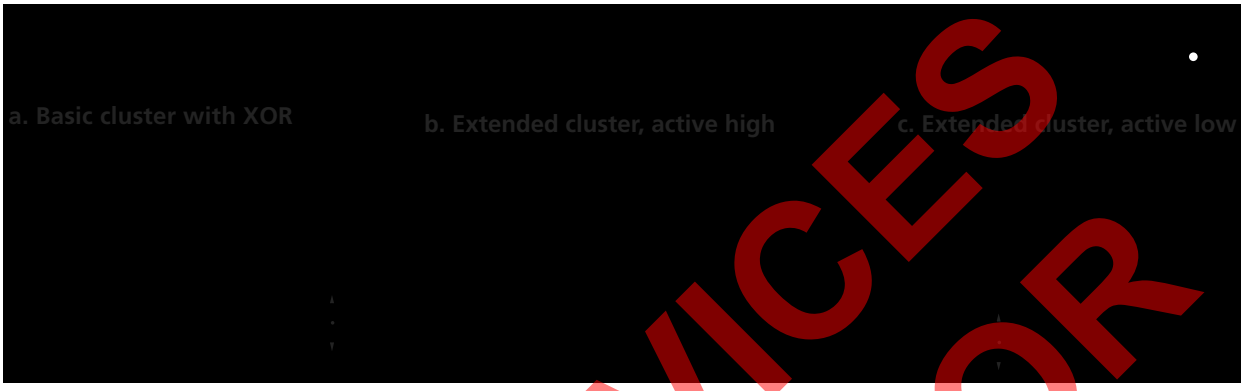
Figure 2. Logic Allocator: Configuration of Cluster "n" Set by Mode of Macrocell "n"



17466G-007

Figure 3. Logic Allocator Configurations: Synchronous Mode

17466G-008

Figure 4. Logic Allocator Configurations: Asynchronous Mode

Note that the configuration of the logic allocator has absolutely no impact on the speed of the signal. All configurations have the same delay. This means that designers do not have to decide between optimizing resources or speed; both can be optimized.

If not used in the cluster, the extra product term can act in conjunction with the basic cluster to provide XOR logic for such functions as data comparison, or it can work with the D-,T-type flip-flop to provide for J-K, and S-R register operation. In addition, if the basic cluster is routed to another macrocell, the extra product term is still available for logic. In this case, the first XOR input will be a logic 0. This circuit has the flexibility to route product terms elsewhere without giving up the use of the macrocell.

Product term clusters do not "wrap" around a PAL block. This means that the macrocells at the ends of the block have fewer product terms available.

The flip-flop can be configured as a D-type or T-type latch. J-K or S-R registers can be synthesized. The primary flip-flop configurations are shown in Figure 6, although others are possible. Flip-flop functionality is defined in Table 8. Note that a J-K latch is inadvisable as it will cause oscillation if both J and K inputs are HIGH.

17466G-011

Figure 6. Primary Macrocell Configurations

Table 8. Register/Latch Operation

Configuration	Input(s)	CLK/LE [1]	Q+
D-type Register	D=X	0, 1, ↓ (↑)	Q
	D=0	↑ (↓)	0
	D=1	↑ (↓)	1
T-type Register	T=X	0, 1, ↓ (↑)	Q
	T=0	↑ (↓)	Q
	T=1	↑ (↓)	$\overline{Q}$
D-type Latch	D=X	1 (0)	Q
	D=0	0 (1)	0
	D=1	0 (1)	1

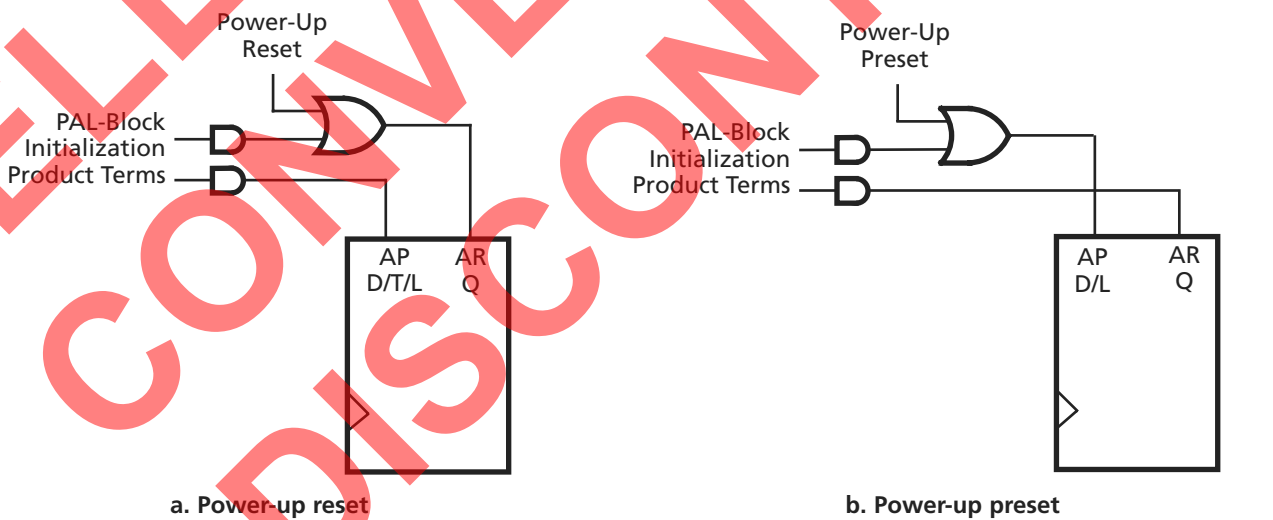
Note:

1. Polarity of CLK/LE can be programmed

Although the macrocell shows only one input to the register, the XOR gate in the logic allocator allows the D-, T-type register to emulate J-K, and S-R behavior. In this case, the available product terms are divided between J and K (or S and R). When configured as J-K, S-R, or T-type, the extra product term must be used on the XOR gate input for flip-flop emulation. In any register type, the polarity of the inputs can be programmed.

The clock input to the flip-flop can select any of the four PAL block clocks in synchronous mode, with the additional choice of either polarity of an individual product term clock in the asynchronous mode.

The initialization circuit depends on the mode. In synchronous mode (Figure 7), asynchronous reset and preset are provided, each driven by a product term common to the entire PAL block.



a. Power-up reset

b. Power-up preset

17466G-012

17466G-013

Figure 7. Synchronous Mode Initialization Configurations

Output Switch Matrix

The output switch matrix allows macrocells to be connected to any of several I/O cells within a PAL block. This provides high flexibility in determining pinout and allows design changes to occur without effecting pinout.

In MACH 4 devices with 2:1 Macrocell-I/O cell ratio, each PAL block has twice as many macrocells as I/O cells. The MACH 4 output switch matrix allows for half of the macrocells to drive I/O cells within a PAL block, in combinations according to Figure 9. Each I/O cell can choose from eight macrocells; each macrocell has a choice of four I/O cells. The MACH 4 devices with 1:1 Macrocell-I/O cell ratio allow each macrocell to drive one of eight I/O cells (Figure 9).

Figure 9. MACH 4 Output Switch Matrix

Table 10. Output Switch Matrix Combinations for MACH 4 Devices with 2:1 Macrocell-I/O Cell Ratio

Macrocell	Routable to I/O Cells
M0, M1	I/00, I/05, I/06, I/07
M2, M3	I/00, I/01, I/06, I/07
M4, M5	I/00, I/01, I/02, I/07
M6, M7	I/00, I/01, I/02, I/03
M8, M9	I/01, I/02, I/03, I/04
M10, M11	I/02, I/03, I/04, I/05
M12, M13	I/03, I/04, I/05, I/06
M14, M15	I/04, I/05, I/06, I/07

I/O Cell	Available Macrocells
I/00	M0, M1, M2, M3, M4, M5, M6, M7
I/01	M2, M3, M4, M5, M6, M7, M8, M9
I/02	M4, M5, M6, M7, M8, M9, M10, M11
I/03	M6, M7, M8, M9, M10, M11, M12, M13
I/04	M8, M9, M10, M11, M12, M13, M14, M15
I/05	M0, M1, M10, M11, M12, M13, M14, M15
I/06	M0, M1, M2, M3, M12, M13, M14, M15
I/07	M0, M1, M2, M3, M4, M5, M14, M15

Table 11. Output Switch Matrix Combinations for M4(LV)-32/32

Macrocell	Routable to I/O Cells
M0, M1, M2, M3, M4, M5, M6, M7	I/00, I/01, I/02, I/03, I/04, I/05, I/06, I/07
M8, M9, M10, M11, M12, M13, M14, M15	I/08, I/09, I/010, I/011, I/012, I/013, I/014, I/015

I/O Cell	Available Macrocells
I/00, I/01, I/02, I/03, I/04, I/05, I/06, I/07	M0, M1, M2, M3, M4, M5, M6, M7
I/08, I/09, I/010, I/011, I/012, I/013, I/014, I/015	M8, M9, M10, M11, M12, M13, M14, M15

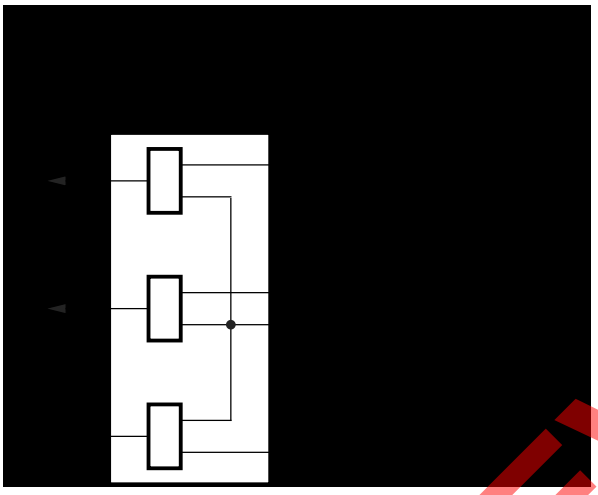


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Figure 12. MACH 4 with 2:1 Macrocell-I/O Cell Ratio - Input Switch Matrix

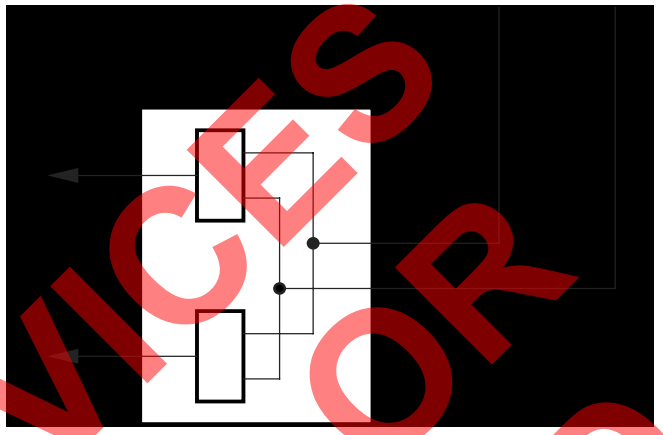

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Figure 13. MACH 4 with 1:1 Macrocell-I/O Cell Ratio - Input Switch Matrix

PAL Block Clock Generation

Each MACH 4 device has four clock pins that can also be used as inputs. These pins drive a clock generator in each PAL block (Figure 14). The clock generator provides four clock signals that can be used anywhere in the PAL block. These four PAL block clock signals can consist of a large number of combinations of the true and complement edges of the global clock signals. Table 12 lists the possible combinations.

17466G-004

Figure 14. PAL Block Clock Generator [1]

Note:

1. *M4(LV)-32/32 and M4(LV)-64/32 have only two clock pins, GCLK0 and GCLK1. GCLK2 is tied to GCLK0, and GCLK3 is tied to GCLK1.*

Table 12. PAL Block Clock Combinations[1]

Block CLK0	Block CLK1	Block CLK2	Block CLK3
GCLK0	GCLK1	X	X
$\overline{\text{GCLK1}}$	GCLK1	X	X
GCLK0	$\overline{\text{GCLK0}}$	X	X
$\overline{\text{GCLK1}}$	$\overline{\text{GCLK0}}$	X	X
X	X	GCLK2 (GCLK0)	GCLK3 (GCLK1)
X	X	$\overline{\text{GCLK3}}$ ($\overline{\text{GCLK1}}$)	GCLK3 (GCLK1)
X	X	GCLK2 (GCLK0)	$\overline{\text{GCLK2}}$ ($\overline{\text{GCLK0}}$)
X	X	$\overline{\text{GCLK3}}$ ($\overline{\text{GCLK1}}$)	$\overline{\text{GCLK2}}$ ($\overline{\text{GCLK0}}$)

Note:

1. Values in parentheses are for the M4(LV)-32/32 and M4(LV)-64/32.

This feature provides high flexibility for partitioning state machines and dual-phase clocks. It also allows latches to be driven with either polarity of latch enable, and in a master-slave configuration.

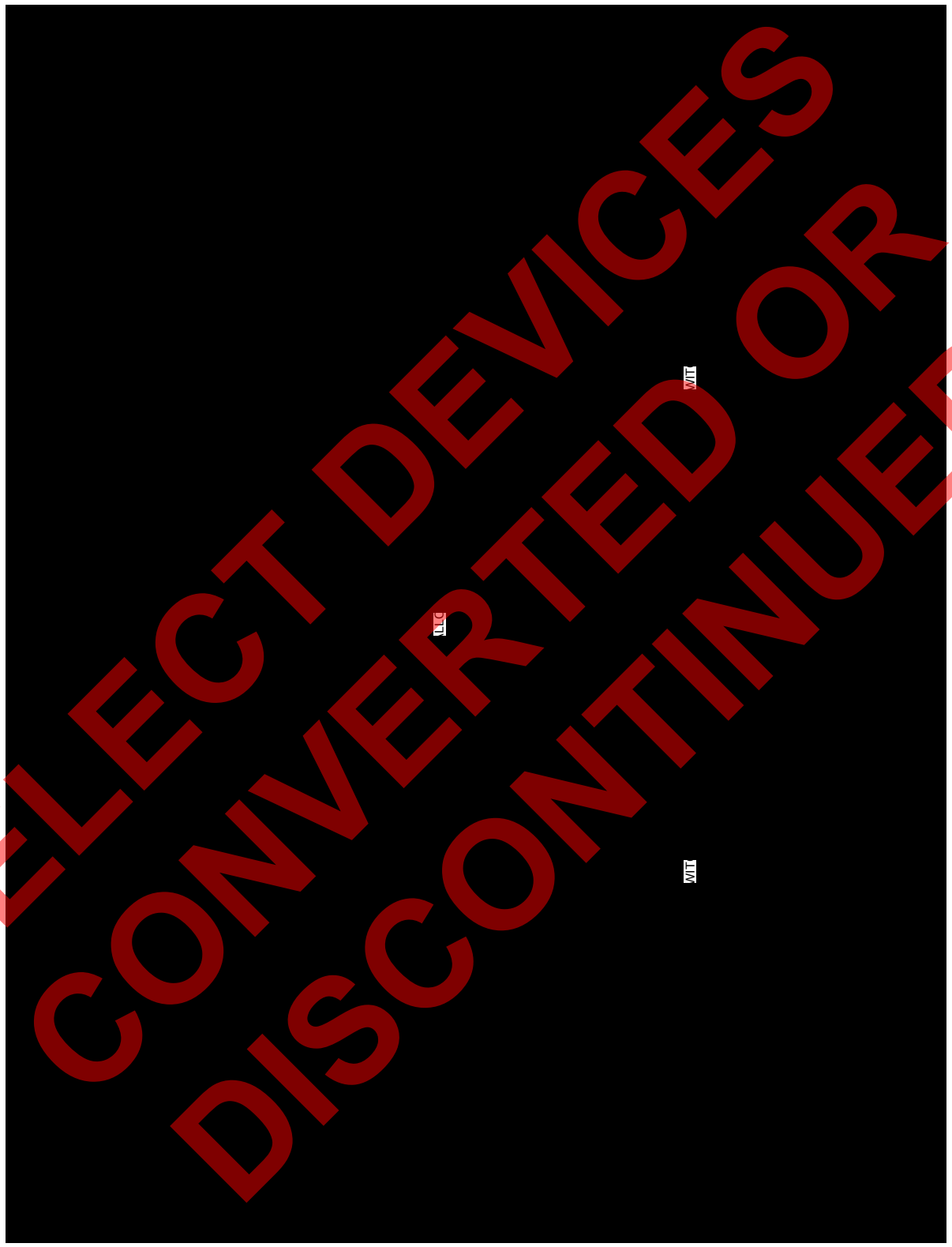

Figure 17. PAL Block for M4(LV)-32/32

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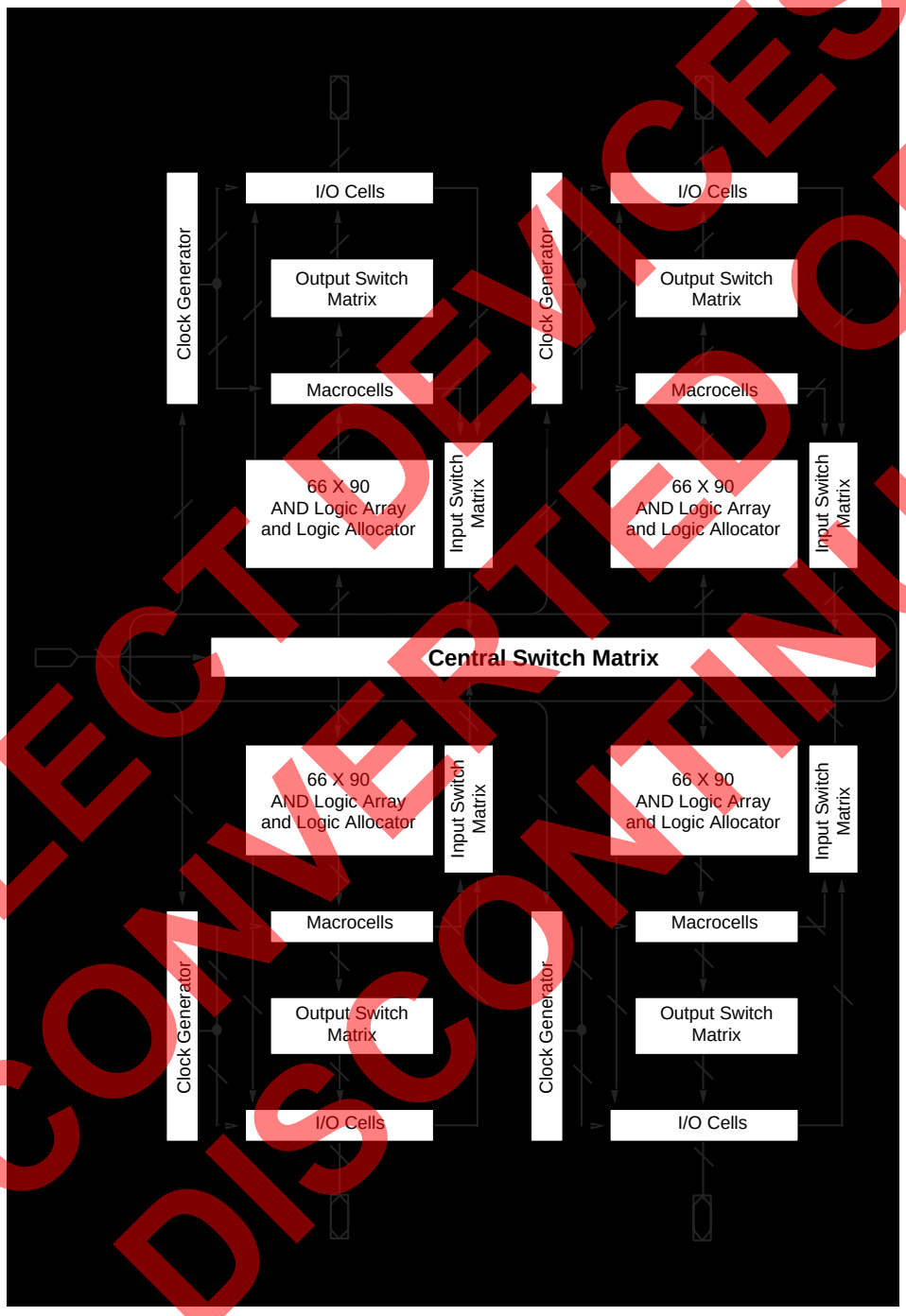
BLOCK DIAGRAM – M4(LV)-64/32



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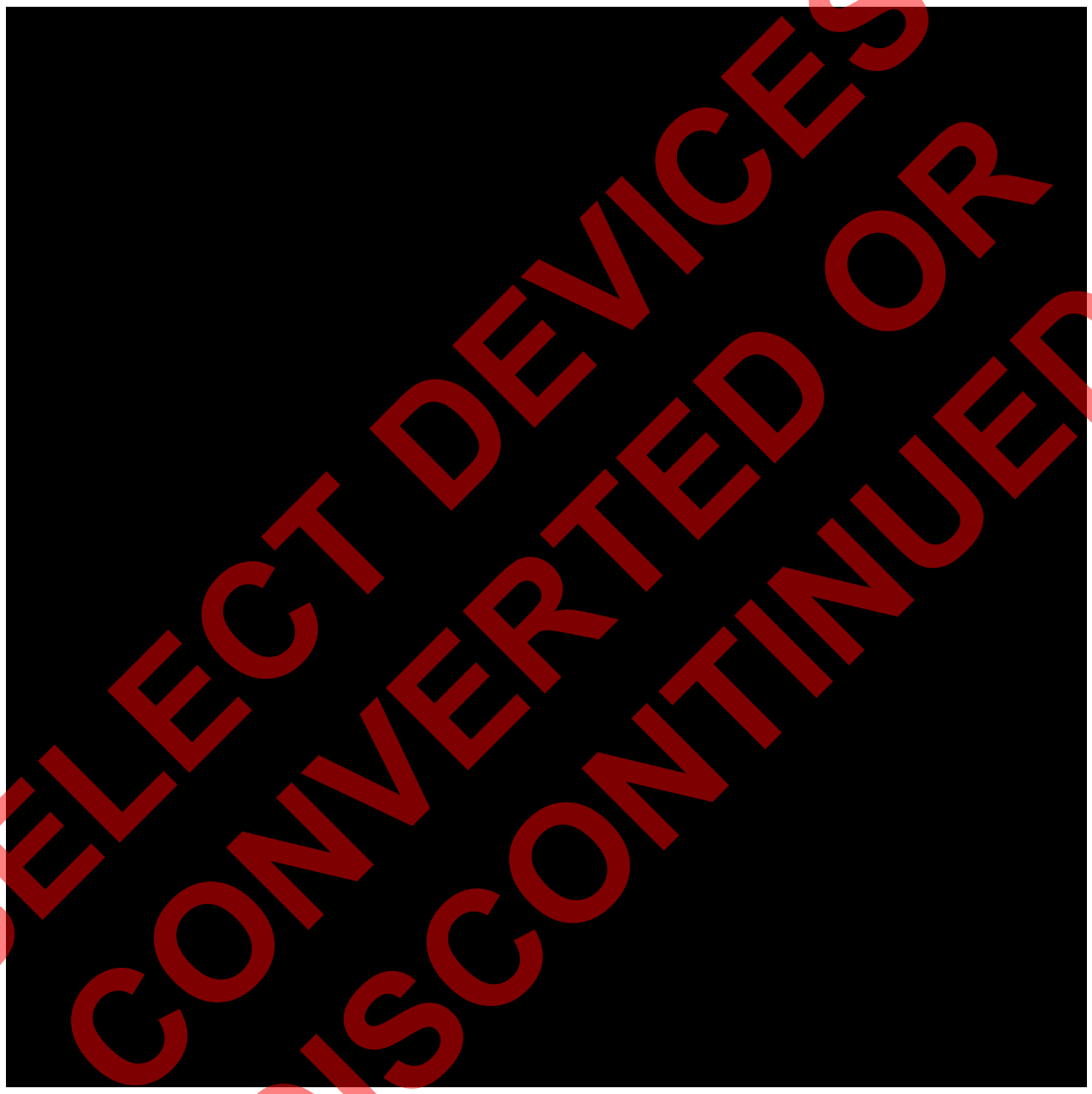
BLOCK DIAGRAM – M4(LV)-192/96



17466G-067

ABSOLUTE MAXIMUM RATINGS

M4LV

Storage Temperature . . . . . -65°C to +150°C

Ambient Temperature
with Power Applied . . . . . -55°C to +100°C

Device Junction Temperature . . . . . +130°C

Supply Voltage
with Respect to Ground . . . . . -0.5 V to +4.5 V

DC Input Voltage . . . . . -0.5 V to 6.0 V

Static Discharge Voltage . . . . . 2000 V

Latchup Current (T_A = -40°C to +85°C). . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +3.0 V to +3.6 V

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

3.3-V DC CHARACTERISTICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	I_{OH} = –100 µA	V_{CC} – 0.2			V
			I_{OH} = –3.2 mA	2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} (Note 1)	I_{OL} = 100 µA			0.2	V
			I_{OL} = 24 mA			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs		2.0		5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs		–0.3		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 3.6 V, V_{CC} = Max (Note 2)				5	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)				–5	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 3.6 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)				5	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 2)				–5	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max (Note 3)		–15		–160	mA

Notes:

1. *Total I_{OL} for one PAL block should not exceed 64 mA.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.*

MACH 4 TIMING PARAMETERS OVER OPERATING RANGES[1]

		-7		-10		-12		-14		-15		-18		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Combinatorial Delay:														
t_{PDi}	Internal combinatorial propagation delay		5.5		8.0		10.0		12.0		13.0		16.0	ns
t_{PD}	Combinatorial propagation delay		7.5		10.0		12.0		14.0		15.0		18.0	ns
Registered Delays:														
t_{SS}	Synchronous clock setup time, D-type register	5.5		6.0		7.0		10.0		10.0		12.0		ns
t_{SST}	Synchronous clock setup time, T-type register	6.5		7.0		8.0		11.0		11.0		13.0		ns
t_{SA}	Asynchronous clock setup time, D-type register	3.5		4.0		5.0		8.0		8.0		10.0		ns
t_{SAT}	Asynchronous clock setup time, T-type register	4.5		5.0		6.0		9.0		9.0		11.0		ns
t_{HS}	Synchronous clock hold time	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{HA}	Asynchronous clock hold time	3.5		4.0		5.0		8.0		8.0		10.0		ns
t_{COSi}	Synchronous clock to internal output		3.5		4.5		6.0		8.0		8.0		10.0	ns
t_{COS}	Synchronous clock to output		5.5		6.5		8.0		10.0		10.0		12.0	ns
t_{COAi}	Asynchronous clock to internal output		7.5		10.0		12.0		16.0		16.0		18.0	ns
t_{COA}	Asynchronous clock to output		9.5		12.0		14.0		18.0		18.0		20.0	ns
Latched Delays:														
t_{SSL}	Synchronous Latch setup time	6.0		7.0		8.0		10.0		10.0		12.0		ns
t_{SAL}	Asynchronous Latch setup time	4.0		4.0		5.0		8.0		8.0		10.0		ns
t_{HSL}	Synchronous Latch hold time	0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{HAL}	Asynchronous Latch hold time	4.0		4.0		5.0		8.0		8.0		10.0		ns
t_{PDLi}	Transparent latch to internal output		8.0		10.0		12.0		15.0		15.0		18.0	ns
t_{PDL}	Propagation delay through transparent latch to output		10.0		12.0		14.0		17.0		17.0		20.0	ns
t_{GOSi}	Synchronous Gate to internal output		4.0		5.5		8.0		9.0		9.0		10.0	ns
t_{GOS}	Synchronous Gate to output		6.0		7.5		10.0		11.0		11.0		12.0	ns
t_{GOAi}	Asynchronous Gate to internal output		9.0		11.0		14.0		17.0		17.0		20.0	ns
t_{GOA}	Asynchronous Gate to output		11.0		13.0		16.0		19.0		19.0		22.0	ns
Input Register Delays:														
t_{SIRS}	Input register setup time	2.0		2.0		2.0		2.0		2.0		2.0		ns
t_{HIRS}	Input register hold time	3.0		3.0		3.0		4.0		4.0		4.0		ns
t_{ICOSi}	Input register clock to internal feedback		3.5		4.5		6.0		6.0		6.0		6.0	ns
Input Latch Delays:														
t_{SIL}	Input latch setup time	2.0		2.0		2.0		2.0		2.0		2.0		ns
t_{HIL}	Input latch hold time	3.0		3.0		3.0		4.0		4.0		4.0		ns
t_{IGOSi}	Input latch gate to internal feedback		4.0		4.0		4.0		5.0		5.0		6.0	ns
t_{PDILi}	Transparent input latch to internal feedback		2.0		2.0		2.0		2.0		2.0		2.0	ns
Input Register Delays with ZHT Option:														
t_{SIRZ}	Input register setup time - ZHT	6.0		6.0		6.0		6.0		6.0		6.0		ns
t_{HIRZ}	Input register hold time - ZHT	0.0		0.0		0.0		0.0		0.0		0.0		ns

MACH 4 TIMING PARAMETERS OVER OPERATING RANGES[1] (CONTINUED)

		-7		-10		-12		-14		-15		-18		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Frequency:														
f_{MAXS}	External feedback, D-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{COS})$	90.9		80.0		66.7		50.0		50.0		41.7		MHz
	External feedback, T-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SST} + t_{COS})$	83.3		74.1		62.5		47.6		47.6		40.0		MHz
	Internal feedback (f_{CNT}), D-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{COSi})$	111.1		95.2		76.9		55.6		55.6		45.5		MHz
	Internal feedback (f_{CNT}), T-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SST} + t_{COSi})$	100.0		87.0		71.4		52.6		52.6		43.5		MHz
	No feedback[2], Min of $1/(t_{WLS} + t_{WHS})$, $1/(t_{SS} + t_{HS})$ or $1/(t_{SST} + t_{HS})$	153.8		100.0		83.3		83.3		83.3		71.4		MHz
f_{MAXA}	External feedback, D-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COA})$	76.9		62.5		52.6		38.5		38.5		33.3		MHz
	External feedback, T-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SAT} + t_{COA})$	71.4		58.8		50.0		37.0		37.0		32.3		MHz
	Internal feedback (f_{CNTA}), D-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COAi})$	90.9		71.4		58.8		41.7		41.7		35.7		MHz
	Internal feedback (f_{CNTA}), T-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SAT} + t_{COAi})$	83.3		66.7		55.6		40.0		40.0		34.5		MHz
	No feedback[2], Min of $1/(t_{WLA} + t_{WHA})$, $1/(t_{SA} + t_{HA})$ or $1/(t_{SAT} + t_{HA})$	125.0		100.0		62.5		55.6		55.6		50.0		MHz
f_{MAXI}	Maximum input register frequency, Min of $1/(t_{WIRH} + t_{WIRL})$ or $1/(t_{SIRS} + t_{HIRS})$	111.0		100.0		83.3		83.3		83.3		71.4		MHz

Notes:

1. *See "MACH Switching Test Circuit" document on the Literature Download page of the Lattice web site.*
2. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

CAPACITANCE [1]

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input capacitance	V_{IN}=2.0 V	3.3 V or 5 V, 25°C, 1 MHz	6	pF
$C_{I/O}$	Output capacitance	V_{OUT}=2.0V	3.3 V or 5 V, 25°C, 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where this parameter may be affected.*

44-PIN TQFP CONNECTION DIAGRAM (M4(LV)-32/32 AND M4(LV)-64/32)

Top View

44-Pin TQFP

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

100-PIN TQFP CONNECTION DIAGRAM (M4(LV)-128/64)

Top View

100-Pin TQFP

17466G-032

PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out
TRST = Test Reset
ENABLE = Program

208-PIN PQFP CONNECTION DIAGRAM (M4(LV)-256/128)

Top View

208-Pin PQFP

17466G-044

17466H-066

MACH 4 PRODUCT ORDERING INFORMATION

MACH 4 Devices Commercial & Industrial - 3.3V and 5V

Lattice/Vantis programmable logic products are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

M4- / 256 / 128 -7 Y C

FAMILY TYPE

M4- = MACH 4 Family (5-V V_{CC})
M4LV- = MACH 4 Family Low Voltage (3.3-V V_{CC})

MACROCELL DENSITY

32 = 32 Macrocells
64 = 64 Macrocells
96 = 96 Macrocells
128 = 128 Macrocells
128N = 128 Macrocells, Non-ISP
192 = 192 Macrocells
256 = 256 Macrocells

I/Os

/32 = 32 I/Os in 44-pin PLCC, 44-pin TQFP or 48-pin TQFP
/48 = 48 I/Os in 100-pin TQFP
/64 = 64 I/Os in 84-pin PLCC, 100-pin PQFP or 100-pin TQFP
/96 = 96 I/Os in 144-pin TQFP
/128 = 128 I/Os in 208-pin PQFP or 256-ball BGA

SPEED

-7 = 7.5 ns t_{PD}
-10 = 10 ns t_{PD}
-12 = 12 ns t_{PD}
-14 = 14 ns t_{PD}
-15 = 15 ns t_{PD}
-18 = 18 ns t_{PD}

PACKAGE TYPE

A = Ball Grid Array (BGA)
J = Plastic Leaded Chip Carrier (PLCC)
V = Thin Quad Flat Pack (TQFP)
Y = Plastic Quad Flat Pack (PQFP)

OPERATING CONDITIONS

C = Commercial (0°C to +70°C)
I = Industrial (-40°C to +85°C)

48 = 48-pin TQFP for M4(LV)-32/32 or M4(LV)-64/32

Valid Combinations		
M4-32/32	-7, -10, -12, -15	JC, VC, VC48
M4LV-32/32		JC, VC, VC48
M4-64/32		JC, VC, VC48
M4LV-64/32		JC, VC, VC48
M4-96/48		VC
M4LV-96/48		VC
M4-128/64		YC, VC
M4LV-128/64		YC, VC
M4-128N/64		JC
M4LV-128N/64		JC
M4-192/96		VC
M4LV-192/96		VC
M4-256/128		YC
M4LV-256/128		YC, AC

All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial speed grade is slower, i.e., M4-256/128-7YC-10YI

Valid Combinations		
M4-32/32	-10, -12, -14, -18	JI, VI, VI48
M4LV-32/32		JI, VI, VI48
M4-64/32		JI, VI, VI48
M4LV-64/32		JI, VI, VI48
M4-96/48		VI
M4LV-96/48		VI
M4-128/64		YI, VI
M4LV-128/64		YI, VI
M4-128N/64		JI
M4LV-128N/64		JI
M4-192/96		VI
M4LV-192/96		VI
M4-256/128		YI
M4LV-256/128		YI, AI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.