Lattice Semiconductor Corporation - M4-128N/64-7JC Datasheet

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Obsolete
Programmable Type	In System Programmable
Delay Time tpd(1) Max	7.5 ns
Voltage Supply - Internal	4.75V ~ 5.25V
Number of Logic Elements/Blocks	-
Number of Macrocells	128
Number of Gates	-
Number of I/O	64
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	84-LCC (J-Lead)
Supplier Device Package	84-PLCC (29.31x29.31)
Purchase URL	https://www.e-xfl.com/product-detail/lattice-semiconductor/m4-128n-64-7jc

Product Line	Ordering Part Number	Product Status	Reference PCN
M4-64/32	M4-64/32-7JC	Converted to M4A5	Contact pcn@latticesemi.com for more info.
	M4-64/32-10JC		
	M4-64/32-12JC		
	M4-64/32-15JC		
	M4-64/32-10JI		
	M4-64/32-12JI		
	M4-64/32-14JI		
	M4-64/32-18JI		
	M4-64/32-7VC		
	M4-64/32-10VC		
	M4-64/32-12VC		
	M4-64/32-15VC		
	M4-64/32-10VI		
	M4-64/32-12VI		
	M4-64/32-14VI		
	M4-64/32-18VI		
	M4-64/32-7VC48		
	M4-64/32-10VC48		
	M4-64/32-12VC48		
	M4-64/32-15VC48		
	M4-64/32-10VI48		
	M4-64/32-12VI48		
	M4-64/32-14VI48		
	M4-64/32-18VI48		
M4-96/48	M4-96/48-7VC	Convert to M4A5	Contact pcn@latticesemi.com for more info.
	M4-96/48-10VC		
	M4-96/48-12VC		
	M4-96/48-15VC		
	M4-96/48-10VI		
	M4-96/48-12VI		
	M4-96/48-14VI		
	M4-96/48-18VI		
M4-128/64	M4-128/64-7YC	Convert to M4A5	Contact pcn@latticesemi.com for more info.
	M4-128/64-10YC		
	M4-128/64-12YC		
	M4-128/64-15YC		
	M4-128/64-10YI		
	M4-128/64-12YI		
	M4-128/64-14YI		
	M4-128/64-18YI		

5555 N.E. Moore Ct. ● Hillsboro, Oregon 97124-6421 ● Phone (503) 268-8000 ● FAX (503) 268-8347
Internet: http://www.latticesemi.com

Product Line	Ordering Part Number	Product Status	Reference PCN
M4LV-32/32 (Cont'd)	M4LV-32/32-7VC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-32/32-10VC		
	M4LV-32/32-12VC		
	M4LV-32/32-15VC		
	M4LV-32/32-10VI		
	M4LV-32/32-12VI		
	M4LV-32/32-14VI		
	M4LV-32/32-18VI		
	M4LV-32/32-7VC48		
	M4LV-32/32-10VC48		
	M4LV-32/32-12VC48		
	M4LV-32/32-15VC48		
	M4LV-32/32-10VI48		
	M4LV-32/32-12VI48		
	M4LV-32/32-14VI48		
	M4LV-32/32-18VI48		
M4LV-64/32	M4LV-64/32-7JC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-64/32-10JC		
	M4LV-64/32-12JC		
	M4LV-64/32-15JC		
	M4LV-64/32-10JI		
	M4LV-64/32-12JI		
	M4LV-64/32-14JI		
	M4LV-64/32-18JI		
	M4LV-64/32-7VC		
	M4LV-64/32-10VC		
	M4LV-64/32-12VC		
	M4LV-64/32-15VC		
	M4LV-64/32-10VI		
	M4LV-64/32-12VI		
	M4LV-64/32-14VI		
	M4LV-64/32-18VI		
	M4LV-64/32-7VC48		
	M4LV-64/32-10VC48		
	M4LV-64/32-12VC48		
	M4LV-64/32-15VC48		
	M4LV-64/32-10VI48		
	M4LV-64/32-12VI48		
	M4LV-64/32-14VI48		
	M4LV-64/32-18VI48		

Product Line	Ordering Part Number	Product Status	Reference PCN
M4LV-256/128	M4LV-256/128-7YC	Convert to M4A3	Contact pcn@latticesemi.com for more info.
	M4LV-256/128-10YC		
	M4LV-256/128-12YC		
	M4LV-256/128-15YC		
	M4LV-256/128-10YI		
	M4LV-256/128-12YI		
	M4LV-256/128-14YI		
	M4LV-256/128-18YI		
	M4LV-256/128-7AC		
	M4LV-256/128-10AC		
	M4LV-256/128-12AC		
	M4LV-256/128-15AC		
	M4LV-256/128-10AI		
	M4LV-256/128-12AI		
	M4LV-256/128-14AI		
	M4LV-256/128-18AI		

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GENERAL DESCRIPTION

The MACH® 4 family from Lattice offers an exceptionally flexible architecture and delivers a superior Complex Programmable Logic Device (CPLD) solution of easy-to-use silicon products and software tools. The overall benefits for users are a guaranteed and predictable CPLD solution, faster time-to-market, greater flexibility and lower cost. The MACH 4 devices offer densities ranging from 32 to 256 macrocells with 100% utilization and 100% pin-out retention. The MACH 4 family offer 5-V (M4-xxx) and 3.3-V (M4LV-xxx) operation.

MACH 4 products are 5-V or 3.3-V in-system programmable through the JTAG (IEEE Std. 1149.1) interface. JTAG boundary scan testing also allows product testability on automated test equipment for device connectivity.

All MACH 4 family members deliver First-Time-Fit and easy system integration with pin-out retention after any design change and refit. For both 3.3-V and 5-V operation, MACH 4 products can deliver guaranteed fixed timing as fast as 7.5 ns t_{PD} and 111 MHz f_{CNT} through the SpeedLocking feature when using up to 20 product terms per output (Table 2).

Table 2. MACH 4 Speed Grades

Device	Speed Grade[1]					
	-7	-10	-12	-14	-15	-18
M4-32/32 M4LV-32/32	C	C, I	C, I	I	C	I
M4-64/32 M4LV-64/32	C	C, I	C, I	I	C	I
M4-96/48 M4LV-96/48	C	C, I	C, I	I	C	I
M4-128/64 M4LV-128/64	C	C, I	C, I	I	C	I
M4-128N/64 M4LV-128N/64	C	C, I	C, I	I	C	I
M4-192/96 M4LV-192/96	C	C, I	C, I	I	C	I
M4-256/128 M4LV-256/128	C	C, I	C, I	I	C	I

Note:

1. C = Commercial, I = Industrial

The MACH 4 family offers numerous density-I/O combinations in Thin Quad Flat Pack (TQFP), Plastic Quad Flat Pack (PQFP), Plastic Leaded Chip Carrier (PLCC), and Ball Grid Array (BGA) packages ranging from 44 to 256 pins (Table 3). It also offers I/O safety features for mixed-voltage designs so that the 3.3-V devices can accept 5-V inputs, and 5-V devices do not overdrive 3.3-V inputs. Additional features include Bus-Friendly inputs and I/Os, a programmable power-down mode for extra power savings and individual output slew rate control for the highest speed transition or for the lowest noise transition.

Table 3. MACH 4 Package and I/O Options (Number of I/Os and dedicated inputs in Table)

Package	M4-32/32 M4LV-32/32	M4-64/32 M4LV-64/32	M4-96/48 M4LV-96/48	M4-128/64 M4LV-128/64	M4-128N/64 M4LV-128N/64	M4-192/96 M4LV-192/96	M4LV-256/128
44-pin PLCC	32+2	32+2					
44-pin TQFP	32+2	32+2					
48-pin TQFP	32+2	32+2					
84-pin PLCC					64+6		
100-pin TQFP			48+8	64+6			
100-pin PQFP				64+6			
144-pin TQFP						96+16	
208-pin PQFP							128+14
256-ball BGA							128+14

FUNCTIONAL DESCRIPTION

The fundamental architecture of MACH 4 devices (Figure 1) consists of multiple, optimized PAL® blocks interconnected by a central switch matrix. The central switch matrix allows communication between PAL blocks and routes inputs to the PAL blocks. Together, the PAL blocks and central switch matrix allow the logic designer to create large designs in a single device instead of having to use multiple devices.

The key to being able to make effective use of these devices lies in the interconnect schemes. In MACH 4 architecture, the macrocells are flexibly coupled to the product terms through the logic allocator, and the I/O pins are flexibly coupled to the macrocells due to the output switch matrix. In addition, more input routing options are provided by the input switch matrix. These resources provide the flexibility needed to fit designs efficiently.

Figure 1. MACH 4 Block Diagram and PAL Block Structure

Notes:

1. *16 for MACH 4 devices with 1:1 macrocell-I/O cell ratio (see next page).*
2. *Block clocks do not go to I/O cells in M4(LV)-32/32.*
3. *M4(LV)-192/96 and M4(LV)-256/128 have dedicated clock pins which cannot be used as inputs and do not connect to the central switch matrix.*

Table 4. Architectural Summary of MACH 4 devices

	MACH 4 Devices	
	M4-64/32, M4LV-64/32 M4-96/48, M4LV-96/48 M4-128/64, M4LV-128/64 M4-128N/64, M4LV-128N/64 M4-192/96, M4LV-192/96 M4-256/128, M4LV-256/128	M4-32/32 M4LV-32/32
Macrocell-I/O Cell Ratio	2:1	1:1
Input Switch Matrix	Yes	Yes
Input Registers	Yes	No
Central Switch Matrix	Yes	Yes
Output Switch Matrix	Yes	Yes

The Macrocell-I/O cell ratio is defined as the number of macrocells versus the number of I/O cells internally in a PAL block (Table 4).

The central switch matrix takes all dedicated inputs and signals from the input switch matrices and routes them as needed to the PAL blocks. Feedback signals that return to the same PAL block still must go through the central switch matrix. This mechanism ensures that PAL blocks in MACH 4 devices communicate with each other with consistent, predictable delays.

The central switch matrix makes a MACH 4 device more advanced than simply several PAL devices on a single chip. It allows the designer to think of the device not as a collection of blocks, but as a single programmable device; the software partitions the design into PAL blocks through the central switch matrix so that the designer does not have to be concerned with the internal architecture of the device.

Each PAL block consists of:

- Product-term array
- Logic allocator
- Macrocells
- Output switch matrix
- I/O cells
- Input switch matrix
- Clock generator

I/O Cell

The I/O cell (Figures 10 and 11) simply consists of a programmable output enable, a feedback path, and flip-flop (except MACH 4 devices with 1:1 macrocell-I/O cell ratio.) An individual output enable product term is provided for each I/O cell. The feedback signal drives the input switch matrix.

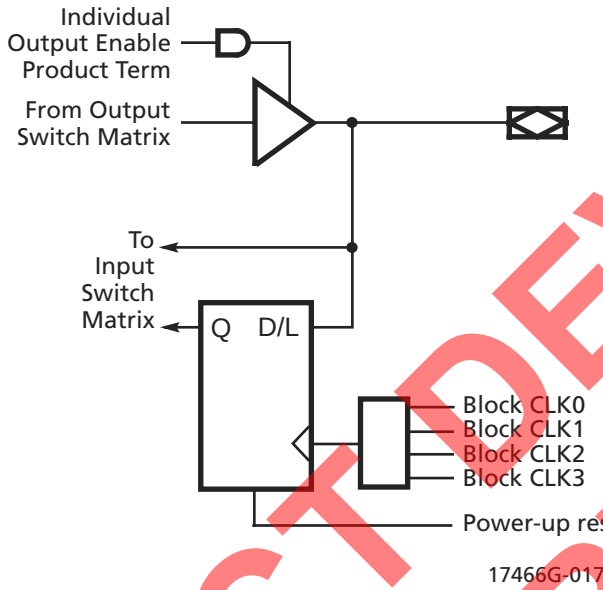


Figure 10. I/O Cell for MACH 4 Devices with 2:1 Macrocell-I/O Cell Ratio

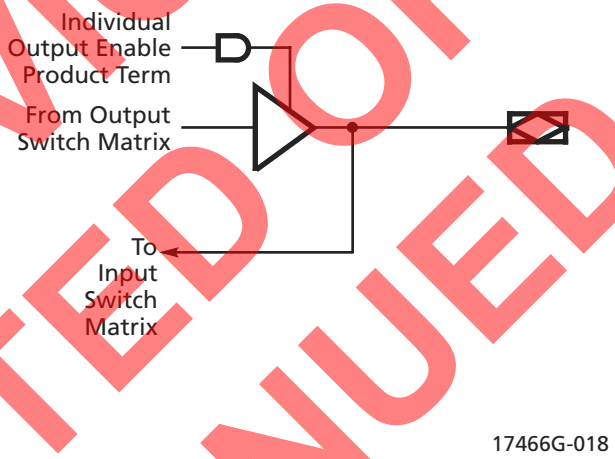


Figure 11. I/O Cell for MACH 4 Devices with 1:1 Macrocell-I/O Cell Ratio

The I/O cell (Figure 10) contains a flip-flop, which provides the capability for storing the input in a D-type register or latch. The clock can be any of the PAL block clocks. Both the direct and registered versions of the input are sent to the input switch matrix. This allows for such functions as "time-domain-multiplexed" data comparison, where the first data value is stored, and then the second data value is put on the I/O pin and compared with the previous stored value.

Note that the flip-flop used in the MACH 4 I/O cell is independent of the flip-flops in the macrocells. It powers up to a logic low.

Zero-Hold-Time Input Register

The MACH 4 devices have a zero-hold-time (ZHT) fuse which controls the time delay associated with loading data into all I/O cell registers and latches. When programmed, the ZHT fuse increases the data path setup delays to input storage elements, matching equivalent delays in the clock path. When the fuse is erased, the setup time to the input storage element is minimized. This feature facilitates doing worst-case designs for which data is loaded from sources which have low (or zero) minimum output propagation delays from clock edges.

Input Switch Matrix

The input switch matrix (Figures 12 and 13) optimizes routing of inputs to the central switch matrix. Without the input switch matrix, each input and feedback signal has only one way to enter the central switch matrix. The input switch matrix provides additional ways for these signals to enter the central switch matrix.

POWER MANAGEMENT

Each individual PAL block in MACH 4 devices features a programmable low-power mode, which results in power savings of up to 50%. The signal speed paths in the low-power PAL block will be slower than those in the non-low-power PAL block. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in the low-power mode.

PROGRAMMABLE SLEW RATE

Each MACH 4 device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3 V/ns) or for the lower noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

POWER-UP RESET/SET

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee initialization values, the V_{CC} rise must be monotonic, and the clock must be inactive until the reset delay time has elapsed.

SECURITY BIT

A programmable security bit is provided on the MACH 4 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

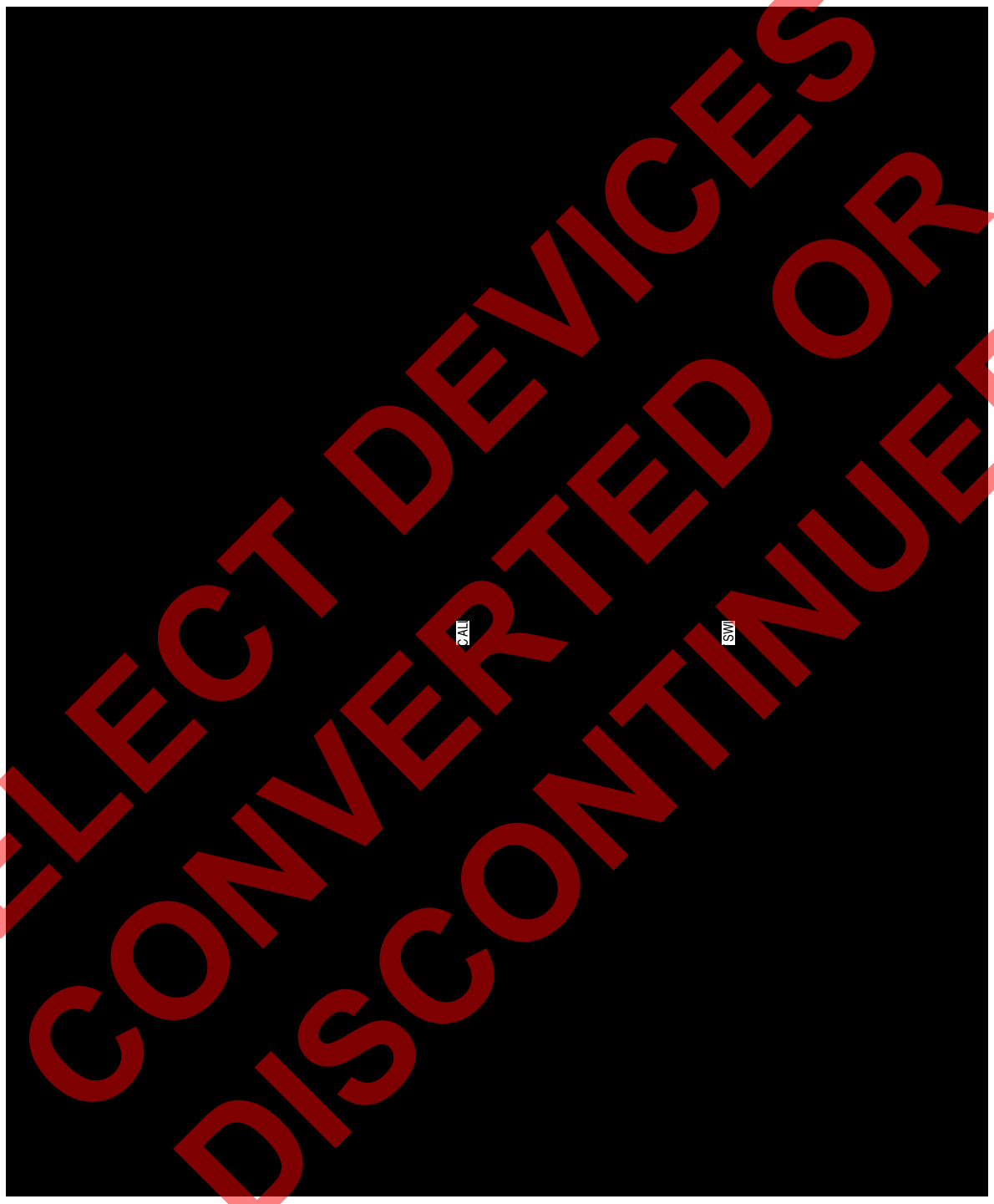
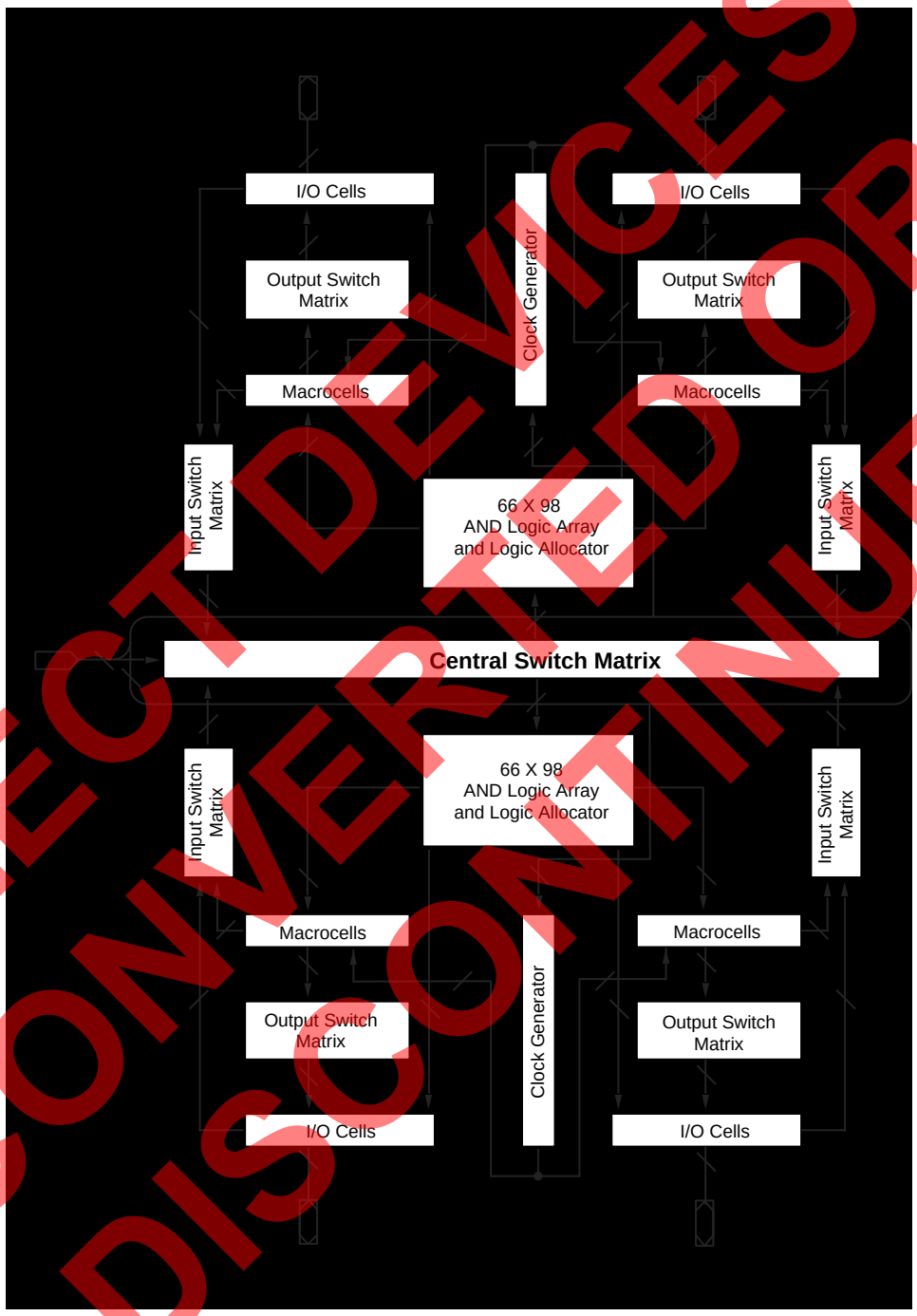


Figure 16. PAL Block for MACH 4 with 2:1 Macrocell - I/O Cell Ratio

BLOCK DIAGRAM – M4(LV)-32/32



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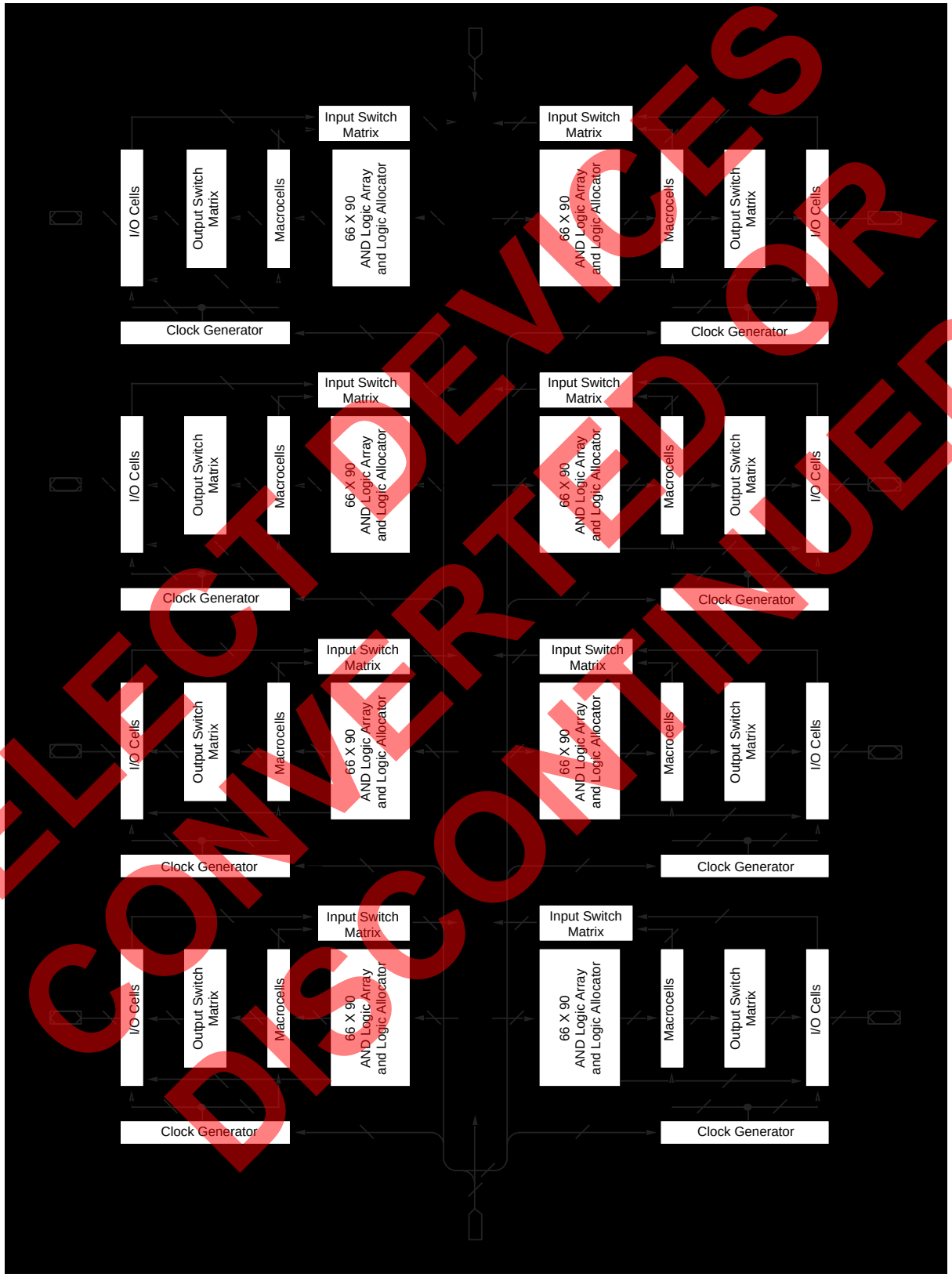
BLOCK DIAGRAM – M4(LV)-128N/64 AND M4(LV)-128/64



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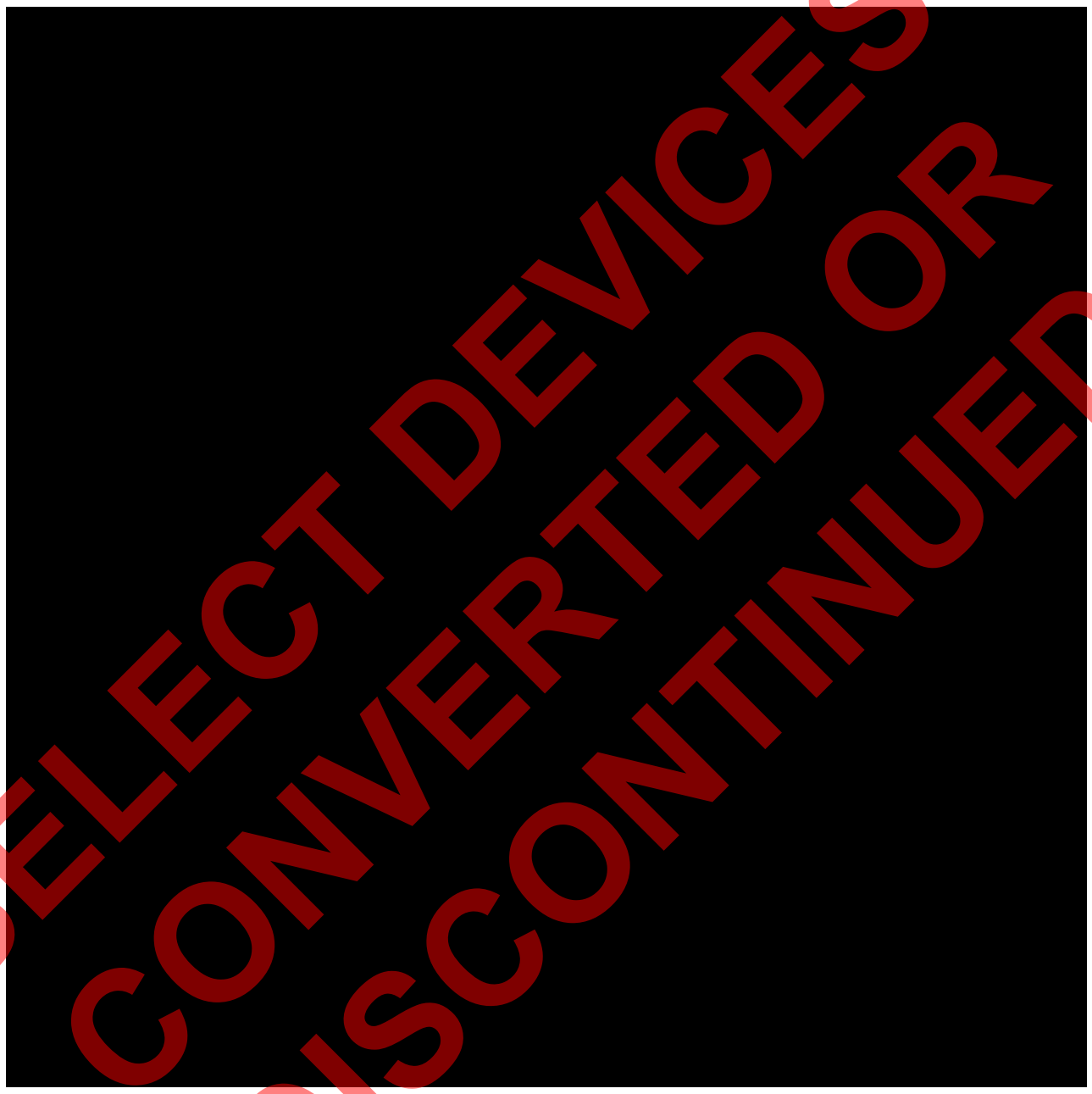
BLOCK DIAGRAM – M4(LV)-192/96



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MACH 4 TIMING PARAMETERS OVER OPERATING RANGES[1] (CONTINUED)

		-7		-10		-12		-14		-15		-18		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Frequency:														
f_{MAXS}	External feedback, D-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{COS})$	90.9		80.0		66.7		50.0		50.0		41.7		MHz
	External feedback, T-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SST} + t_{COS})$	83.3		74.1		62.5		47.6		47.6		40.0		MHz
	Internal feedback (f_{CNT}), D-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{COSi})$	111.1		95.2		76.9		55.6		55.6		45.5		MHz
	Internal feedback (f_{CNT}), T-type, Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SST} + t_{COSi})$	100.0		87.0		71.4		52.6		52.6		43.5		MHz
	No feedback[2], Min of $1/(t_{WLS} + t_{WHS})$, $1/(t_{SS} + t_{HS})$ or $1/(t_{SST} + t_{HS})$	153.8		100.0		83.3		83.3		83.3		71.4		MHz
f_{MAXA}	External feedback, D-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COA})$	76.9		62.5		52.6		38.5		38.5		33.3		MHz
	External feedback, T-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SAT} + t_{COA})$	71.4		58.8		50.0		37.0		37.0		32.3		MHz
	Internal feedback (f_{CNTA}), D-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COAi})$	90.9		71.4		58.8		41.7		41.7		35.7		MHz
	Internal feedback (f_{CNTA}), T-type, Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SAT} + t_{COAi})$	83.3		66.7		55.6		40.0		40.0		34.5		MHz
	No feedback[2], Min of $1/(t_{WLA} + t_{WHA})$, $1/(t_{SA} + t_{HA})$ or $1/(t_{SAT} + t_{HA})$	125.0		100.0		62.5		55.6		55.6		50.0		MHz
f_{MAXI}	Maximum input register frequency, Min of $1/(t_{WIRH} + t_{WIRL})$ or $1/(t_{SIRS} + t_{HIRS})$	111.0		100.0		83.3		83.3		83.3		71.4		MHz

Notes:

1. *See "MACH Switching Test Circuit" document on the Literature Download page of the Lattice web site.*
2. *This parameter does not apply to flip-flops in the emulated mode since the feedback path is required for emulation.*

CAPACITANCE [1]

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input capacitance	V_{IN}=2.0 V	3.3 V or 5 V, 25°C, 1 MHz	6	pF
$C_{I/O}$	Output capacitance	V_{OUT}=2.0V	3.3 V or 5 V, 25°C, 1 MHz	8	pF

Note:

1. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where this parameter may be affected.*

I_{CC} vs. FREQUENCY

These curves represent the typical power consumption for a particular device at system frequency. The selected "typical" pattern is a 16-bit up-down counter. This pattern fills the device and exercises every macrocell. Maximum frequency shown uses internal feedback and a D-type register. Power/Speed are optimized to obtain the highest counter frequency and the lowest power. The highest frequency (LSBs) is placed in common PAL blocks, which are set to high power. The lowest frequency signals (MSBs) are placed in a common PAL block and set to lowest power.

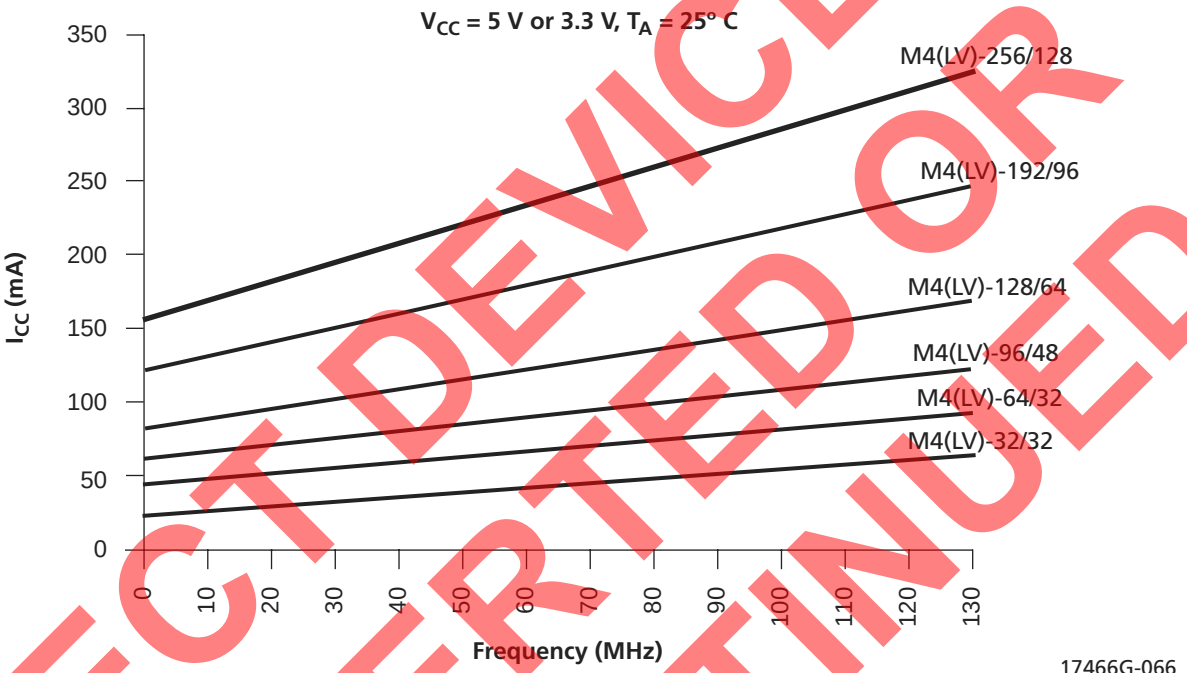

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Figure 18. MACH 4 I_{CC} Curves at High Speed Mode

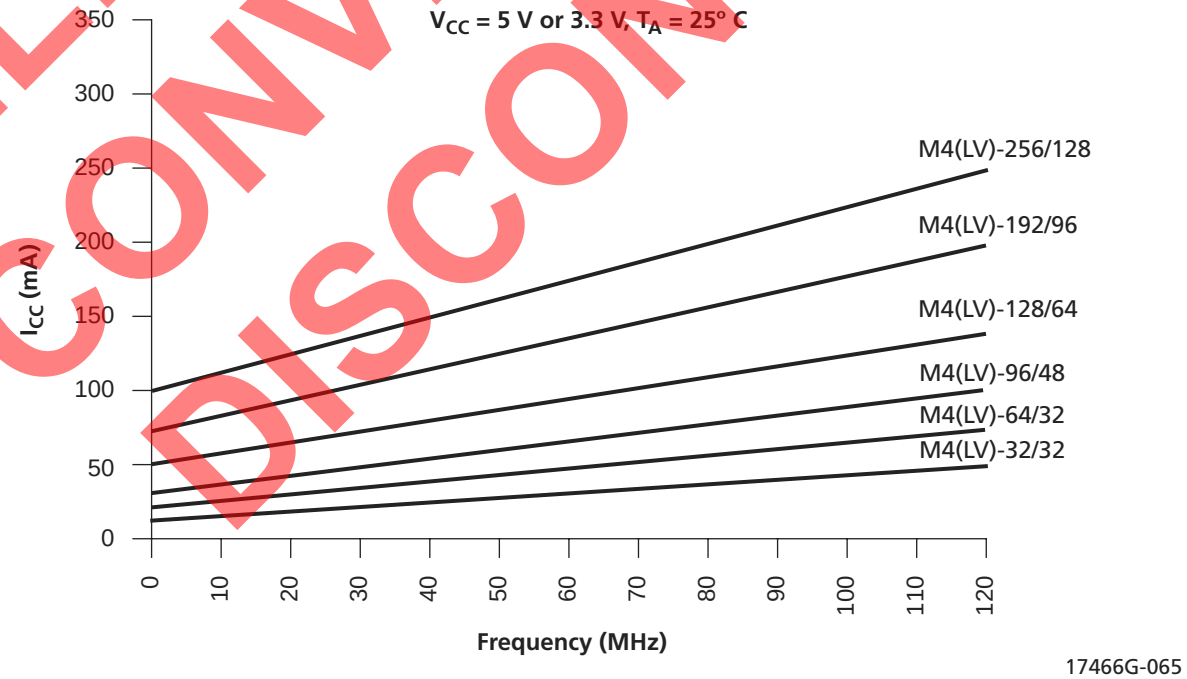

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Figure 19. MACH 4 I_{CC} Curves at Low Power Mode

100-PIN TQFP CONNECTION DIAGRAM (M4(LV)-96/48)

Top View

100-Pin TQFP

17466G-029

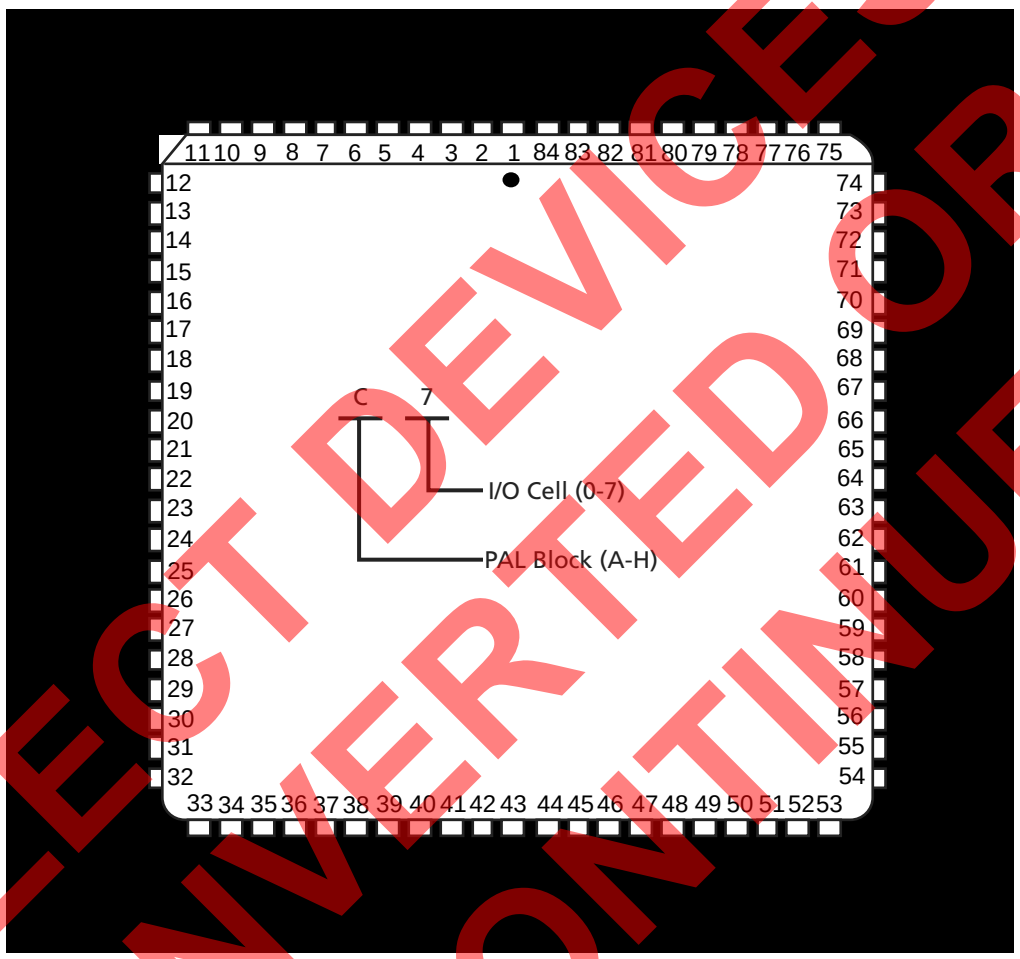
PIN DESIGNATIONS

CLK/I = Clock or Input
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
NC = No Connect
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

84-PIN PLCC CONNECTION DIAGRAM (M4(LV)-128N/64)

Top View

84-Pin PLCC



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Note:
Pin-compatible with the MACH131, MACH231, MACH435.

PIN DESIGNATIONS

CLK/I = Clock or Input

GND = Ground

I = Input

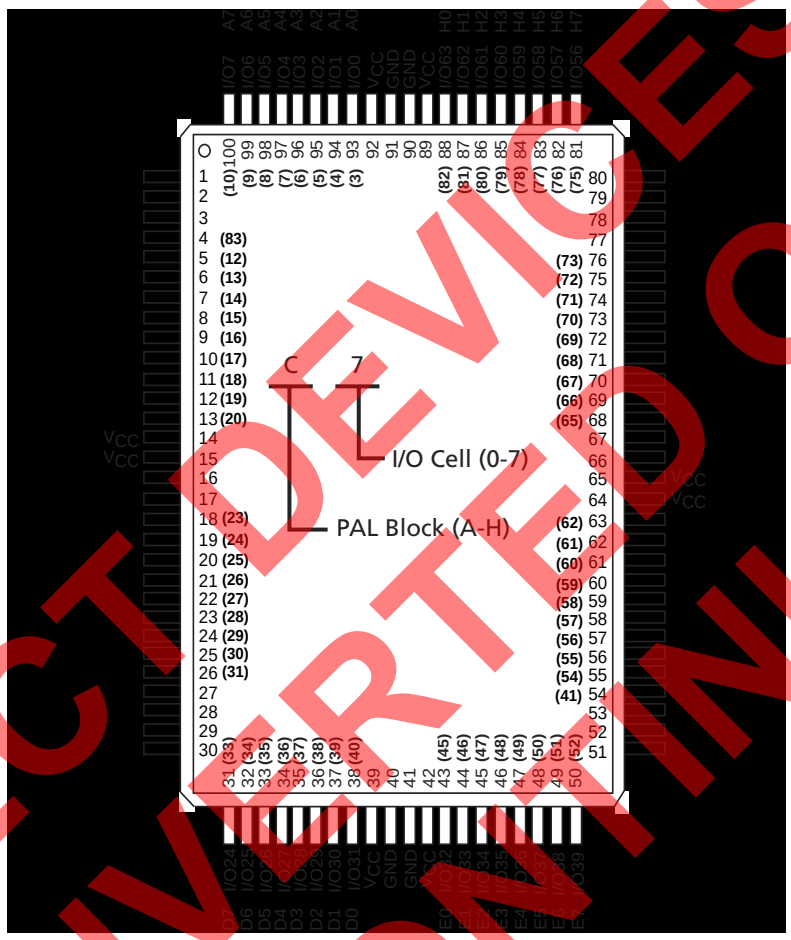
I/O = Input/Output

V_{CC} = Supply Voltage

100-PIN PQFP CONNECTION DIAGRAM (M4(LV)-128/64)

Top View

100-Pin PQFP



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Note:
The numbers in parentheses reflect compatible pin numbers for 84-pin PLCC.

PIN DESIGNATIONS

I/CLK = Input or Clock
GND = Ground
I = Input
I/O = Input/Output
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out
TRST = Test Reset
ENABLE = Program

208-PIN PQFP CONNECTION DIAGRAM (M4(LV)-256/128)

Top View

208-Pin PQFP

17466G-044

17466H-066

256-BALL BGA CONNECTION DIAGRAM (M4LV-256/128)

Bottom View

256-Ball BGA

17466G-045