Renesas Electronics America Inc - M30280F6HP#U5B Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, IEBus, SIO, UART/USART
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	71
Program Memory Size	48KB (48K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30280f6hp-u5b

1.2 Performance Overview

Table 1.1 and **1.2** outline performance overview of the M16C/28 Group (M16C/28, M16C/28B).

Table 1.1 M16C/28 Group (M16C/28, M16C/28) Performance (80/85-Pin Package)

	Item	Performance
CPU	Number of basic instructions	91 instructions
	Minimum instruction excution time	41.7 ns (f(BCLK) = 24 MHz, Vcc = 4.2 V to 5.5 V) (M16C/28B) 50 ns (f(BCLK) = 20 MHz, Vcc = 3.0 V to 5.5 V) (M16C/28, M16C/28B) 100 ns (f(BCLK) = 10 MHz, Vcc= 2.7 V to 5.5 V) (M16C/28, M16C/28B)
	Operation mode	Single chip mode
	Address space	1M bytes
	Memory capacity	See **Table 1.3**
Peripheral Function	I/O port	Input/Output : 71 lines
	Multifunction timer	TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase Motor Control Timer TimerS (Input Capture/Output Compare) : 16bit base timer x 1 channel (Input/Output x 8 channels)
	Serial I/O	2 channels (UART0, UART1) UART, clock synchronous 1 channel (UART2) UART, clock synchronous, I^2C bus(1), or IEbus(2) 2 channels (SI/O3, SI/O4) Clock synchronous 1 channel (Multi-Master I^2C bus(1))
	A/D converter	10 bits x 24 channels
	DMAC	2 channels
	Watchdog timer	15 bits x 1 (with prescaler)
	Interrupt	25 internal and 8 external sources, 4 software sources, 7 levels
	Clock generation circuit	4 circuits • Main clock (*) • Sub-clock (*) • On-chip oscillator • PLL frequency synthesizer (*) Equipped with a built-in feedback resistor
	Oscillation Stop Detect Function	Main clock oscillation stop, re-oscillation detect function
	Voltage detection circuit	Available
Electrical Characteristics	Power supply voltage	Vcc = 4.2 V to 5.5 V (f(BCLK) = 24 MHz) (M16C/28B) Vcc = 3.0 V to 5.5 V (f(BCLK) = 20 MHz) (M16C/28, M16C/28B) Vcc = 2.7 V to 5.5 V (f(BCLK) = 10 MHz) (M16C/28, M16C/28B)
	Power consumption	16 mA (Vcc = 5V, f(BCLK) = 20 MHz) 25 µA (f(XCIN) = 32 KHz on RAM) 3.0 µA (Vcc = 3V, f(XCIN) = 32 KHz, in wait mode) 0.7 µA (Vcc = 3V, in stop mode)
Flash Memory	Program/erase supply voltage	2.7 V to 5.5 V
	Program and erase endurance	100 times (all space) or 1,000 times (Blocks 0 to 5) /10,000 times (Block A, Block B(3))
Operating Ambient Temperature		-20 to 85°C/-40 to 85°C(3)
Package		80-pin plastic mold LQFP, 85-pin plastic mold TFLGA

NOTES:
1. I^2C bus is a trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a trademark of NEC Electronics Corporation.
3. Refer to **Table 1.5** to **1.7** for number of program/erase.
4. Use PLL frequency synthesizer to use M16C/28B at f(BCLK) = 24 MHz.

Table 1.2 M16C/28 Group (M16C/28, M16C/28) (64-Pin Package)

	Item	Performance
CPU	Number of basic instructions	91 instructions
	Minimum instruction excution time	41.7 ns (f(BCLK) = 24 MHZ, VCC = 4.2 V to 5.5 V) (M16C/28B) 50 ns (f(BCLK) = 20 MHZ, VCC = 3.0V to 5.5V) (M16C/28, M16C/28B) 100 ns (f(BCLK) = 10 MHZ, VCC = 2.7V to 5.5V) (M16C/28, M16C/28B)
	Operation mode	Single chip mode
	Address space	1M bytes
	Memory capacity	See **Table 1.3**
Peripheral Function	I/O Port	Input/Output : 55 lines
	Multifunction timer	TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase Motor Control Timer TimerS (Input Capture/Output Compare) : 16bit base timer x 1 channel (Input/Output x 8 channels)
	Serial I/O	2 channels (UART0, UART1) UART, clock synchronous 1 channel (UART2) UART, clock synchronous, I^2C bus(1), or IEbus(2) 1 channels (SI/O3, SI/O4) Clock synchronous 1 channel (Multi-Master I^2C bus(1))
	A/D converter	10 bits x 13 channels
	DMAC	2 channels
	Watchdog timer	15 bits x 1 (with prescaler)
	Interrupt	24 internal and 8 external sources, 4 software sources, 7 levels
	Clock generation circuit	4 circuits • Main clock(*) • Sub-clock(*) • On-chip oscillator • PLL frequency synthesizer (*) Equipped with a built-in feedback resistor
	Oscillation Stop Detect Function	Main clock oscillation stop, re-oscillation detect function
	Voltage detection circuit	Available
Electrical Characteristics	Power supply voltage	Vcc = 4.2 V to 5.5 V (f(BCLK) = 24 MHz) (M16C/28) Vcc = 3.0 V to 5.5 V (f(BCLK) = 20 MHz) (M16C/28, M16C/28B) Vcc = 2.7 V to 5.5 V (f(BCLK) = 10 MHz) (M16C/28, M16C/28B)
	Power consumption	16 mA (Vcc = 5 V, f(BCLK) = 20 MHz) 25 µA (f(XCIN) = 32 KHz on RAM) 3.0 µA (Vcc = 3 V, f(XCIN) = 32 KHz, in wait mode) 0.7 µA (Vcc = 3 V, in stop mode)
Flash Memory	Program/erase supply voltage	2.7 V to 5.5 V
	Program and erase endurance	100 times (all space) or 1,000 times (Blocks 0 to 5) /10,000 times (Block A, Block B(3))
Operating Ambient Temperature		-20 to 85C°/-40 to 85C°(3)
Package		64-pin plastic mold LQFP

NOTES:
1. I^2C bus is a trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a trademark of NEC Electronics Corporation.
3. Refer to **Table 1.5** to **1.7** for number of program/erase.
4. Use PLL frequency synthesizer to use M16C/28B at f(BCLK) = 24 MHz.

1.3 Block Diagram

Figure 1.1 is a block diagram of the M16C/28 Group (M16C/28, M16C/28B), 80-pin and 85-pin package.
Figure 1.2 is a block diagram of the M16C/28 Group (M16C/28, M16C/28B), 64-pin package.

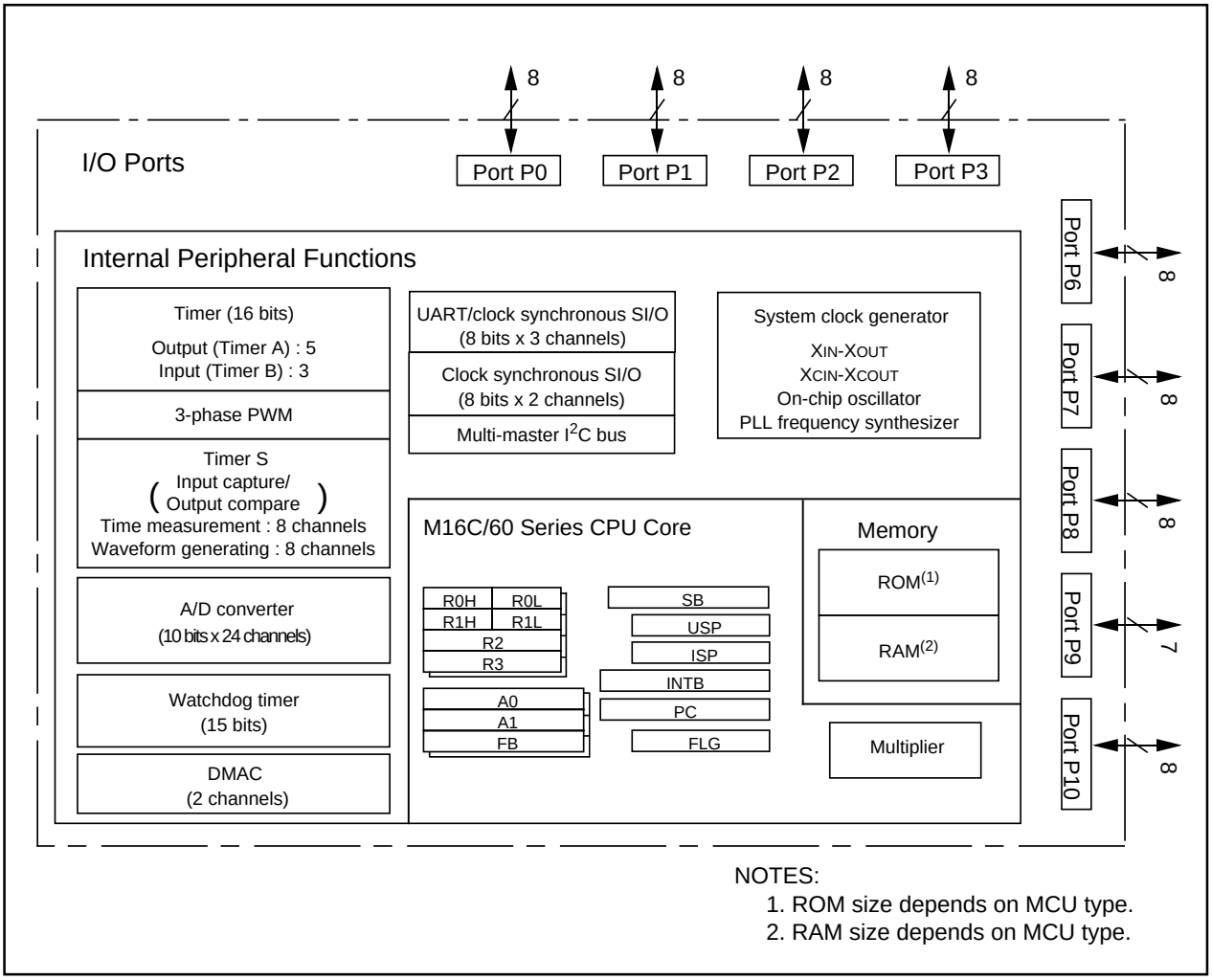


Figure 1.1 M16C/28 Group (M16C/28, M16C/28B), 80-Pin/85-Pin Block Diagram

1.4 Product Information

Tables 1.3 and **1.4** list the M16C/28 Group product information and **Figure 1.3** shows the product numbering system. The specifications are partially different between normal-ver.and T/ V-ver..

Table 1.3 M16C/28 Product List -Normal-ver. **As of September, 2006**

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30280F6WG (N)	48 K + 4 K	4 K	PTLG0085JB-A (85F0G)	Flash Memory	U3, U5, U7, U9
M30280F8WG (N)	64 K + 4 K	4 K			
M30280FAWG (N)	96 K + 4 K	8 K			
M30280F6HP (N)	48 K + 4 K	4 K	PLQP0080KB-A (80P6Q-A)		
M30280F8HP (N)	64 K + 4 K	4 K			
M30280FAHP (N)	96 K + 4 K	8 K			
M30280FCHP (N)	128 K + 4 K	12 K			
M30281F6HP (N)	48 K + 4 K	4 K	PLQP0064KB-A (64P6Q-A)		
M30281F8HP (N)	64 K + 4 K	4 K			
M30281FAHP (N)	96 K + 4 K	8 K			
M30281FCHP (N)	128 K + 4 K	12 K			
M30280M8-XXXHP (N)	64 K	4 K	PLQP0080KB-A (80P6Q-A)	Mask ROM	U3, U5
M30280MA-XXXHP (N)	96 K	8 K			
M30280MC-XXXHP (N)	128 K	12 K			
M30281M8-XXXHP (N)	64 K	4 K	PLQP0064KB-A (64P6Q-A)		
M30281MA-XXXHP (N)	96 K	8 K			
M30281MC-XXXHP (N)	128 K	12 K			

(N): New

Table 1.4 M16C/28B Product List -Normal-ver. **As of September, 2006**

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30280FCBHP (D)	128 K + 4 K	12 K	PLQP0080KB-A (80P6Q-A)	Flash memory	U7
M30281FCBHP (D)	128 K + 4 K	12 K	PLQP0064KB-A (64P6Q-A)		

(D): Under development

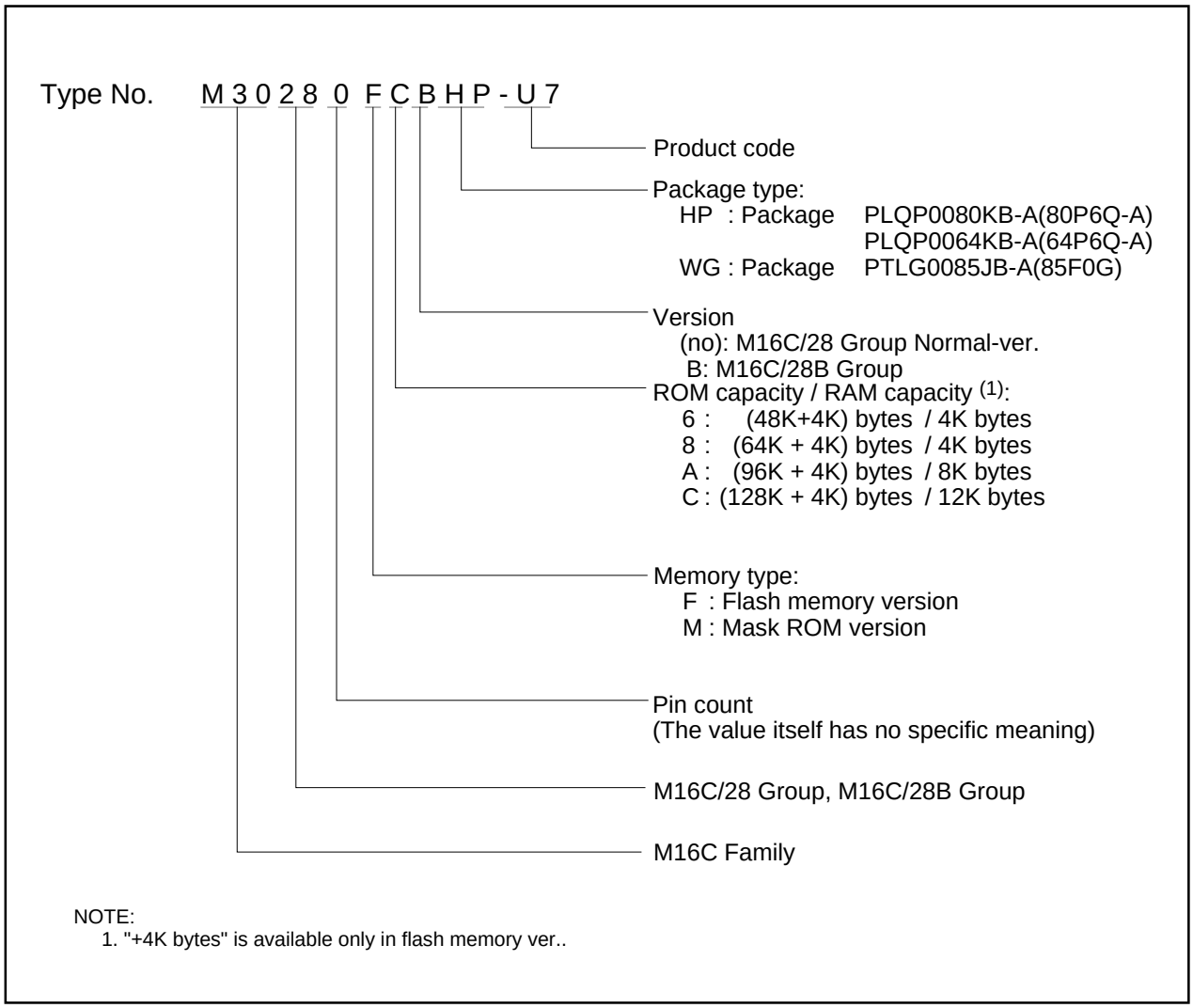
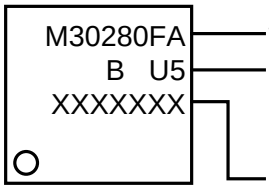


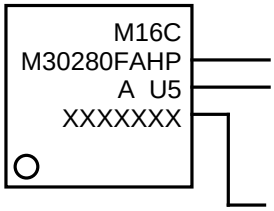
Figure 1.3 Product Numbering System

(1) Flash Memory Version, PTLG0085JB-A (85F0G), Normal-ver.



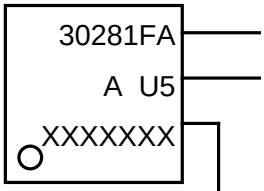
Type No. M30280FAWG
Chip version and product code
B : Chip version.
The first edition is shown to be blank and continues with A, B, and C.
U5 : Product code. (See **Table 1.5**)
Date code seven digits
Manufacturing management code

(2) Flash Memory Version, PLQP0080KB-A (80P6Q-A), Normal-ver.



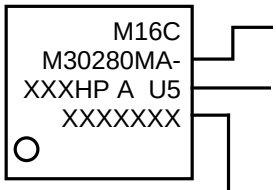
Type No. M30280FAHP
Chip version and product code
A : Chip version and product code(1)
The first edition is shown to be blank and continues with A, B and C.
U5 : Product code. (**Table 1.4**)
Date code seven digits
Manufacturing management code

(3) Flash Memory Version, PLQP0064KB-A (64P6Q-A), Normal-ver.



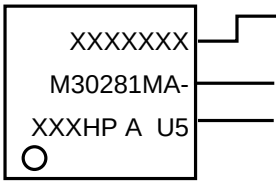
Type No. M30281FAHP
Chip version and product code
A : Chip version and product code(1)
The first edition is shown to be blank and continues with A, B and C.
U5 : Product code. (**Table 1.4**)
Date code seven digits
Manufacturing management code

(4) Mask ROM Version, PLQP0080KB-A (80P6Q-A), Normal-ver.



Type No. M30280MAHP
Chip version and product code
XXX : ROM No.
A : Chip version and product code(1)
The first edition is shown to be blank and continues with A, B and C.
U5 : Product code. (**Table 1.6**)
Date code seven digits
Manufacturing management code

(5) Mask ROM Version, PLQP0064-KB-A (64P6Q-A), Normal-ver.



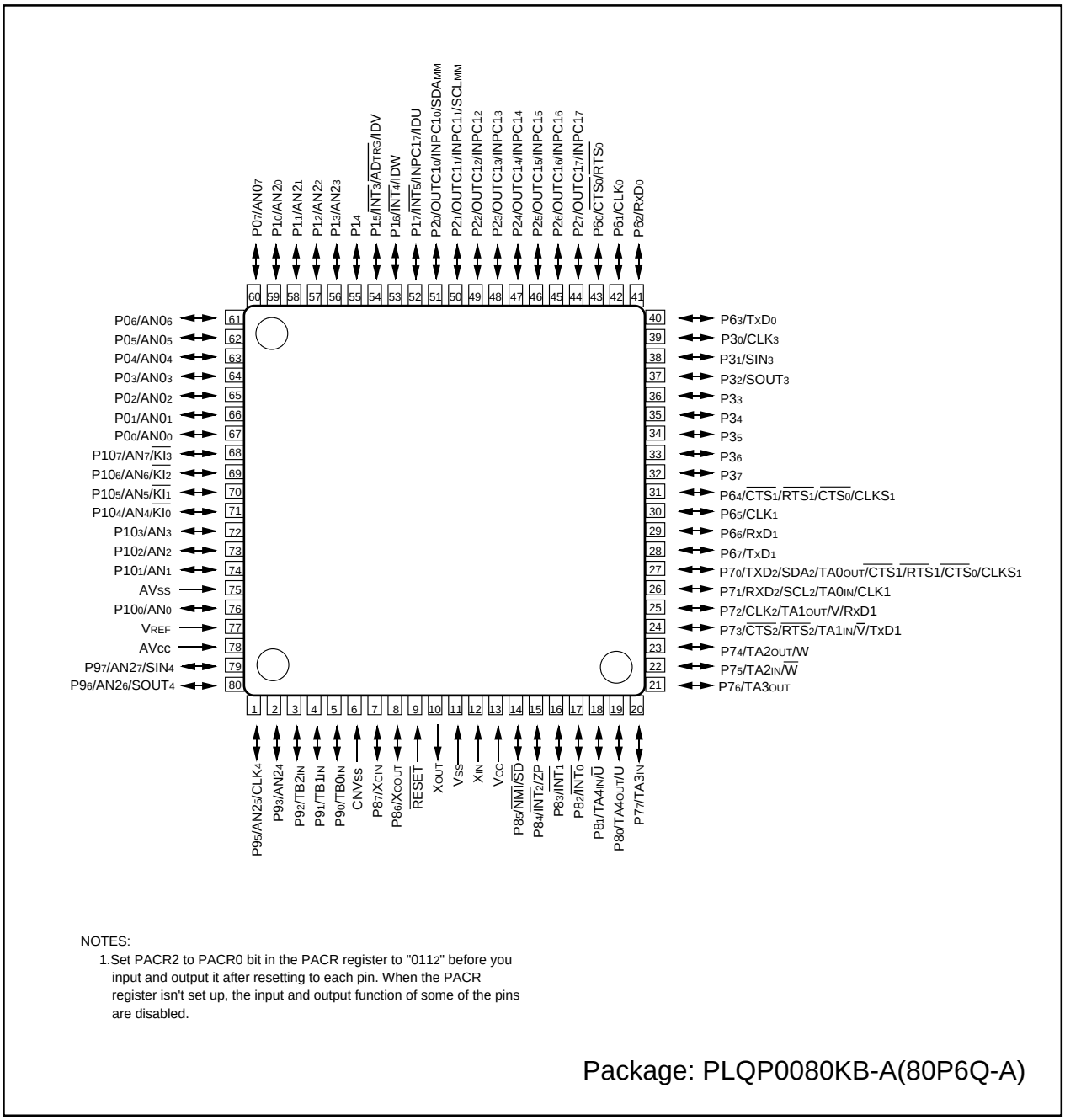
Date code seven digits
Manufacturing management code
Type No. M30281MAHP
Chip version and product code
XXX: ROM No.
A : Chip version and product code(1)
The first edition is shown to be blank and continues with A, B and C.
U5 : Product code. (**Table 1.6**)

NOTES:
1. The following functinos are not available in the first version and version A products.
-Delay trigger mode 0 of A/D conversion
-Delay trigger mode 1 of A/D conversion

Figure 1.4 Marking Diagram-M16C/28 Normal-ver.

Table 1.8 Pin Characteristics for 85-pin Package (continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I²C bus Pin	Analog Pin	PLQP0080KB-A Pin Number
E8		P15	$\overline{INT3}$	IDV				$\overline{ADTRG}$	54
E9		P16	$\overline{INT4}$	IDW					53
E10		P17	$\overline{INT5}$	IDU	INPC17				52
F1	Vcc								13
F2	Vcc								13
F3		P85	$\overline{NMI}$	$\overline{SD}$					14
F8	Vss(1)								(11)
F9		P20			OUTC10 / INPC10		SDAMM		51
F10		P21			OUTC11 / INPC11		SCLMM		50
G1		P84	$\overline{INT2}$	ZP					15
G2		P83	$\overline{INT1}$						16
G3		P82	$\overline{INT0}$						17
G8		P22			OUTC12 / INPC12				49
G9		P23			OUTC13 / INPC13				48
G10		P24			OUTC14 / INPC14				47
H1		P81		TA4IN / $\overline{U}$					18
H2		P80		TA4OUT / U					19
H3		P71		TA0IN		RXD2 / SCL2 / CLK1			26
H4		P66				RXD1			29
H5	Vss(1)								(11)
H6		P35							34
H7		P32				SOUT3			37
H8		P25			OUTC15 / INPC15				46
H9		P26			OUTC16 / INPC16				45
H10		P27			OUTC17 / INPC17				44
J1		P76		TA3OUT					21
J2		P74		TA2OUT / W					23
J3		P72		TA1OUT / V		CLK2 / RXD1			25
J4		P67				TXD1			28
J5		P64				$\overline{RTS1}$ / $\overline{CTS1}$/ $\overline{CTS0}$ / CLKS1			31
J6		P36							33
J7		P33							36
J8		P62				RXD0			41
J9		P60				$\overline{RTS0}$ / $\overline{CTS0}$			43
J10		P61				CLK0			42
K1		P77		TA3IN					20
K2		P75		TA2IN / $\overline{W}$					22
K3		P73		TA1IN / $\overline{V}$		$\overline{CTS2}$ / $\overline{RTS2}$ / $\overline{TXD1}$			24
K4		P70		TA0OUT		$\overline{TXD2}$ / $\overline{SDA2}$ / $\overline{RTS1}$ / $\overline{CTS1}$ / $\overline{CTS0}$ / $\overline{CLKS1}$			27
K5		P65				CLK1			30
K6		P37							32
K7		P34							35
K8		P63				TXD0			40
K9		P30				CLK3			39
K10		P31				SIN3			38



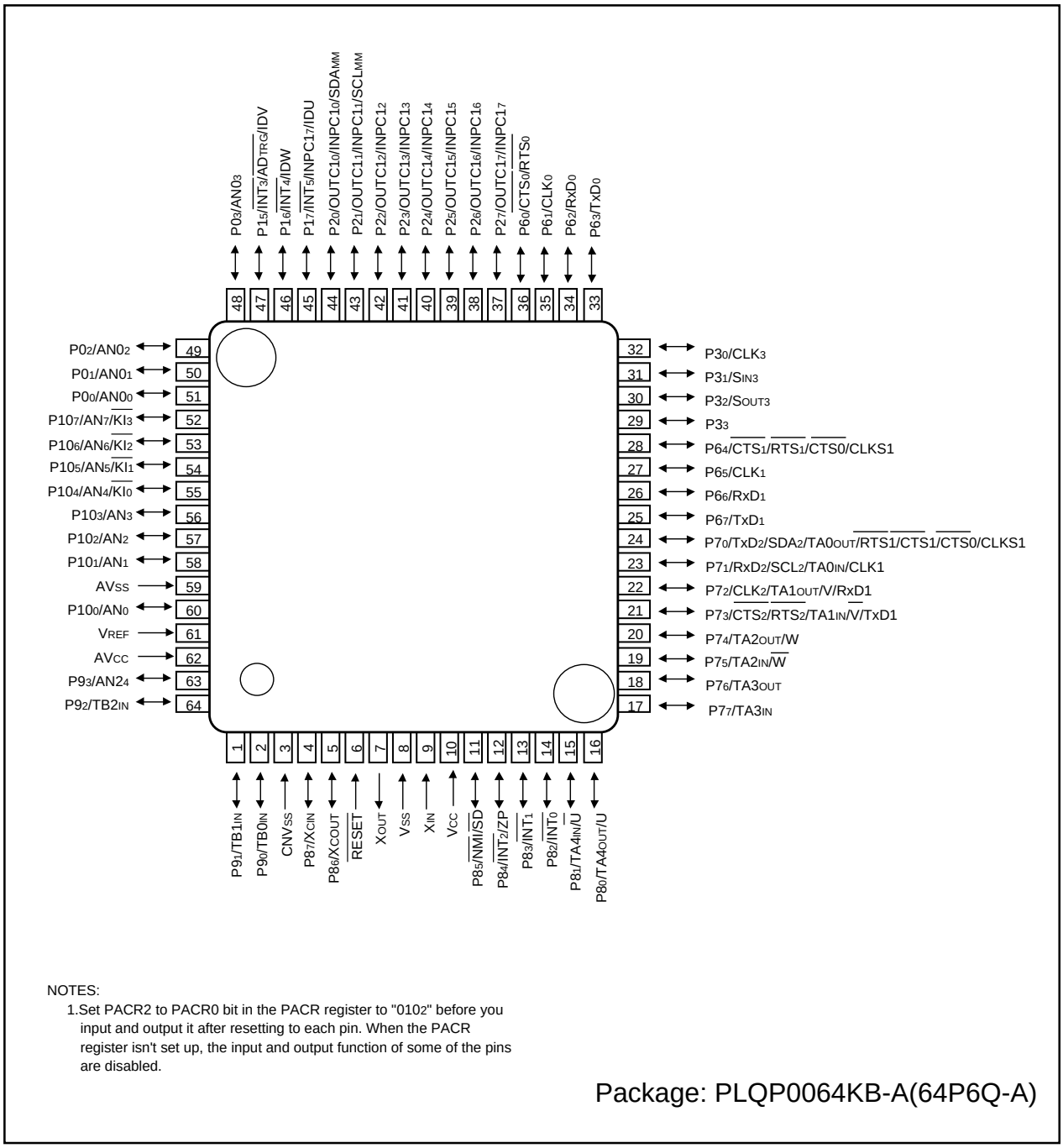
NOTES:
1.Set PACR2 to PACR0 bit in the PACR register to "011₂" before you input and output it after resetting to each pin. When the PACR register isn't set up, the input and output function of some of the pins are disabled.

Package: PLQP0080KB-A(80P6Q-A)

Figure 1.5 Pin Assignment (Top View) of 80-Pin Package

Table 1.9 Pin Characteristics for 80-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I^2C bus Pin	Analog Pin
1		$P9_5$				CLK_4		$AN2_5$
2		$P9_3$						$AN2_4$
3		$P9_2$		TB_{2IN}				
4		$P9_1$		TB_{1IN}				
5		$P9_0$		TB_{0IN}				
6	CNVss							
7	X_{CIN}	$P8_7$						
8	X_{COUT}	$P8_6$						
9	$\overline{RESET}$							
10	X_{OUT}							
11	Vss							
12	X_{IN}							
13	Vcc							
14		$P8_5$	$\overline{NMI}$	$\overline{SD}$				
15		$P8_4$	$\overline{INT_2}$	ZP				
16		$P8_3$	$\overline{INT_1}$					
17		$P8_2$	$\overline{INT_0}$					
18		$P8_1$		TA_{4IN} / $\overline{U}$				
19		$P8_0$		TA_{4OUT} / U				
20		$P7_7$		TA_{3IN}				
21		$P7_6$		TA_{3OUT}				
22		$P7_5$		TA_{2IN} / $\overline{W}$				
23		$P7_4$		TA_{2OUT} / W				
24		$P7_3$		TA_{1IN} / $\overline{V}$		$\overline{CTS_2}$ / $\overline{RTS_2}$ / TxD_1		
25		$P7_2$		TA_{1OUT} / V		CLK_2 / RxD_1		
26		$P7_1$		TA_{0IN}		RxD_2 / SCL_2 / CLK_1		
27		$P7_0$		TA_{0OUT}		TxD_2 / SDA_2 / $\overline{RTS_1}$ / $\overline{CTS_1}$ / $\overline{CTS_0}$ / $CLKS_1$		
28		$P6_7$				TxD_1		
29		$P6_6$				RxD_1		
30		$P6_5$				CLK_1		
31		$P6_4$				RTS_1 / $\overline{CTS_1}$/ $\overline{CTS_0}$ / $CLKS_1$		
32		$P3_7$						
33		$P3_6$						
34		$P3_5$						
35		$P3_4$						
36		$P3_3$						
37		$P3_2$				$SOUT_3$		
38		$P3_1$				SIN_3		
39		$P3_0$				CLK_3		
40		$P6_3$				TxD_0		



NOTES:
1. Set PACR2 to PACR0 bit in the PACR register to "010₂" before you input and output it after resetting to each pin. When the PACR register isn't set up, the input and output function of some of the pins are disabled.

Package: PLQP0064KB-A(64P6Q-A)

Figure 1.6 Pin Assignment (Top View) of 64-Pin Package

1.6 Pin Description

Table 1.10 Pin Description (64-Pin, 80-Pin and 85-Pin Packages)

Classification	Symbol	I/O Type	Function
Power Supply	VCC, VSS	I	Apply 2.7 to 5.5V to the Vcc pin. Apply 0V to the Vss pin.
Analog Power Supply	AVCC AVSS	I	Supplies power to the A/D converter. Connect the AVCC pin to VCC and the AVSS pin to VSS.
Reset Input	$\overline{\text{RESET}}$	I	The MCU is in a reset state when "L" is applied to the $\overline{\text{RESET}}$ pin
CNVSS	CNVSS	I	Connect the CNVSS pin to VSS.
Main Clock Input	XIN	I	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, apply it to XIN and leave XOUT open. If XIN is not used (for external oscillator or external clock) connect XIN pin to VCC and leave XOUT open.
Main Clock Output	XOUT	O	
Sub Clock Input	XCIN	I	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT.
Sub Clock Output	XCOUT	O	
$\overline{\text{INT}}$ Interrupt Input	$\overline{\text{INT0}}$ to $\overline{\text{INT5}}$	I	Input pins for the $\overline{\text{INT}}$ interrupt. $\overline{\text{INT2}}$ can be used for Timer A Z-phase function.
$\overline{\text{NMI}}$ Interrupt Input	$\overline{\text{NMI}}$	I	Input pin for the $\overline{\text{NMI}}$ interrupt. $\overline{\text{NMI}}$ cannot be used as I/O port while the three-phase motor control is enabled. Apply a stable "H" to $\overline{\text{NMI}}$ after setting it's direction register to "0" when the three-phase motor control is enabled.
Key Input Interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	I/O pins for the timer A0 to A4
	TA0IN to TA4IN	I	Input pins for the timer A0 to A4
	ZP	I	Input pin for Z-phase
Timer B	TB0IN to TB2IN	I	Input pins for the timer B0 to B2
Three-phase Motor Control Timer Output	U, $\overline{\text{U}}$, V, $\overline{\text{V}}$, W, $\overline{\text{W}}$	O	Output pins for the three-phase motor control timer
	IDU, IDW, IDV, $\overline{\text{SD}}$	I/O	Input and output pins for the three-phase motor control timer
Serial I/O	$\overline{\text{CTS0}}$ to $\overline{\text{CTS2}}$	I	Input pins for data transmission control
	$\overline{\text{RTS0}}$ to $\overline{\text{RTS2}}$	O	Output pins for data reception control
	CLK0 to CLK3	I/O	Inputs and outputs the transfer clock
	RxD0 to RxD2	I	Inputs serial data
	TxD0 to TxD2	O	Outputs serial data
	CLKS1	O	Output pin for transfer clock
I^2C Mode	SDA2	I/O	Inputs and outputs serial data
	SCL2		Inputs and outputs the transfer clock
Multi-master I^2C bus	SDAMM	I/O	Inputs and outputs serial data
	SCLMM		Inputs and outputs the transfer clock
Reference Voltage Input	VREF	I	Applies reference voltage to the A/D converter
A/D Converter	AN0 to AN7 AN00 to AN03 AN24	I	Analog input pins for the A/D converter
	$\overline{\text{ADTRG}}$		Input pin for an external A/D trigger

I : Input O : Output I/O : Input and output

Table 1.10 Pin Description (64-Pin, 80-Pin and 85-Pin Packages) (Continued)

Classification	Symbol	I/O Type	Function
Timer S	$INPC1_0$ to $INPC1_7$	I	Input pins for the time measurement function
	$OUTC1_0$ to $OUTC1_7$	O	Output pins for the waveform generating function
I/O Ports	$P0_0$ to $P0_3$ $P1_5$ to $P1_7$ $P2_0$ to $P2_7$ $P3_0$ to $P3_3$ $P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P8_0$ to $P8_7$ $P10_0$ to $P10_7$	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 4-bit units
	$P9_0$ to $P9_3$	I/O	I/O ports having equivalent functions to P0

I : Input O : Output I/O : Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The register bank is comprised of 7 registers (R0, R1, R2, R3, A0, A1 and FB) out of 13 CPU registers. Two sets of register banks are provided.

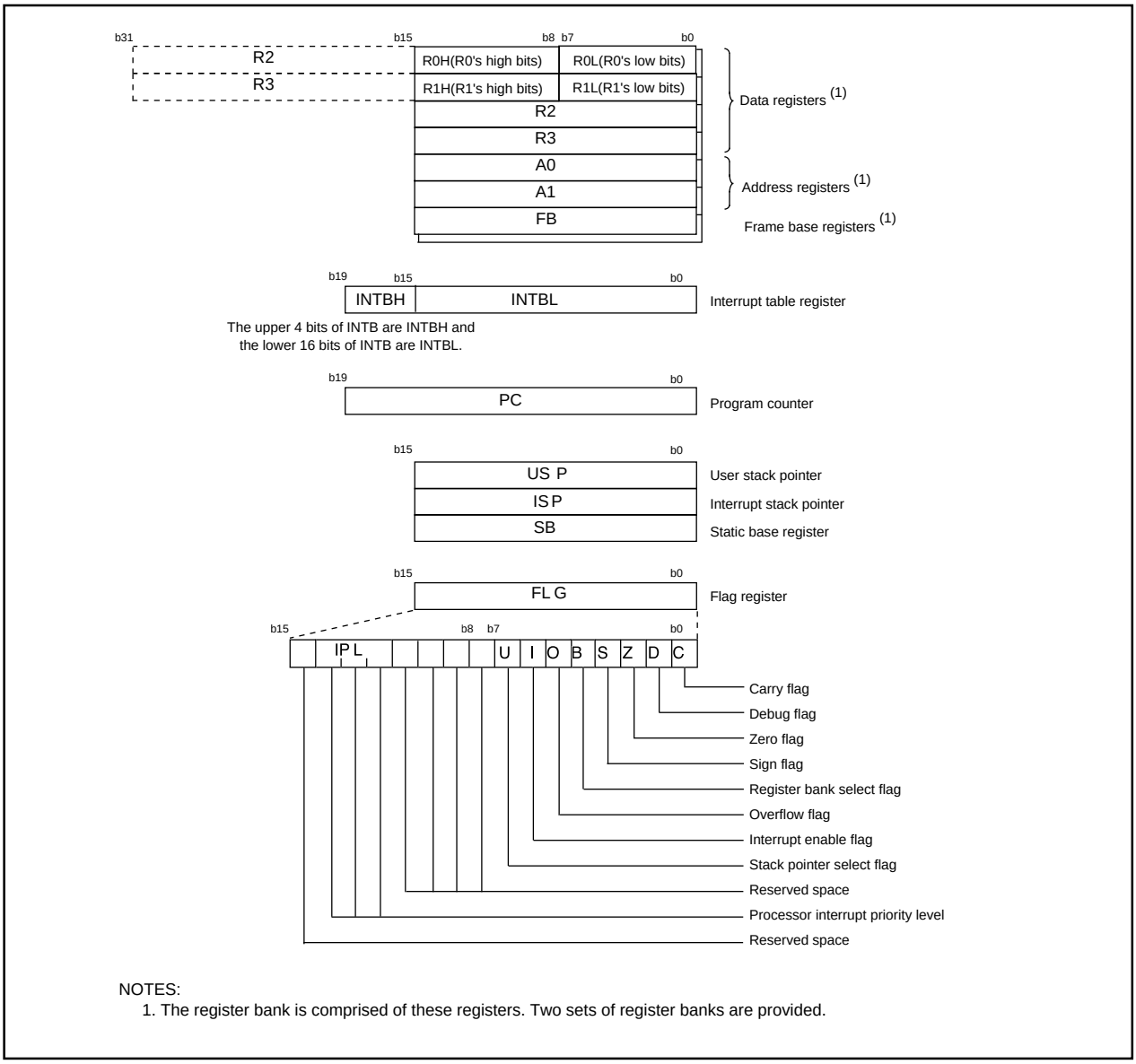


Figure 2.1 Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0, R1, R2 and R3 registers are 16 bit registers for transfer and arithmetic/logic operations.

The R0 and R1 registers can be split into high-order bits(R0H, R1H) and low-order bits (R0L, R1L) to be used seperately as 8-bit data registers. Conversely, R2 and R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R1 and R2.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and arithmetic/logic operations. A1 is the same as A0. In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to 0.

2.8.3 Zero Flag (Z Flag)

This flag is set to 1 when an arithmetic operation resulted in 0; otherwise, it is 0.

2.8.4 Sign Flag (S Flag)

This flag is set to 1 when an arithmetic operation resulted in a negative value; otherwise, it is 0.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is 0 ; register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O Flag)

This flag is set to 1 when the operation resulted in an overflow; otherwise, it is 0.

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1. The I flag is cleared to 0 when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is 0; USP is selected when the U flag is 1.

The U flag is cleared to 0 when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write 0. When read, its content is indeterminate.

3. Memory

Figure 3.1 is a memory map of the M16C/28 Group (M16C/28, M16C/28B). M16C/28 Group provides 1-Mbyte address space from addresses 00000$_{16}$ to FFFFF$_{16}$. The internal ROM is allocated lower addresses beginning with address FFFFF$_{16}$. For example, 64 Kbytes internal ROM is allocated addresses F0000$_{16}$ to FFFFF$_{16}$.

Two 2-Kbyte internal ROM areas, block A and block B, are available in the flash memory version. The blocks are allocated addresses F000$_{16}$ to FFFF$_{16}$.

The fixed interrupt vector tables are allocated addresses FFFDC$_{16}$ to FFFFF$_{16}$. It stores the starting address of each interrupt routine. See the section on interrupts for details.

The internal RAM is allocated higher addresses beginning with address 00400$_{16}$. For example, 4-Kbytes internal RAM is allocated addresses 00400$_{16}$ to 013FF$_{16}$. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowledged.

SFR, consisting of control registers for peripheral functions such as I/O port, A/D converter, serial I/O, timers is allocated addresses 00000$_{16}$ to 003FF$_{16}$. All blank spaces within SFR are reserved and cannot be accessed by users.

The special page vector table is allocated to the addresses FFE00$_{16}$ to FFFDB$_{16}$. This vector is used by the JMPS or JSRS instruction. For details, refer to the ***M16C/60 and M16C/20 Series Software Manual***.

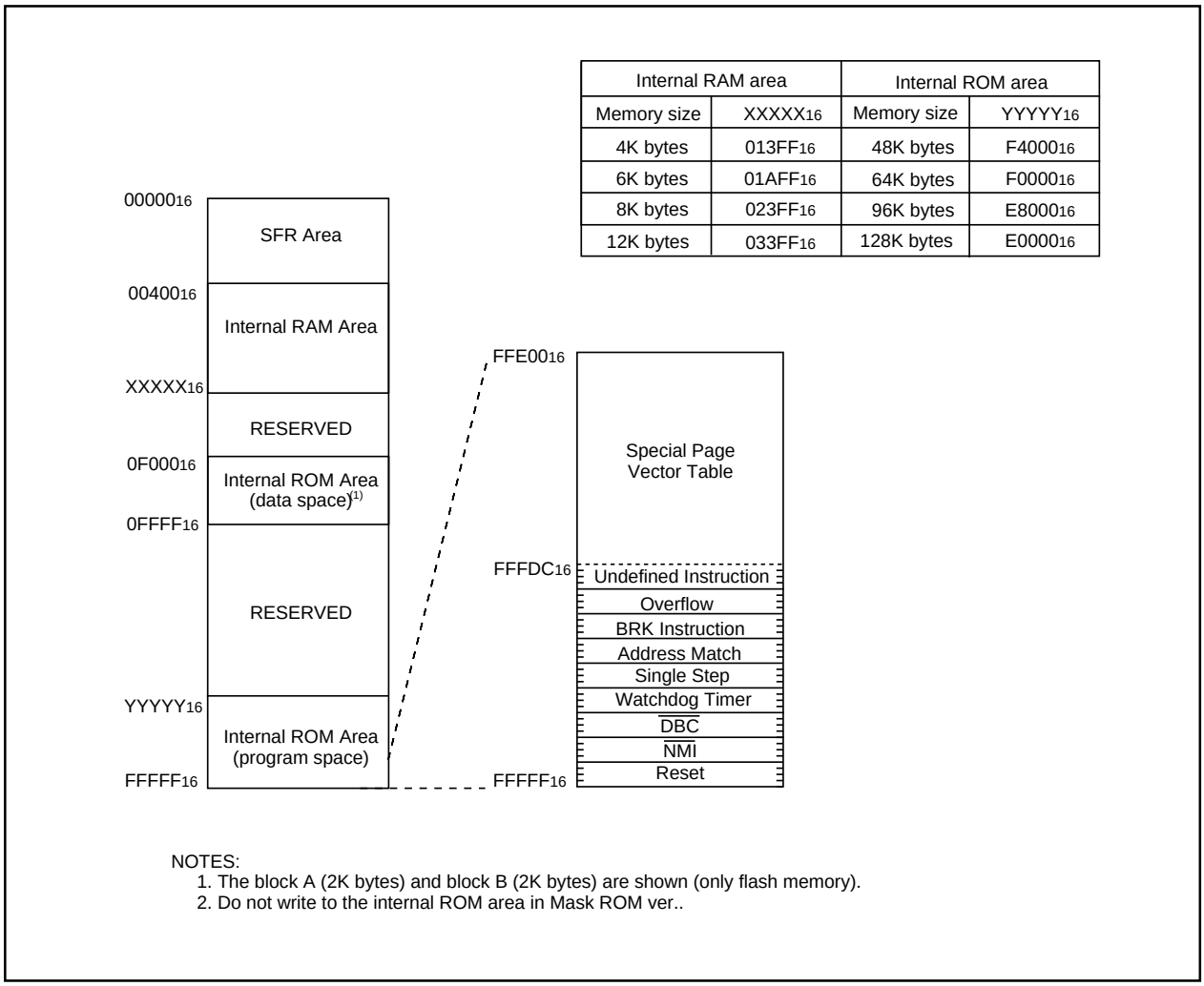


Figure 3.1 Memory Map

4. Special Function Register (SFR)

SFR (Special Function Register) is the control register of peripheral functions. **Tables 4.1** to **4.7** list the SFR information.

Table 4.1 SFR Information(1)[1]

Address	Register	Symbol	After Reset
0000₁₆			
0001₁₆			
0002₁₆			
0003₁₆			
0004₁₆	Processor mode register 0	PM0	00₁₆
0005₁₆	Processor mode register 1	PM1	00001000₂
0006₁₆	System clock control register 0	CM0	01001000₂
0007₁₆	System clock control register 1	CM1	00100000₂
0008₁₆			
0009₁₆	Address match interrupt enable register	AIER	XXXXXX00₂
000A₁₆	Protect register	PRCR	XX000000₂
000B₁₆			
000C₁₆	Oscillation stop detection register [2]	CM2	0X000010₂
000D₁₆			
000E₁₆	Watchdog timer start register	WDTS	XX₁₆
000F₁₆	Watchdog timer control register	WDC	00XXXXX₂
0010₁₆	Address match interrupt register 0	RMAD0	00₁₆
0011₁₆			00₁₆
0012₁₆			X0₁₆
0013₁₆			
0014₁₆	Address match interrupt register 1	RMAD1	00₁₆
0015₁₆			00₁₆
0016₁₆			X0₁₆
0017₁₆			
0018₁₆			
0019₁₆	Voltage detection register 1 [3]	VCR1	00001000₂
001A₁₆	Voltage detection register 2 [3]	VCR2	00₁₆
001B₁₆			
001C₁₆	PLL control register 0	PLC0	0001X010₂
001D₁₆			
001E₁₆	Processor mode register 2	PM2	XXX00000₂
001F₁₆	Low voltage detection interrupt register	D4INT	00₁₆
0020₁₆	DMA0 source pointer	SAR0	XX₁₆
0021₁₆			XX₁₆
0022₁₆			XX₁₆
0023₁₆			
0024₁₆	DMA0 destination pointer	DAR0	XX₁₆
0025₁₆			XX₁₆
0026₁₆			XX₁₆
0027₁₆			
0028₁₆	DMA0 transfer counter	TCR0	XX₁₆
0029₁₆			XX₁₆
002A₁₆			
002B₁₆			
002C₁₆	DMA0 control register	DM0CON	00000X00₂
002D₁₆			
002E₁₆			
002F₁₆			
0030₁₆	DMA1 source pointer	SAR1	XX₁₆
0031₁₆			XX₁₆
0032₁₆			XX₁₆
0033₁₆			
0034₁₆	DMA1 destination pointer	DAR1	XX₁₆
0035₁₆			XX₁₆
0036₁₆			XX₁₆
0037₁₆			
0038₁₆	DMA1 transfer counter	TCR1	XX₁₆
0039₁₆			XX₁₆
003A₁₆			
003B₁₆			
003C₁₆	DMA1 control register	DM1CON	00000X00₂
003D₁₆			
003E₁₆			
003F₁₆			

NOTES:
1. The blank spaces are reserved. No access is allowed.
2. The CM20, CM21, and CM27 bits do not change at oscillation stop detection reset.
3. This register does not change at software reset, watchdog timer reset and oscillation stop detection reset.

X : Undefined

Table 4.3 SFR Information(3)(1)

Address	Register	Symbol	After Reset
≈			≈
01B0₁₆			
01B1₁₆			
01B2₁₆			
01B3₁₆	Flash memory control register 4 (2)	FMR4	01000000₂
01B4₁₆			
01B5₁₆	Flash memory control register 1 (2)	FMR1	000XXX0X₂
01B6₁₆			
01B7₁₆	Flash memory control register 0 (2)	FMR0	00000001₂
01B8₁₆			
01B9₁₆			
≈			≈
0210₁₆	Low-power Consumption Control 0	LPCC0	X0000001₂
0211₁₆			
0212₁₆			
0213₁₆			
0214₁₆			
0215₁₆			
0216₁₆			
0217₁₆			
0218₁₆			
0219₁₆			
≈			≈
0250₁₆			
0251₁₆			
0252₁₆			
0253₁₆			
0254₁₆			
0255₁₆			
0256₁₆			
0257₁₆			
0258₁₆			
0259₁₆			
025A₁₆			
025B₁₆			
025C₁₆	On-chip oscillator control register	ROCR	X0000101₂
025D₁₆	Pin assignment control register	PACR	00₁₆
025E₁₆	Peripheral clock select register	PCLKR	00000011₂
025F₁₆	Low-power Consumption Control 1	LPCC1	00₁₆
≈			≈
02E0₁₆	I^2C0 data shift register	S00	XX₁₆
02E1₁₆			
02E2₁₆	I^2C0 address register	S0D0	00₁₆
02E3₁₆	I^2C0 control register 0	S1D0	00₁₆
02E4₁₆	I^2C0 clock control register	S20	00₁₆
02E5₁₆	I^2C0 start/stop condition control register	S2D0	00011010₂
02E6₁₆	I^2C0 control register 1	S3D0	00110000₂
02E7₁₆	I^2C0 control register 2	S4D0	00₁₆
02E8₁₆	I^2C0 status register	S10	0001000X₂
02E9₁₆			
02EA₁₆			
≈			≈
02FE₁₆			
02FF₁₆			

Note 1:The blank spaces are reserved. No access is allowed.
Note 2:This register is included in the flash memory version.

X : Undefined

Table 4.4 SFR Information(4)(1)

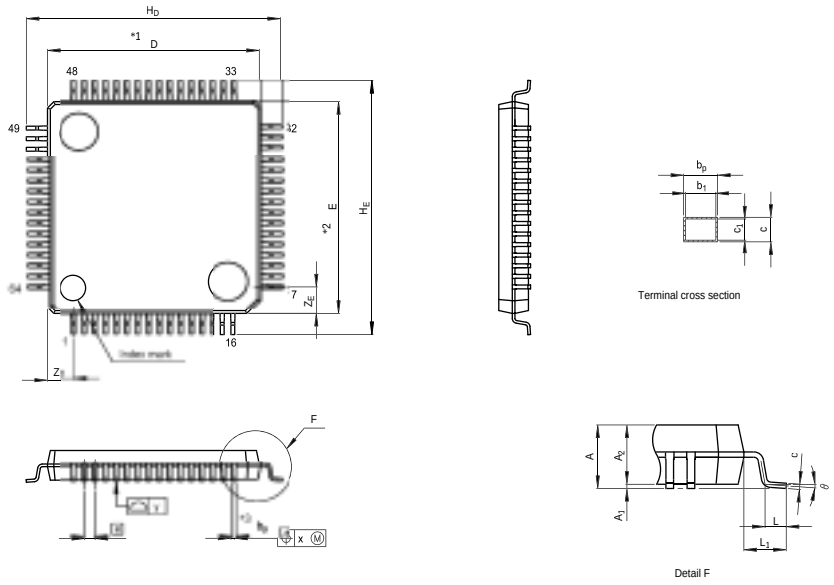
Address	Register	Symbol	After Reset
0300₁₆	TM, WG register 0	G1TM0, G1PO0	XX₁₆
0301₁₆			XX₁₆
0302₁₆	TM, WG register 1	G1TM1, G1PO1	XX₁₆
0303₁₆			XX₁₆
0304₁₆	TM, WG register 2	G1TM2, G1PO2	XX₁₆
0305₁₆			XX₁₆
0306₁₆	TM, WG register 3	G1TM3, G1PO3	XX₁₆
0307₁₆			XX₁₆
0308₁₆	TM, WG register 4	G1TM4, G1PO4	XX₁₆
0309₁₆			XX₁₆
030A₁₆	TM, WG register 5	G1TM5, G1PO5	XX₁₆
030B₁₆			XX₁₆
030C₁₆	TM, WG register 6	G1TM6, G1PO6	XX₁₆
030D₁₆			XX₁₆
030E₁₆	TM, WG register 7	G1TM7, G1PO7	XX₁₆
030F₁₆			XX₁₆
0310₁₆	WG control register 0	G1POCR0	0X00XX00₂
0311₁₆	WG control register 1	G1POCR1	0X00XX00₂
0312₁₆	WG control register 2	G1POCR2	0X00XX00₂
0313₁₆	WG control register 3	G1POCR3	0X00XX00₂
0314₁₆	WG control register 4	G1POCR4	0X00XX00₂
0315₁₆	WG control register 5	G1POCR5	0X00XX00₂
0316₁₆	WG control register 6	G1POCR6	0X00XX00₂
0317₁₆	WG control register 7	G1POCR7	0X00XX00₂
0318₁₆	TM control register 0	G1TMCR0	00₁₆
0319₁₆	TM control register 1	G1TMCR1	00₁₆
031A₁₆	TM control register 2	G1TMCR2	00₁₆
031B₁₆	TM control register 3	G1TMCR3	00₁₆
031C₁₆	TM control register 4	G1TMCR4	00₁₆
031D₁₆	TM control register 5	G1TMCR5	00₁₆
031E₁₆	TM control register 6	G1TMCR6	00₁₆
031F₁₆	TM control register 7	G1TMCR7	00₁₆
0320₁₆	Base timer register	G1BT	XX₁₆
0321₁₆			XX₁₆
0322₁₆	Base timer control register 0	G1BCR0	00₁₆
0323₁₆	Base timer control register 1	G1BCR1	00₁₆
0324₁₆	TM prescale register 6	G1TPR6	00₁₆
0325₁₆	TM prescale register 7	G1TPR7	00₁₆
0326₁₆	Function enable register	G1FE	00₁₆
0327₁₆	Function select register	G1FS	00₁₆
0328₁₆	Base timer reset register	G1BTRR	XX₁₆
0329₁₆			XX₁₆
032A₁₆	Divider register	G1DV	00₁₆
032B₁₆			
032C₁₆			
032D₁₆			
032E₁₆			
032F₁₆			
0330₁₆	Interrupt request register	G1IR	XX₁₆
0331₁₆	Interrupt enable register 0	G1IE0	00₁₆
0332₁₆	Interrupt enable register 1	G1IE1	00₁₆
0333₁₆			
0334₁₆			
0335₁₆			
0336₁₆			
0337₁₆			
0338₁₆			
0339₁₆			
033A₁₆			
033B₁₆			
033C₁₆			
033D₁₆			
033E₁₆	NMI digital debounce register	NDDR	FF₁₆
033F₁₆	P17 digital debounce register	P17DDR	FF₁₆

Note 1:The blank spaces are reserved. No access is allowed.

X : Undefined

Appendix 1. Package Dimensions

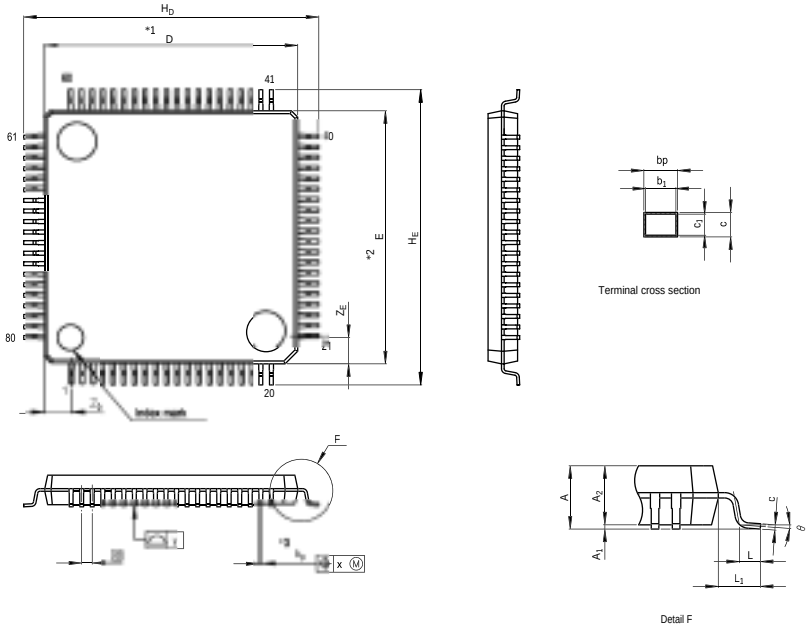
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP64-10x10-0.50	PLQP0064KB-A	64P6Q-A / FP-64K / FP-64KV	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A_2	—	1.4	—
H_D	11.8	12.0	12.2
H_E	11.8	12.0	12.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

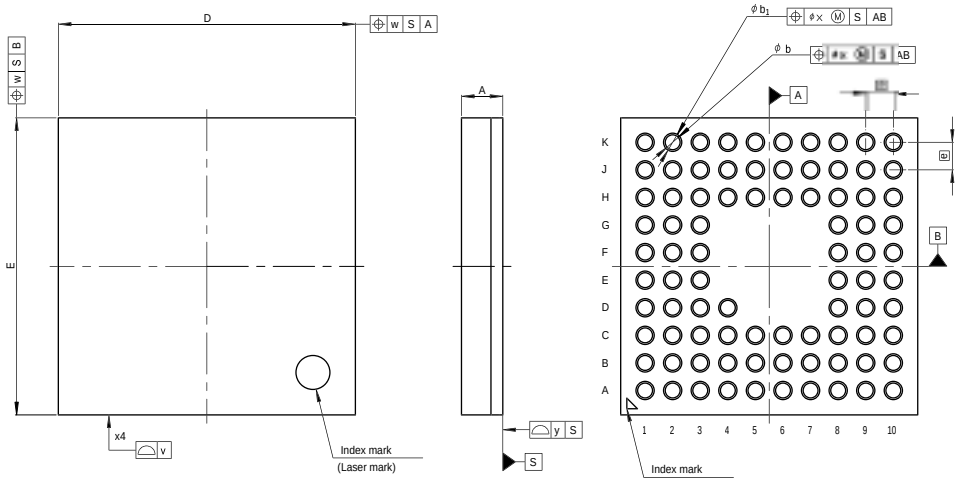
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA85-7x7-0.65	PTLG0085JB-A	85F0G	0.1g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.65	—
b	0.31	0.35	0.39
b_1	0.39	0.43	0.47
x	—	—	0.08
y	—	—	0.10