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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | M16C/60 |
| Core Size | 16-Bit |
| Speed | 20MHz |
| Connectivity | I²C, IEBus, SIO, UART/USART |
| Peripherals | DMA, POR, PWM, Voltage Detect, WDT |
| Number of I/O | 71 |
| Program Memory Size | 48KB (48K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | A/D 24x10b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 80-LQFP |
| Supplier Device Package | 80-LQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/m30280f6hp-u9b |

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Rev.0.50
2006.09.15

# 1. Overview

The M16C/28 Group (M16C/28 and M16C/28B) MCU are single-chip control MCU, fabricated using high-performance silicon gate CMOS technology with the M16C/60 series CPU core. The M16C/28 Group (M16C/28 and M16C/28B) are housed in 64-pin and 80-pin plastic molded LQFP packages and also in 85-pin plastic molded TFLGA (Thin Fine Pitch Land Grid Array) package. With a 1-Mbyte address space, this MCU combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed. It includes a multiplier and DMAC adequate for office automation, communication devices and other high-speed processing applications.

The M16C/28 has Normal-ver., T-ver., and V-ver.. The M16C/28B has Normal-ver. only.

This hardware manual describes the Normal-ver. only. Please contact Renesas Technology Corp. for T-ver./V-ver. information.

## 1.1 Applications

Audio, cameras, office equipment, communication equipment, portable equipment, home appliances (in-verter solution), motor control, industrial equipment, etc.

**Table 1.2 M16C/28 Group (M16C/28, M16C/28) (64-Pin Package)**

| | Item | Performance |
|---|---|---|
| CPU | Number of basic instructions | 91 instructions |
| | Minimum instruction excution time | 41.7 ns (f(BCLK) = 24 MHZ, VCC = 4.2 V to 5.5 V) (M16C/28B)<br>50 ns (f(BCLK) = 20 MHZ, VCC = 3.0V to 5.5V) (M16C/28, M16C/28B)<br>100 ns (f(BCLK) = 10 MHZ, VCC = 2.7V to 5.5V) (M16C/28, M16C/28B) |
| | Operation mode | Single chip mode |
| | Address space | 1M bytes |
| | Memory capacity | See **Table 1.3** |
| Peripheral Function | I/O Port | Input/Output : 55 lines |
| | Multifunction timer | TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels<br>Three-phase Motor Control Timer<br>TimerS (Input Capture/Output Compare)<br>: 16bit base timer x 1 channel (Input/Output x 8 channels ) |
| | Serial I/O | 2 channels (UART0, UART1)<br>UART, clock synchronous<br>1 channel (UART2)<br>UART, clock synchronous, $I^2C$ bus(1), or IEbus(2)<br>1 channels (SI/O3, SI/O4)<br>Clock synchronous<br>1 channel (Multi-Master $I^2C$ bus(1)) |
| | A/D converter | 10 bits x 13 channels |
| | DMAC | 2 channels |
| | Watchdog timer | 15 bits x 1 (with prescaler) |
| | Interrupt | 24 internal and 8 external sources, 4 software sources, 7 levels |
| | Clock generation circuit | 4 circuits<br>• Main clock(*)<br>• Sub-clock(*)<br>• On-chip oscillator<br>• PLL frequency synthesizer<br>(*) Equipped with a built-in feedback resistor |
| | Oscillation Stop Detect Function | Main clock oscillation stop, re-oscillation detect function |
| | Voltage detection circuit | Available |
| Electrical Characteristics | Power supply voltage | Vcc = 4.2 V to 5.5 V (f(BCLK) = 24 MHz) (M16C/28)<br>Vcc = 3.0 V to 5.5 V (f(BCLK) = 20 MHz) (M16C/28, M16C/28B)<br>Vcc = 2.7 V to 5.5 V (f(BCLK) = 10 MHz) (M16C/28, M16C/28B) |
| | Power consumption | 16 mA (Vcc = 5 V, f(BCLK) = 20 MHz)<br>25 µA (f(XCIN) = 32 KHz on RAM)<br>3.0 µA (Vcc = 3 V, f(XCIN) = 32 KHz, in wait mode)<br>0.7 µA (Vcc = 3 V, in stop mode) |
| Flash Memory | Program/erase supply voltage | 2.7 V to 5.5 V |
| | Program and erase endurance | 100 times (all space) or 1,000 times (Blocks 0 to 5)<br>/10,000 times (Block A, Block B(3)) |
| Operating Ambient Temperature | | -20 to 85C°/-40 to 85C°(3) |
| Package | | 64-pin plastic mold LQFP |

NOTES:
1. $I^2C$ bus is a trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a trademark of NEC Electronics Corporation.
3. Refer to **Table 1.5** to **1.7** for number of program/erase.
4. Use PLL frequency synthesizer to use M16C/28B at f(BCLK) = 24 MHz.

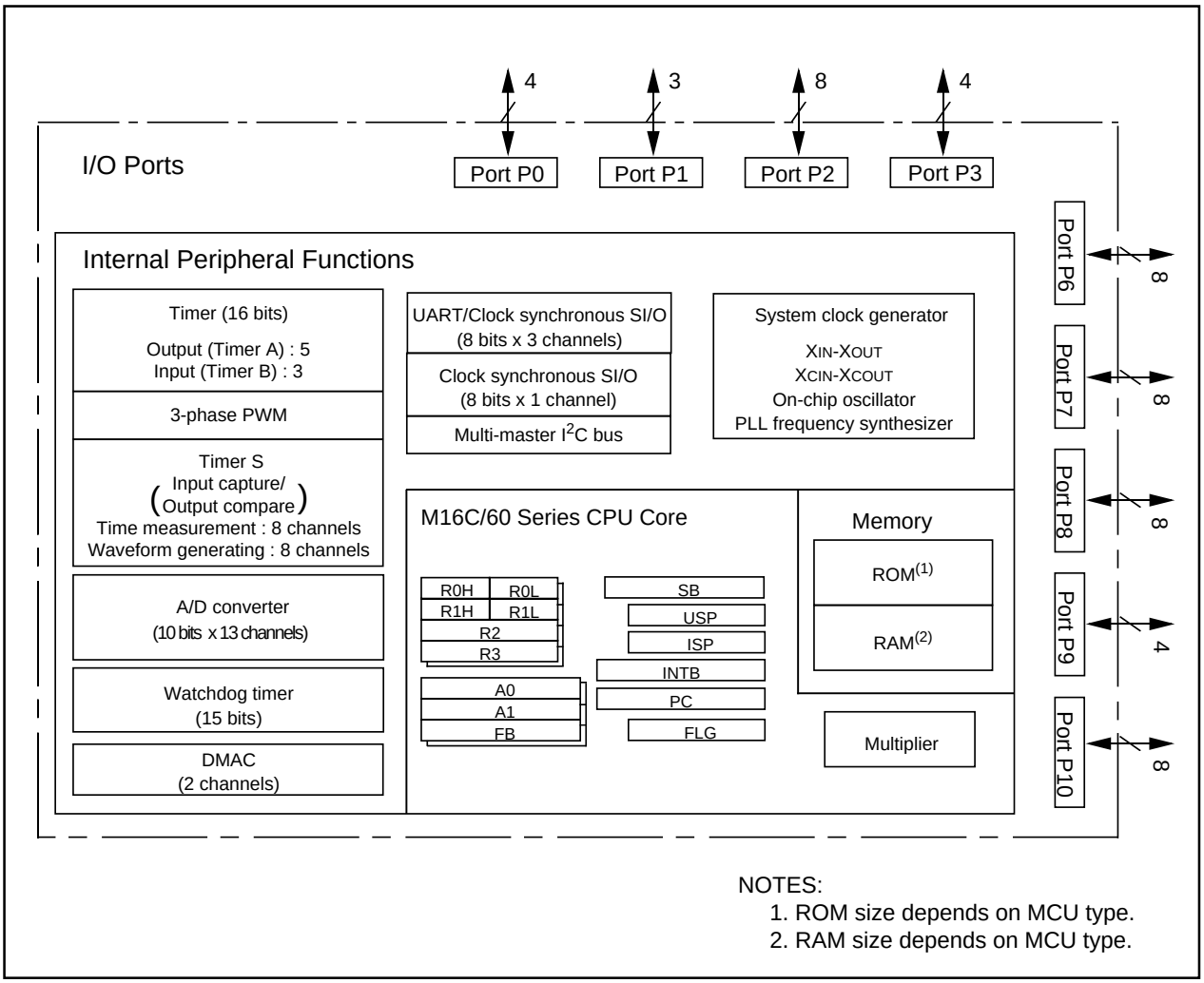



**Figure 1.2 M16C/28 Group (M16C/28, M16C/28B), 64-Pin Block Diagram**

## 1.4 Product Information

**Tables 1.3** and **1.4** list the M16C/28 Group product information and **Figure 1.3** shows the product numbering system. The specifications are partially different between normal-ver.and T/ V-ver..

**Table 1.3 M16C/28 Product List -Normal-ver.** **As of September, 2006**

| Type Number | ROM Capacity | RAM Capacity | Package Type | Remarks | Product Code |
|---|---|---|---|---|---|
| M30280F6WG (N) | 48 K + 4 K | 4 K | PTLG0085JB-A (85F0G) | Flash Memory | U3, U5, U7, U9 |
| M30280F8WG (N) | 64 K + 4 K | 4 K | | | |
| M30280FAWG (N) | 96 K + 4 K | 8 K | | | |
| M30280F6HP (N) | 48 K + 4 K | 4 K | PLQP0080KB-A (80P6Q-A) | | |
| M30280F8HP (N) | 64 K + 4 K | 4 K | | | |
| M30280FAHP (N) | 96 K + 4 K | 8 K | | | |
| M30280FCHP (N) | 128 K + 4 K | 12 K | | | |
| M30281F6HP (N) | 48 K + 4 K | 4 K | PLQP0064KB-A (64P6Q-A) | | |
| M30281F8HP (N) | 64 K + 4 K | 4 K | | | |
| M30281FAHP (N) | 96 K + 4 K | 8 K | | | |
| M30281FCHP (N) | 128 K + 4 K | 12 K | | | |
| M30280M8-XXXHP (N) | 64 K | 4 K | PLQP0080KB-A (80P6Q-A) | Mask ROM | U3, U5 |
| M30280MA-XXXHP (N) | 96 K | 8 K | | | |
| M30280MC-XXXHP (N) | 128 K | 12 K | | | |
| M30281M8-XXXHP (N) | 64 K | 4 K | PLQP0064KB-A (64P6Q-A) | | |
| M30281MA-XXXHP (N) | 96 K | 8 K | | | |
| M30281MC-XXXHP (N) | 128 K | 12 K | | | |

(N): New

**Table 1.4 M16C/28B Product List -Normal-ver.** **As of September, 2006**

| Type Number | ROM Capacity | RAM Capacity | Package Type | Remarks | Product Code |
|---|---|---|---|---|---|
| M30280FCBHP (D) | 128 K + 4 K | 12 K | PLQP0080KB-A (80P6Q-A) | Flash memory | U7 |
| M30281FCBHP (D) | 128 K + 4 K | 12 K | PLQP0064KB-A (64P6Q-A) | | |

(D): Under development

**Table 1.5 Product Code (Flash Memory-ver.) - M16C/28 Normal-ver., 64-Pin(1)/80-Pin(1)/85-Pin Package**

| Product Code | Package | Internal ROM (User Program Space) | | Internal ROM (Data Space) | | Operating Ambient Temperature |
|---|---|---|---|---|---|---|
| | | Program and Erase Endurance | Temperature Range | Program and Erase Endurance | Temperature Range | |
| U3 | Lead free | 100 | 0 to 60°C | 100 | 0 to 60°C | -40 to 85°C |
| U5 | | | | | | -20 to 85°C |
| U7 | | 1,000 | | 10,000 | -40 to 85°C | -40 to 85°C |
| U9 | | | | | -20 to 85°C | -20 to 85°C |

NOTE:
1. The lead contained products, D3, D5, D7 and D9, are put together with U3, U5, U7 and U9 respectively. Lead-free (Sn-Ag-Cu plating) products can be mounted by both conventional Sn-Pb paste and Lead-free paste.

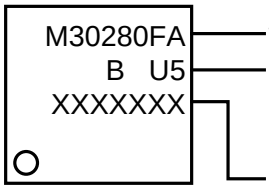
**Table 1.6 Product Code (Flash Memory-ver.) - M16C/28B Normal-ver., 64-Pin/85-Pin Package**

| Product Code | Package | Internal ROM (User Program Space) | | Internal ROM (Data Space) | | Operating Ambient Temperature |
|---|---|---|---|---|---|---|
| | | Program and Erase Endurance | Temperature Range | Program and Erase Endurance | Temperature Range | |
| U7 | Lead-free | 1,000 | 0 to 60°C | 10,000 | -40 to 85°C | -40 to 85°C |

**Table 1.7 Product Code (Mask ROM ver.) - M16C/28B Normal-ver., 64-Pin/80-Pin/85-Pin Package**

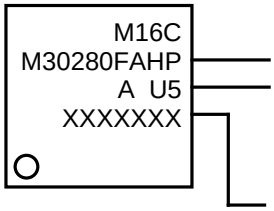
| Product Code | Package | Operating Ambient Temperature |
|---|---|---|
| U3 | Lead-free | -40 to 85°C |
| U5 | | -20 to 85°C |

(1) Flash Memory Version, PTLG0085JB-A (85F0G), Normal-ver.



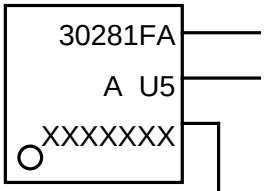

Type No. M30280FAWG
Chip version and product code
B : Chip version.
The first edition is shown to be blank and continues with A, B, and C.
U5 : Product code. (See **Table 1.5**)
Date code seven digits
Manufacturing management code

(2) Flash Memory Version, PLQP0080KB-A (80P6Q-A), Normal-ver.



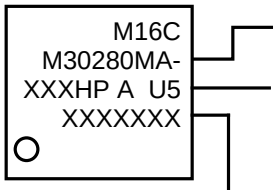

Type No. M30280FAHP
Chip version and product code
A : Chip version and product code(1)
The first edition is shown to be blank and continues with A, B and C.
U5 : Product code. (**Table 1.4**)
Date code seven digits
Manufacturing management code

(3) Flash Memory Version, PLQP0064KB-A (64P6Q-A), Normal-ver.



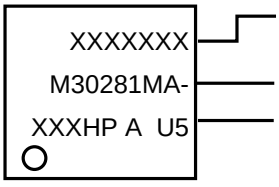

Type No. M30281FAHP
Chip version and product code
A : Chip version and product code(1)
The first edition is shown to be blank and continues with A, B and C.
U5 : Product code. (**Table 1.4**)
Date code seven digits
Manufacturing management code

(4) Mask ROM Version, PLQP0080KB-A (80P6Q-A), Normal-ver.




Type No. M30280MAHP
Chip version and product code
XXX : ROM No.
A : Chip version and product code(1)
The first edition is shown to be blank and continues with A, B and C.
U5 : Product code. (**Table 1.6**)
Date code seven digits
Manufacturing management code

(5) Mask ROM Version, PLQP0064-KB-A (64P6Q-A), Normal-ver.



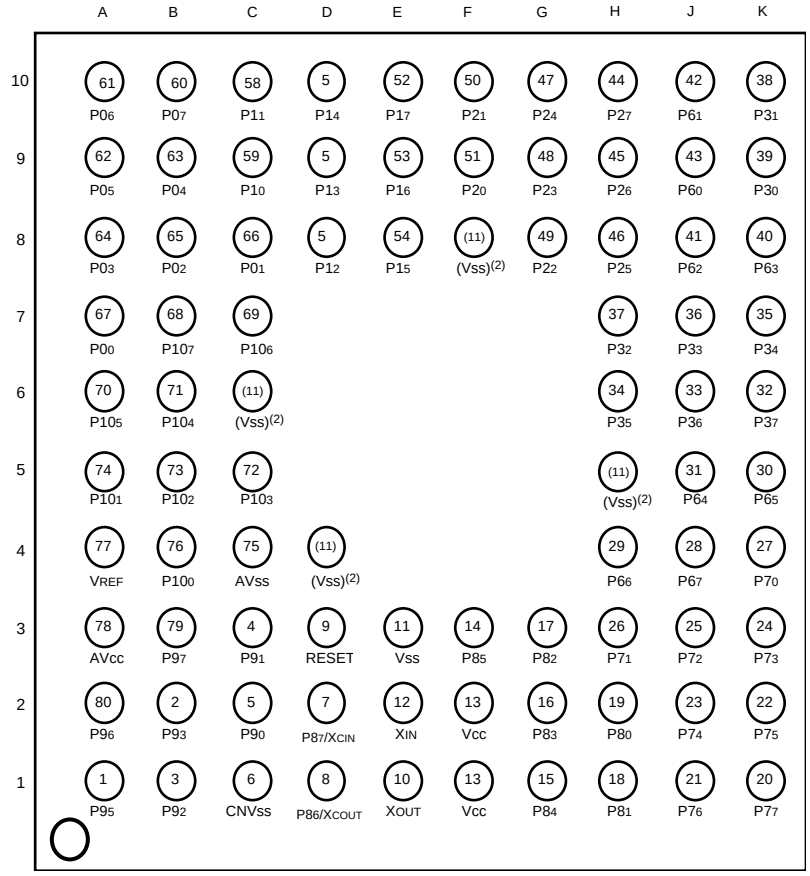

Date code seven digits
Manufacturing management code
Type No. M30281MAHP
Chip version and product code
XXX: ROM No.
A : Chip version and product code(1)
The first edition is shown to be blank and continues with A, B and C.
U5 : Product code. (**Table 1.6**)

NOTES:
1. The following functinos are not available in the first version and version A products.
-Delay trigger mode 0 of A/D conversion
-Delay trigger mode 1 of A/D conversion

**Figure 1.4 Marking Diagram-M16C/28 Normal-ver.**

## 1.5 Pin Assignment

Figures 1.5 to 1.7 show the pin Assignments (top view).



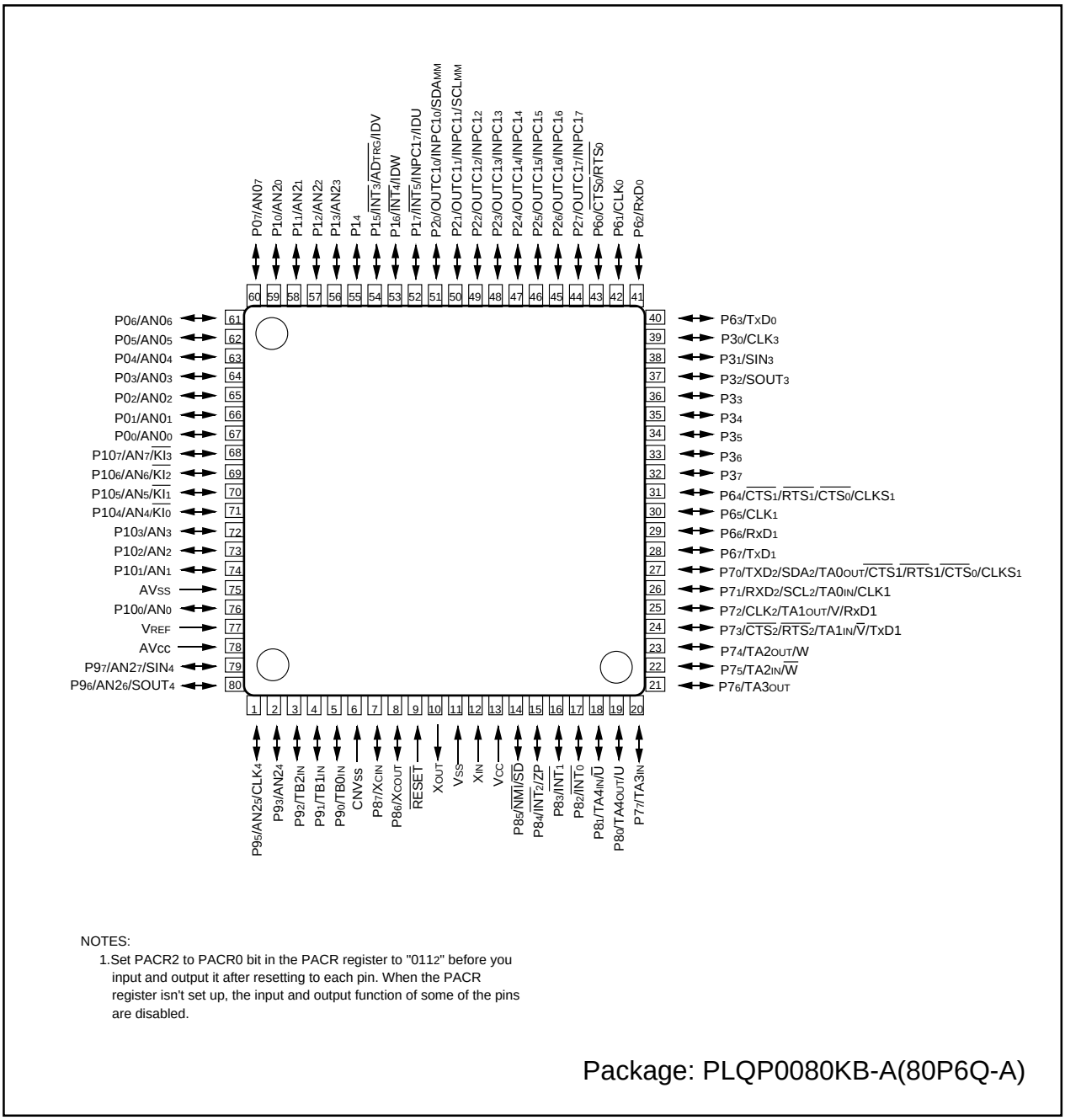

NOTES :
1. The numbers in each grid (circle) show the pin numbers of the M30280FAHP (80P6Q-A package)
2. Connect grids written as (Vss) to Vss(GND) or leave them open.
3. Set PACR2 to PACR0 bits in the PACR register to "0112" before you input and output it after resetting to each pin. When the PACR register is not set, the input and output function of some pins are disabled.

Package: PTLG0085JB-A(85F0G)

**Figure 1.5 Pin Assignment (Top View) of 85-pin Package**

**Table 1.8 Pin Characteristics for 85-pin Package**

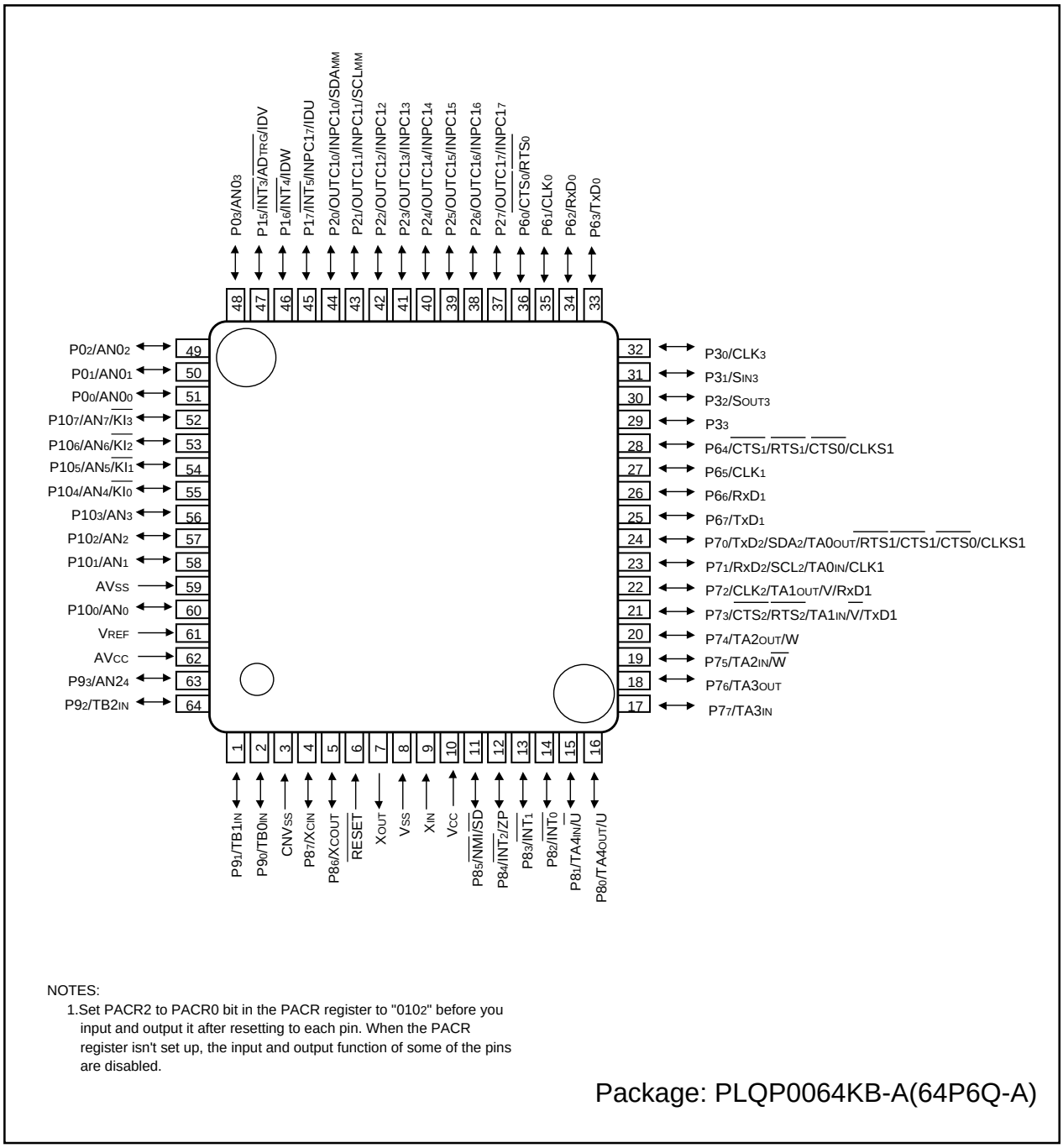
| Pin No. | Control Pin | Port | Interrupt Pin | Timer Pin | Timer S Pin | UART Pin | Multi-master $I^2C$ bus Pin | Analog Pin | PLQP0080KB-A Pin Number |
|---|---|---|---|---|---|---|---|---|---|
| A1 | | P9$_5$ | | | | CLK$_4$ | | AN2$_5$ | 1 |
| A2 | | P9$_6$ | | | | SOUT$_4$ | | AN2$_6$ | 80 |
| A3 | AVcc | | | | | | | | 78 |
| A4 | VREF | | | | | | | | 77 |
| A5 | | P10$_1$ | | | | | | AN$_1$ | 74 |
| A6 | | P10$_5$ | $\overline{KI}_1$ | | | | | AN$_5$ | 70 |
| A7 | | P0$_0$ | | | | | | AN0$_0$ | 67 |
| A8 | | P0$_3$ | | | | | | AN0$_3$ | 64 |
| A9 | | P0$_5$ | | | | | | AN0$_5$ | 62 |
| A10 | | P0$_6$ | | | | | | AN0$_6$ | 61 |
| B1 | | P9$_2$ | | TB2IN | | | | | 3 |
| B2 | | P9$_3$ | | | | | | AN2$_4$ | 2 |
| B3 | | P9$_7$ | | | | SIN$_4$ | | AN2$_7$ | 79 |
| B4 | | P10$_0$ | | | | | | AN$_0$ | 76 |
| B5 | | P10$_2$ | | | | | | AN$_2$ | 73 |
| B6 | | P10$_4$ | $\overline{KI}_0$ | | | | | AN$_4$ | 71 |
| B7 | | P10$_7$ | $\overline{KI}_3$ | | | | | AN$_7$ | 68 |
| B8 | | P0$_2$ | | | | | | AN0$_2$ | 65 |
| B9 | | P0$_4$ | | | | | | AN0$_4$ | 63 |
| B10 | | P0$_7$ | | | | | | AN0$_7$ | 60 |
| C1 | CNVss | | | | | | | | 6 |
| C2 | | P9$_0$ | | TB0IN | | | | | 5 |
| C3 | | P9$_1$ | | TB1IN | | | | | 4 |
| C4 | AVss | | | | | | | | 75 |
| C5 | | P10$_3$ | | | | | | AN$_3$ | 72 |
| C6 | Vss(1) | | | | | | | | (11) |
| C7 | | P10$_6$ | $\overline{KI}_2$ | | | | | AN$_6$ | 69 |
| C8 | | P0$_1$ | | | | | | AN0$_1$ | 66 |
| C9 | | P1$_0$ | | | | | | AN2$_0$ | 59 |
| C10 | | P1$_1$ | | | | | | AN2$_1$ | 58 |
| D1 | XCOUT | P8$_6$ | | | | | | | 8 |
| D2 | XCIN | P8$_7$ | | | | | | | 7 |
| D3 | $\overline{RESET}$ | | | | | | | | 9 |
| D4 | Vss(1) | | | | | | | | (11) |
| D8 | | P1$_2$ | | | | | | AN2$_2$ | 57 |
| D9 | | P1$_3$ | | | | | | AN2$_3$ | 56 |
| D10 | | P1$_4$ | | | | | | | 55 |
| E1 | XOUT | | | | | | | | 10 |
| E2 | XIN | | | | | | | | 12 |
| E3 | Vss | | | | | | | | 11 |




NOTES:
1.Set PACR2 to PACR0 bit in the PACR register to "011₂" before you input and output it after resetting to each pin. When the PACR register isn't set up, the input and output function of some of the pins are disabled.

Package: PLQP0080KB-A(80P6Q-A)

**Figure 1.5 Pin Assignment (Top View) of 80-Pin Package**




NOTES:
1. Set PACR2 to PACR0 bit in the PACR register to "010₂" before you input and output it after resetting to each pin. When the PACR register isn't set up, the input and output function of some of the pins are disabled.

Package: PLQP0064KB-A(64P6Q-A)

**Figure 1.6 Pin Assignment (Top View) of 64-Pin Package**

**Table 10 Pin Characteristics for 64-Pin Package (Continued)**

| Pin No. | Control Pin | Port | Interrupt Pin | Timer Pin | Timer S Pin | UART Pin | Multi-master $I^2C$ bus Pin | Analog Pin |
|---|---|---|---|---|---|---|---|---|
| 41 | | $P2_3$ | | | $OUTC1_3$ / $INPC1_3$ | | | |
| 42 | | $P2_2$ | | | $OUTC1_2$ / $INPC1_2$ | | | |
| 43 | | $P2_1$ | | | $OUTC1_1$ / $INPC1_1$ | | $SCL_{MM}$ | |
| 44 | | $P2_0$ | | | $OUTC1_0$ / $INPC1_0$ | | $SDA_{MM}$ | |
| 45 | | $P1_7$ | $\overline{INT}_5$ | IDU | $INPC1_7$ | | | |
| 46 | | $P1_6$ | $\overline{INT}_4$ | IDW | | | | |
| 47 | | $P1_5$ | $\overline{INT}_3$ | IDV | | | | $\overline{AD_{TRG}}$ |
| 48 | | $P0_3$ | | | | | | $AN0_3$ |
| 49 | | $P0_2$ | | | | | | $AN0_2$ |
| 50 | | $P0_1$ | | | | | | $AN0_1$ |
| 51 | | $P0_0$ | | | | | | $AN0_0$ |
| 52 | | $P10_7$ | $\overline{KI}_3$ | | | | | $AN_7$ |
| 53 | | $P10_6$ | $\overline{KI}_2$ | | | | | $AN_6$ |
| 54 | | $P10_5$ | $\overline{KI}_1$ | | | | | $AN_5$ |
| 55 | | $P10_4$ | $\overline{KI}_0$ | | | | | $AN_4$ |
| 56 | | $P10_3$ | | | | | | $AN_3$ |
| 57 | | $P10_2$ | | | | | | $AN_2$ |
| 58 | | $P10_1$ | | | | | | $AN_1$ |
| 59 | AVss | | | | | | | |
| 60 | | $P10_0$ | | | | | | $AN_0$ |
| 61 | $V_{REF}$ | | | | | | | |
| 62 | AVcc | | | | | | | |
| 63 | | $P9_3$ | | | | | | $AN2_4$ |
| 64 | | $P9_2$ | | $TB_{2IN}$ | | | | |

**Table 1.10 Pin Description (80-Pin and 85-Pin Packages only) (Continued)**

| Classification | Symbol | I/O Type | Function |
|---|---|---|---|
| Serial I/O | CLK4 | I/O | Inputs and outputs the transfer clock |
| | SIN4 | I | Inputs serial data |
| | SOUT4 | O | Outputs serial data |
| A/D Converter | AN04 to AN07<br>AN20 to AN23<br>AN25 to AN27 | I | Analog input pins for the A/D converter |
| I/O Ports | P04 to P07<br>P10 to P14<br>P34 to P37 | I/O | I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 4-bit units |
| | P95 to P97 | I/O | I/O ports having equivalent functions to P0 |

I : Input O : Output I/O : Input and output

# 2. Central Processing Unit (CPU)

**Figure 2.1** shows the CPU registers. The register bank is comprised of 7 registers (R0, R1, R2, R3, A0, A1 and FB) out of 13 CPU registers. Two sets of register banks are provided.

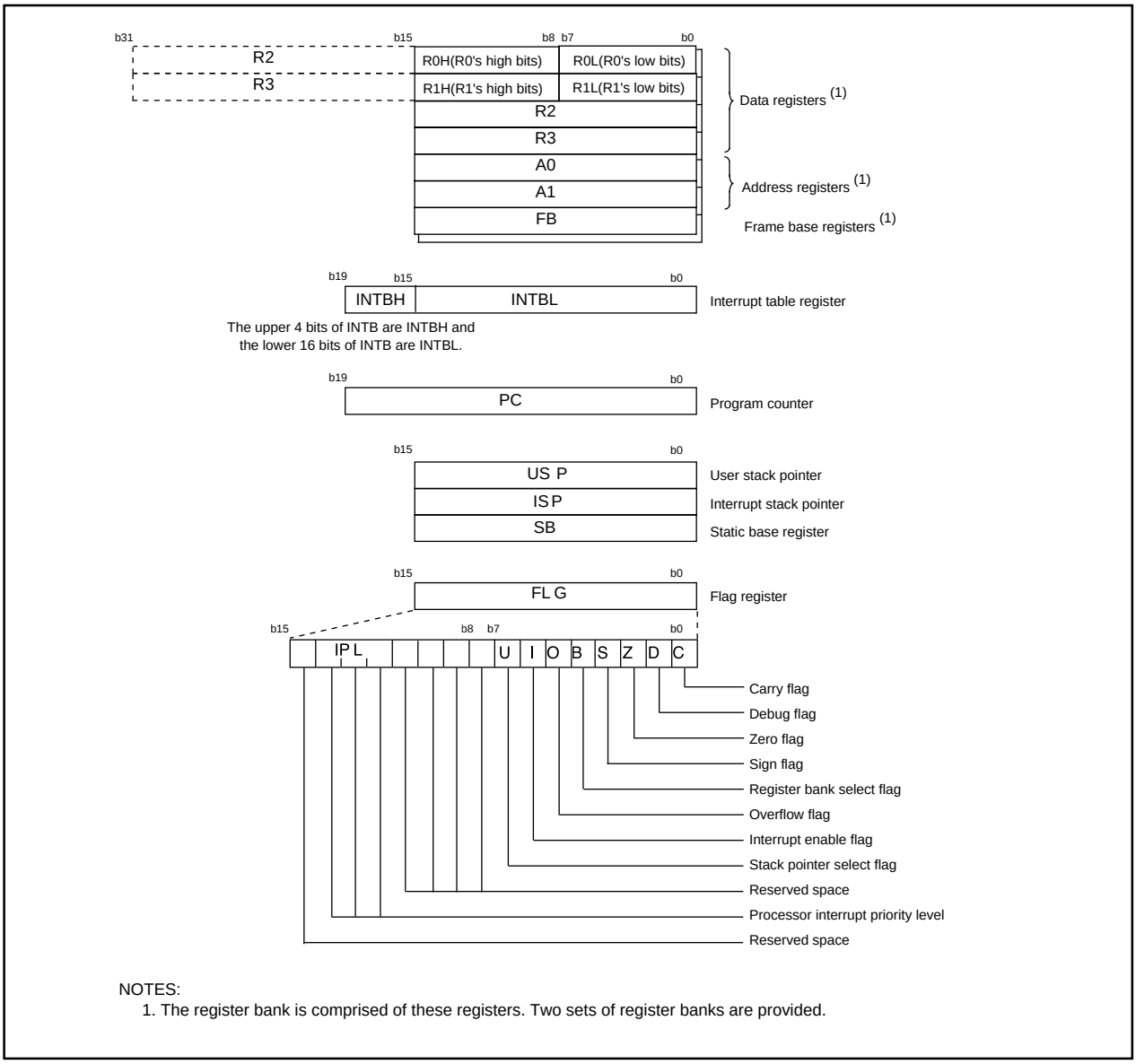



**Figure 2.1 Central Processing Unit Register**

## 2.1 Data Registers (R0, R1, R2 and R3)

The R0, R1, R2 and R3 registers are 16 bit registers for transfer and arithmetic/logic operations.

The R0 and R1 registers can be split into high-order bits(R0H, R1H) and low-order bits (R0L, R1L) to be used seperately as 8-bit data registers. Conversely, R2 and R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R1 and R2.

## 2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and arithmetic/logic operations. A1 is the same as A0. In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

## 2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

### 2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

### 2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to 0.

### 2.8.3 Zero Flag (Z Flag)

This flag is set to 1 when an arithmetic operation resulted in 0; otherwise, it is 0.

### 2.8.4 Sign Flag (S Flag)

This flag is set to 1 when an arithmetic operation resulted in a negative value; otherwise, it is 0.

### 2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is 0 ; register bank 1 is selected when this flag is 1.

### 2.8.6 Overflow Flag (O Flag)

This flag is set to 1 when the operation resulted in an overflow; otherwise, it is 0.

### 2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1. The I flag is cleared to 0 when the interrupt request is accepted.

### 2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is 0; USP is selected when the U flag is 1.

The U flag is cleared to 0 when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

### 2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

### 2.8.10 Reserved Area

When write to this bit, write 0. When read, its content is indeterminate.

# 3. Memory

**Figure 3.1** is a memory map of the M16C/28 Group (M16C/28, M16C/28B). M16C/28 Group provides 1-Mbyte address space from addresses 00000$_{16}$ to FFFFF$_{16}$. The internal ROM is allocated lower addresses beginning with address FFFFF$_{16}$. For example, 64 Kbytes internal ROM is allocated addresses F0000$_{16}$ to FFFFF$_{16}$.

Two 2-Kbyte internal ROM areas, block A and block B, are available in the flash memory version. The blocks are allocated addresses F000$_{16}$ to FFFF$_{16}$.

The fixed interrupt vector tables are allocated addresses FFFDC$_{16}$ to FFFFF$_{16}$. It stores the starting address of each interrupt routine. See the section on interrupts for details.

The internal RAM is allocated higher addresses beginning with address 00400$_{16}$. For example, 4-Kbytes internal RAM is allocated addresses 00400$_{16}$ to 013FF$_{16}$. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowledged.

SFR, consisting of control registers for peripheral functions such as I/O port, A/D converter, serial I/O, timers is allocated addresses 00000$_{16}$ to 003FF$_{16}$. All blank spaces within SFR are reserved and cannot be accessed by users.

The special page vector table is allocated to the addresses FFE00$_{16}$ to FFFDB$_{16}$. This vector is used by the JMPS or JSRS instruction. For details, refer to the ***M16C/60 and M16C/20 Series Software Manual***.

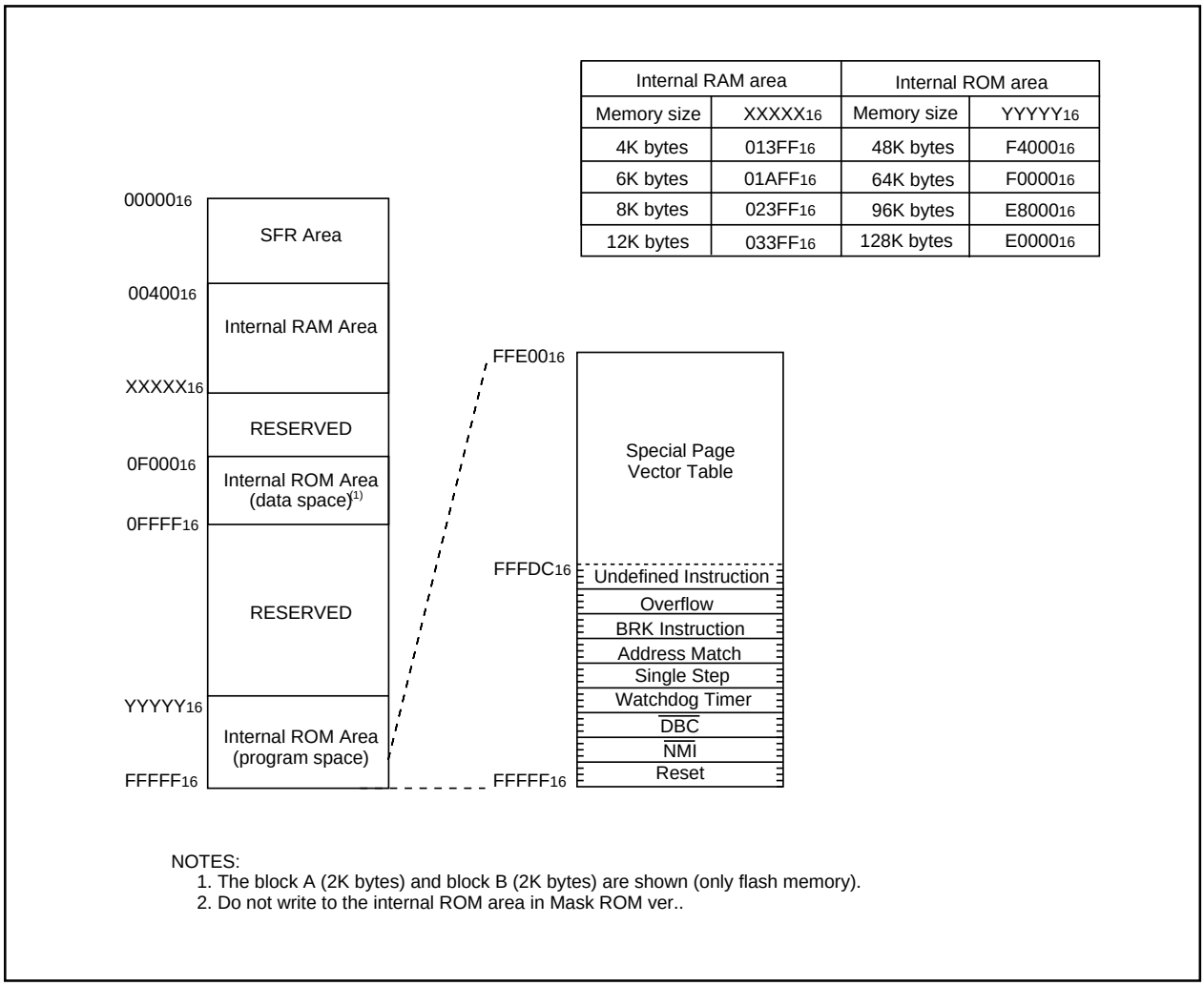



**Figure 3.1 Memory Map**

# 4. Special Function Register (SFR)

SFR (Special Function Register) is the control register of peripheral functions. **Tables 4.1** to **4.7** list the SFR information.

**Table 4.1 SFR Information(1)[1]**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 0000₁₆ | | | |
| 0001₁₆ | | | |
| 0002₁₆ | | | |
| 0003₁₆ | | | |
| 0004₁₆ | Processor mode register 0 | PM0 | 00₁₆ |
| 0005₁₆ | Processor mode register 1 | PM1 | 00001000₂ |
| 0006₁₆ | System clock control register 0 | CM0 | 01001000₂ |
| 0007₁₆ | System clock control register 1 | CM1 | 00100000₂ |
| 0008₁₆ | | | |
| 0009₁₆ | Address match interrupt enable register | AIER | XXXXXX00₂ |
| 000A₁₆ | Protect register | PRCR | XX000000₂ |
| 000B₁₆ | | | |
| 000C₁₆ | Oscillation stop detection register [2] | CM2 | 0X000010₂ |
| 000D₁₆ | | | |
| 000E₁₆ | Watchdog timer start register | WDTS | XX₁₆ |
| 000F₁₆ | Watchdog timer control register | WDC | 00XXXXX₂ |
| 0010₁₆ | Address match interrupt register 0 | RMAD0 | 00₁₆ |
| 0011₁₆ | | | 00₁₆ |
| 0012₁₆ | | | X0₁₆ |
| 0013₁₆ | | | |
| 0014₁₆ | Address match interrupt register 1 | RMAD1 | 00₁₆ |
| 0015₁₆ | | | 00₁₆ |
| 0016₁₆ | | | X0₁₆ |
| 0017₁₆ | | | |
| 0018₁₆ | | | |
| 0019₁₆ | Voltage detection register 1 [3] | VCR1 | 00001000₂ |
| 001A₁₆ | Voltage detection register 2 [3] | VCR2 | 00₁₆ |
| 001B₁₆ | | | |
| 001C₁₆ | PLL control register 0 | PLC0 | 0001X010₂ |
| 001D₁₆ | | | |
| 001E₁₆ | Processor mode register 2 | PM2 | XXX00000₂ |
| 001F₁₆ | Low voltage detection interrupt register | D4INT | 00₁₆ |
| 0020₁₆ | DMA0 source pointer | SAR0 | XX₁₆ |
| 0021₁₆ | | | XX₁₆ |
| 0022₁₆ | | | XX₁₆ |
| 0023₁₆ | | | |
| 0024₁₆ | DMA0 destination pointer | DAR0 | XX₁₆ |
| 0025₁₆ | | | XX₁₆ |
| 0026₁₆ | | | XX₁₆ |
| 0027₁₆ | | | |
| 0028₁₆ | DMA0 transfer counter | TCR0 | XX₁₆ |
| 0029₁₆ | | | XX₁₆ |
| 002A₁₆ | | | |
| 002B₁₆ | | | |
| 002C₁₆ | DMA0 control register | DM0CON | 00000X00₂ |
| 002D₁₆ | | | |
| 002E₁₆ | | | |
| 002F₁₆ | | | |
| 0030₁₆ | DMA1 source pointer | SAR1 | XX₁₆ |
| 0031₁₆ | | | XX₁₆ |
| 0032₁₆ | | | XX₁₆ |
| 0033₁₆ | | | |
| 0034₁₆ | DMA1 destination pointer | DAR1 | XX₁₆ |
| 0035₁₆ | | | XX₁₆ |
| 0036₁₆ | | | XX₁₆ |
| 0037₁₆ | | | |
| 0038₁₆ | DMA1 transfer counter | TCR1 | XX₁₆ |
| 0039₁₆ | | | XX₁₆ |
| 003A₁₆ | | | |
| 003B₁₆ | | | |
| 003C₁₆ | DMA1 control register | DM1CON | 00000X00₂ |
| 003D₁₆ | | | |
| 003E₁₆ | | | |
| 003F₁₆ | | | |

NOTES:
1. The blank spaces are reserved. No access is allowed.
2. The CM20, CM21, and CM27 bits do not change at oscillation stop detection reset.
3. This register does not change at software reset, watchdog timer reset and oscillation stop detection reset.

X : Undefined

**Table 4.4 SFR Information(4)(1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 0300₁₆ | TM, WG register 0 | G1TM0, G1PO0 | XX₁₆ |
| 0301₁₆ | | | XX₁₆ |
| 0302₁₆ | TM, WG register 1 | G1TM1, G1PO1 | XX₁₆ |
| 0303₁₆ | | | XX₁₆ |
| 0304₁₆ | TM, WG register 2 | G1TM2, G1PO2 | XX₁₆ |
| 0305₁₆ | | | XX₁₆ |
| 0306₁₆ | TM, WG register 3 | G1TM3, G1PO3 | XX₁₆ |
| 0307₁₆ | | | XX₁₆ |
| 0308₁₆ | TM, WG register 4 | G1TM4, G1PO4 | XX₁₆ |
| 0309₁₆ | | | XX₁₆ |
| 030A₁₆ | TM, WG register 5 | G1TM5, G1PO5 | XX₁₆ |
| 030B₁₆ | | | XX₁₆ |
| 030C₁₆ | TM, WG register 6 | G1TM6, G1PO6 | XX₁₆ |
| 030D₁₆ | | | XX₁₆ |
| 030E₁₆ | TM, WG register 7 | G1TM7, G1PO7 | XX₁₆ |
| 030F₁₆ | | | XX₁₆ |
| 0310₁₆ | WG control register 0 | G1POCR0 | 0X00XX00₂ |
| 0311₁₆ | WG control register 1 | G1POCR1 | 0X00XX00₂ |
| 0312₁₆ | WG control register 2 | G1POCR2 | 0X00XX00₂ |
| 0313₁₆ | WG control register 3 | G1POCR3 | 0X00XX00₂ |
| 0314₁₆ | WG control register 4 | G1POCR4 | 0X00XX00₂ |
| 0315₁₆ | WG control register 5 | G1POCR5 | 0X00XX00₂ |
| 0316₁₆ | WG control register 6 | G1POCR6 | 0X00XX00₂ |
| 0317₁₆ | WG control register 7 | G1POCR7 | 0X00XX00₂ |
| 0318₁₆ | TM control register 0 | G1TMCR0 | 00₁₆ |
| 0319₁₆ | TM control register 1 | G1TMCR1 | 00₁₆ |
| 031A₁₆ | TM control register 2 | G1TMCR2 | 00₁₆ |
| 031B₁₆ | TM control register 3 | G1TMCR3 | 00₁₆ |
| 031C₁₆ | TM control register 4 | G1TMCR4 | 00₁₆ |
| 031D₁₆ | TM control register 5 | G1TMCR5 | 00₁₆ |
| 031E₁₆ | TM control register 6 | G1TMCR6 | 00₁₆ |
| 031F₁₆ | TM control register 7 | G1TMCR7 | 00₁₆ |
| 0320₁₆ | Base timer register | G1BT | XX₁₆ |
| 0321₁₆ | | | XX₁₆ |
| 0322₁₆ | Base timer control register 0 | G1BCR0 | 00₁₆ |
| 0323₁₆ | Base timer control register 1 | G1BCR1 | 00₁₆ |
| 0324₁₆ | TM prescale register 6 | G1TPR6 | 00₁₆ |
| 0325₁₆ | TM prescale register 7 | G1TPR7 | 00₁₆ |
| 0326₁₆ | Function enable register | G1FE | 00₁₆ |
| 0327₁₆ | Function select register | G1FS | 00₁₆ |
| 0328₁₆ | Base timer reset register | G1BTRR | XX₁₆ |
| 0329₁₆ | | | XX₁₆ |
| 032A₁₆ | Divider register | G1DV | 00₁₆ |
| 032B₁₆ | | | |
| 032C₁₆ | | | |
| 032D₁₆ | | | |
| 032E₁₆ | | | |
| 032F₁₆ | | | |
| 0330₁₆ | Interrupt request register | G1IR | XX₁₆ |
| 0331₁₆ | Interrupt enable register 0 | G1IE0 | 00₁₆ |
| 0332₁₆ | Interrupt enable register 1 | G1IE1 | 00₁₆ |
| 0333₁₆ | | | |
| 0334₁₆ | | | |
| 0335₁₆ | | | |
| 0336₁₆ | | | |
| 0337₁₆ | | | |
| 0338₁₆ | | | |
| 0339₁₆ | | | |
| 033A₁₆ | | | |
| 033B₁₆ | | | |
| 033C₁₆ | | | |
| 033D₁₆ | | | |
| 033E₁₆ | NMI digital debounce register | NDDR | FF₁₆ |
| 033F₁₆ | P17 digital debounce register | P17DDR | FF₁₆ |

Note 1:The blank spaces are reserved. No access is allowed.

X : Undefined

**Table 4.6 SFR Information(6)(1)**

| Address | Register | Symbol | After Reset |
|---|---|---|---|
| 038016 | Count start flag | TABSR | 0016 |
| 038116 | Clock prescaler reset flag | CPSRF | 0XXXXXXX2 |
| 038216 | One-shot start flag | ONSF | 0016 |
| 038316 | Trigger select register | TRGSR | 0016 |
| 038416 | Up-down flag | UDF | 0016 |
| 038516 | | | |
| 038616 | Timer A0 register | TA0 | XX16 |
| 038716 | | | XX16 |
| 038816 | Timer A1 register | TA1 | XX16 |
| 038916 | | | XX16 |
| 038A16 | Timer A2 register | TA2 | XX16 |
| 038B16 | | | XX16 |
| 038C16 | Timer A3 register | TA3 | XX16 |
| 038D16 | | | XX16 |
| 038E16 | Timer A4 register | TA4 | XX16 |
| 038F16 | | | XX16 |
| 039016 | Timer B0 register | TB0 | XX16 |
| 039116 | | | XX16 |
| 039216 | Timer B1 register | TB1 | XX16 |
| 039316 | | | XX16 |
| 039416 | Timer B2 register | TB2 | XX16 |
| 039516 | | | XX16 |
| 039616 | Timer A0 mode register | TA0MR | 0016 |
| 039716 | Timer A1 mode register | TA1MR | 0016 |
| 039816 | Timer A2 mode register | TA2MR | 0016 |
| 039916 | Timer A3 mode register | TA3MR | 0016 |
| 039A16 | Timer A4 mode register | TA4MR | 0016 |
| 039B16 | Timer B0 mode register | TB0MR | 00XX00002 |
| 039C16 | Timer B1 mode register | TB1MR | 00XX00002 |
| 039D16 | Timer B2 mode register | TB2MR | 00XX00002 |
| 039E16 | Timer B2 special mode register | TB2SC | X0000000 2 |
| 039F16 | | | |
| 03A016 | UART0 transmit/receive mode register | U0MR | 0016 |
| 03A116 | UART0 bit rate generator | U0BRG | XX16 |
| 03A216 | UART0 transmit buffer register | U0TB | XX16 |
| 03A316 | | | XX16 |
| 03A416 | UART0 transmit/receive control register 0 | U0C0 | 000010002 |
| 03A516 | UART0 transmit/receive control register 1 | U0C1 | 000000102 |
| 03A616 | UART0 receive buffer register | U0RB | XX16 |
| 03A716 | | | XX16 |
| 03A816 | UART1 transmit/receive mode register | U1MR | 0016 |
| 03A916 | UART1 bit rate generator | U1BRG | XX16 |
| 03AA16 | UART1 transmit buffer register | U1TB | XX16 |
| 03AB16 | | | XX16 |
| 03AC16 | UART1 transmit/receive control register 0 | U1C0 | 000010002 |
| 03AD16 | UART1 transmit/receive control register 1 | U1C1 | 000000102 |
| 03AE16 | UART1 receive buffer register | U1RB | XX16 |
| 03AF16 | | | XX16 |
| 03B016 | UART transmit/receive control register 2 | UCON | X0000000 2 |
| 03B116 | | | |
| 03B216 | | | |
| 03B316 | | | |
| 03B416 | | | |
| 03B516 | | | |
| 03B616 | | | |
| 03B716 | | | |
| 03B816 | DMA0 request cause select register | DM0SL | 0016 |
| 03B916 | | | |
| 03BA16 | DMA1 request cause select register | DM1SL | 0016 |
| 03BB16 | | | |
| 03BC16 | | | |
| 03BD16 | | | |
| 03BE16 | | | |
| 03BF16 | | | |

Note 1:The blank spaces are reserved. No access is allowed.

X : Undefined

| REVISION HISTORY | M16C/28 Group (M16C/28, M16C/28B) Shortsheet |
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