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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, IEBus, SIO, UART/USART
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	71
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	85-TFLGA
Supplier Device Package	85-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30280f8wg-u5b

RENESAS

M16C/28 Group (M16C/28, M16C/28B)
SINGLE-CHIP 16-BIT CMOS MCU

REJ03B0201-0050
Rev.0.50
2006.09.15

1. Overview

The M16C/28 Group (M16C/28 and M16C/28B) MCU are single-chip control MCU, fabricated using high-performance silicon gate CMOS technology with the M16C/60 series CPU core. The M16C/28 Group (M16C/28 and M16C/28B) are housed in 64-pin and 80-pin plastic molded LQFP packages and also in 85-pin plastic molded TFLGA (Thin Fine Pitch Land Grid Array) package. With a 1-Mbyte address space, this MCU combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed. It includes a multiplier and DMAC adequate for office automation, communication devices and other high-speed processing applications.

The M16C/28 has Normal-ver., T-ver., and V-ver.. The M16C/28B has Normal-ver. only.

This hardware manual describes the Normal-ver. only. Please contact Renesas Technology Corp. for T-ver./V-ver. information.

1.1 Applications

Audio, cameras, office equipment, communication equipment, portable equipment, home appliances (inverter solution), motor control, industrial equipment, etc.

Table 1.2   M16C/28 Group (M16C/28, M16C/28) (64-Pin Package)

	Item	Performance
CPU	Number of basic instructions	91 instructions
	Minimum instruction excution time	41.7 ns (f(BCLK) = 24 MHZ, VCC = 4.2 V to 5.5 V) (M16C/28B) 50 ns (f(BCLK) = 20 MHZ, VCC = 3.0V to 5.5V) (M16C/28, M16C/28B) 100 ns (f(BCLK) = 10 MHZ, VCC = 2.7V to 5.5V) (M16C/28, M16C/28B)
	Operation mode	Single chip mode
	Address space	1M bytes
	Memory capacity	See **Table 1.3**
Peripheral Function	I/O Port	Input/Output : 55 lines
	Multifunction timer	TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase Motor Control Timer TimerS (Input Capture/Output Compare) : 16bit base timer x 1 channel (Input/Output x 8 channels)

	Serial I/O	2 channels (UART0, UART1)
		    UART, clock synchronous
		 1 channel (UART2)
		    UART, clock synchronous, I^2C bus[1], or IEbus[2]
		 1 channels (SI/O3, SI/O4)
		    Clock synchronous
		 1 channel (Multi-Master I^2C bus[1])

	A/D converter	10 bits x 13 channels
	DMAC	2 channels
	Watchdog timer	15 bits x 1 (with prescaler)
	Interrupt	24 internal and 8 external sources, 4 software sources, 7 levels
	Clock generation circuit	4 circuits • Main clock(*) • Sub-clock(*) • On-chip oscillator • PLL frequency synthesizer (*) Equipped with a built-in feedback resistor
	Oscillation Stop Detect Function	Main clock oscillation stop, re-oscillation detect function
	Voltage detection circuit	Available
Electrical Characteristics	Power supply voltage	VCC = 4.2 V to 5.5 V (f(BCLK) = 24 MHz) (M16C/28) VCC = 3.0 V to 5.5 V (f(BCLK) = 20 MHz) (M16C/28, M16C/28B) VCC = 2.7 V to 5.5 V (f(BCLK) = 10 MHz) (M16C/28, M16C/28B)
	Power consumption	16 mA (VCC = 5 V, f(BCLK) = 20 MHz) 25 μA (f(XCIN) = 32 KHz on RAM) 3.0 μA (VCC = 3 V, f(XCIN) = 32 KHz, in wait mode) 0.7 μA (VCC = 3 V, in stop mode)
Flash Memory	Program/erase supply voltage	2.7 V to 5.5 V
	Program and erase endurance	100 times (all space) or 1,000 times (Blocks 0 to 5) /10,000 times (Block A, Block B[3])
Operating Ambient Temperature		-20 to 85C°/-40 to 85C°[3]
Package		64-pin plastic mold LQFP

NOTES:
  1. I^2C bus is a trademark of Koninklijke Philips Electronics N. V.
  2. IEBus is a trademark of NEC Electronics Corporation.
  3. Refer to **Table 1.5** to **1.7** for number of program/erase.
  4. Use PLL frequency synthesizer to use M16C/28B at f(BCLK) = 24 MHz.
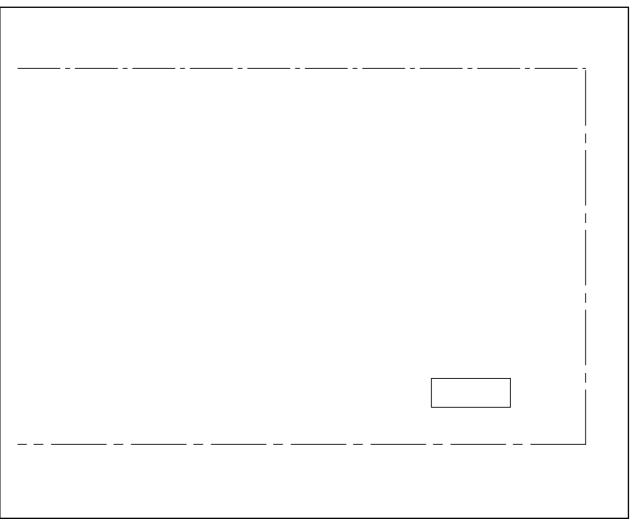
Figure 1.2 M16C/28 Group (M16C/28, M16C/28B), 64-Pin Block Diagram

1.4 Product Information

Tables 1.3 and **1.4** list the M16C/28 Group product information and **Figure 1.3** shows the product numbering system. The specifications are partially different between normal-ver.and T/ V-ver..

Table 1.3 M16C/28 Product List -Normal-ver.   **As of September, 2006**

Type Number		ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30280F6WG	(N)	48 K + 4 K	4 K	PTLG0085JB-A (85F0G)	Flash Memory	U3, U5, U7, U9
M30280F8WG	(N)	64 K + 4 K	4 K			
M30280FAWG	(N)	96 K + 4 K	8 K			
M30280F6HP	(N)	48 K + 4 K	4 K	PLQP0080KB-A (80P6Q-A)		
M30280F8HP	(N)	64 K + 4 K	4 K			
M30280FAHP	(N)	96 K + 4 K	8 K			
M30280FCHP	(N)	128 K + 4 K	12 K			
M30281F6HP	(N)	48 K + 4 K	4 K	PLQP0064KB-A (64P6Q-A)		
M30281F8HP	(N)	64 K + 4 K	4 K			
M30281FAHP	(N)	96 K + 4 K	8 K			
M30281FCHP	(N)	128 K + 4 K	12 K			
M30280M8-XXXHP	(N)	64 K	4 K	PLQP0080KB-A (80P6Q-A)	Mask ROM	U3, U5
M30280MA-XXXHP	(N)	96 K	8 K			
M30280MC-XXXHP	(N)	128 K	12 K			
M30281M8-XXXHP	(N)	64 K	4 K	PLQP0064KB-A (64P6Q-A)		
M30281MA-XXXHP	(N)	96 K	8 K			
M30281MC-XXXHP	(N)	128 K	12 K			

(N): New

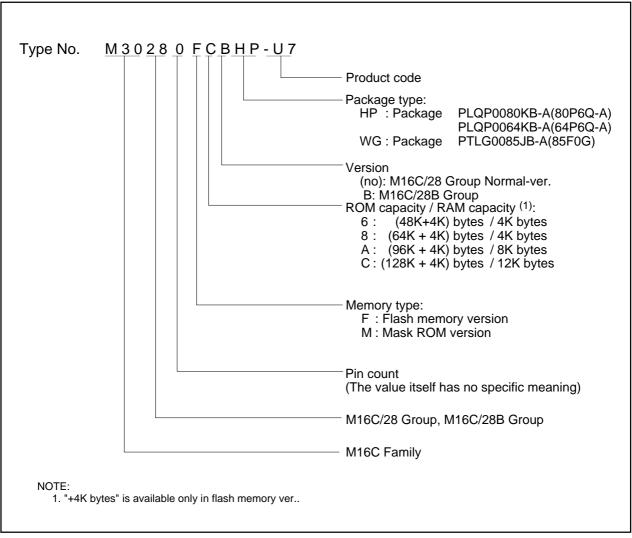**Table 1.4 M16C/28B Product List -Normal-ver.**   **As of September, 2006**

Type Number		ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30280FCBHP	(D)	128 K + 4 K	12 K	PLQP0080KB-A (80P6Q-A)	Flash memory	U7
M30281FCBHP	(D)	128 K + 4 K	12 K	PLQP0064KB-A (64P6Q-A)		

(D): Under development

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Type No.　M 3 0 2 8 0 F C B H P - U 7

　　　　　　　　　　　　　　　　　　　Product code

　　　　　　　　　　　　　　　　Package type:
　　　　　　　　　　　　　　　　　HP : Package　PLQP0080KB-A(80P6Q-A)
　　　　　　　　　　　　　　　　　　　　　　　　PLQP0064KB-A(64P6Q-A)
　　　　　　　　　　　　　　　　　WG : Package　PTLG0085JB-A(85F0G)

　　　　　　　　　　　　　　　Version
　　　　　　　　　　　　　　　　(no): M16C/28 Group Normal-ver.
　　　　　　　　　　　　　　　　B: M16C/28B Group
　　　　　　　　　　　　　　ROM capacity / RAM capacity [1]:
　　　　　　　　　　　　　　　6 :　 (48K+4K) bytes　/ 4K bytes
　　　　　　　　　　　　　　　8 :　 (64K + 4K) bytes　/ 4K bytes
　　　　　　　　　　　　　　　A :　 (96K + 4K) bytes　/ 8K bytes
　　　　　　　　　　　　　　　C : (128K + 4K) bytes　/ 12K bytes

　　　　　　　　　　　　Memory type:
　　　　　　　　　　　　　F : Flash memory version
　　　　　　　　　　　　　M : Mask ROM version

　　　　　　　　　Pin count
　　　　　　　　　(The value itself has no specific meaning)

　　　　　　M16C/28 Group, M16C/28B Group

　　　M16C Family

NOTE:
　　1. "+4K bytes" is available only in flash memory ver..

Figure 1.3 Product Numbering System

Table 1.5 Product Code (Flash Memory-ver.) - M16C/28 Normal-ver., 64-Pin[(1)]/80-Pin[(1)]/85-Pin Package

Product Code	Package	Internal ROM (User Program Space)		Internal ROM (Data Space)		Operating Ambient Temperature
		Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
U3	Lead free	100	0 to 60℃	100	0 to 60℃	-40 to 85℃
U5						-20 to 85℃
U7		1,000		10,000	-40 to 85℃	-40 to 85℃
U9					-20 to 85℃	-20 to 85℃

NOTE:
  1. The lead contained products, D3, D5, D7 and D9, are put together with U3, U5, U7 and U9 respectively. Lead-free (Sn-Ag-Cu plating) products can be mounted by both conventional Sn-Pb paste and Lead-free paste.

Table 1.6 Product Code (Flash Memory-ver.) - M16C/28B Normal-ver., 64-Pin/85-Pin Package

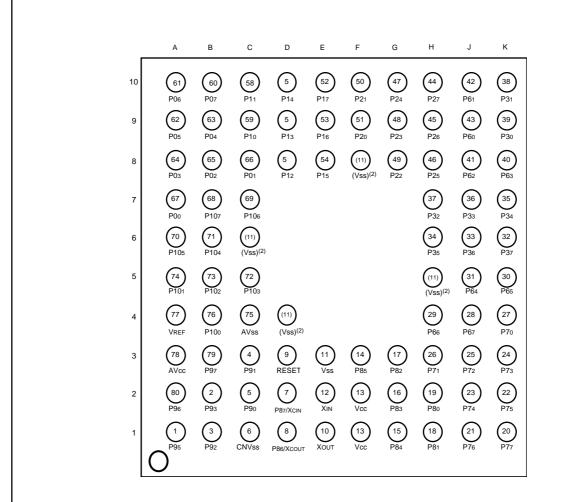| Product Code	Package	Internal ROM (User Program Space)		Internal ROM (Data Space)		Operating Ambient Temperature
		Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
U7	Lead-free	1,000	0 to 60℃	10,000	-40 to 85℃	-40 to 85℃

Table 1.7 Product Code (Mask ROM ver.) - M16C/28B Normal-ver., 64-Pin/80-Pin/85-Pin Package

Product Code	Package	Operating Ambient Temperature
U3	Lead-free	-40 to 85℃
U5		-20 to 85℃

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1.5 Pin Assignment

Figures 1.5 to 1.7 show the pin Assignments (top view).

NOTES :
1. The numbers in each grid (circle) show the pin numbers of the M30280FAHP (80P6Q-A package)
2. Connect grids written as (Vss) to Vss(GND) or leave them open.
3. Set PACR2 to PACR0 bits in the PACR register to "0112" before you input and output it after resetting to each pin. When the PACR register is not set, the input and output function of some pins are disabled.

Package: PTLG0085JB-A(85F0G)

Figure 1.5 Pin Assignment (Top View) of 85-pin Package

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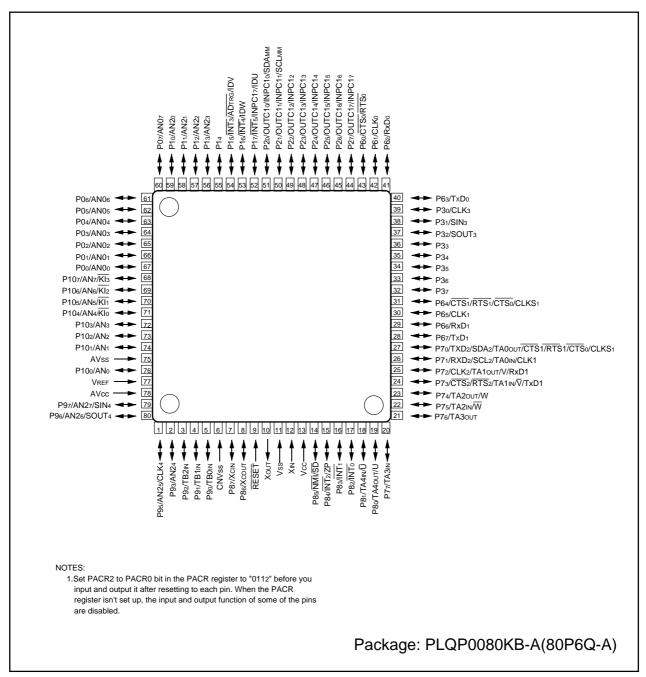
Figure 1.5 Pin Assignment (Top View) of 80-Pin Package

Table 1.9 Pin Characteristics for 80-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I^{2}C bus Pin	Analog Pin
1		P9$_5$				CLK$_4$		AN2$_5$
2		P9$_3$						AN2$_4$
3		P9$_2$		TB2$_{IN}$				
4		P9$_1$		TB1$_{IN}$				
5		P9$_0$		TB0$_{IN}$				
6	CNVss							
7	X$_{CIN}$	P8$_7$						
8	X$_{COUT}$	P8$_6$						
9	$\overline{RESET}$							
10	X$_{OUT}$							
11	Vss							
12	X$_{IN}$							
13	Vcc							
14		P8$_5$	$\overline{NMI}$	$\overline{SD}$				
15		P8$_4$	$\overline{INT_2}$	ZP				
16		P8$_3$	$\overline{INT_1}$					
17		P8$_2$	$\overline{INT_0}$					
18		P8$_1$		TA4$_{IN}$ / $\overline{U}$				
19		P8$_0$		TA4$_{OUT}$ / U				
20		P7$_7$		TA3$_{IN}$				
21		P7$_6$		TA3$_{OUT}$				
22		P7$_5$		TA2$_{IN}$ / $\overline{W}$				
23		P7$_4$		TA2$_{OUT}$ / W				
24		P7$_3$		TA1$_{IN}$ / $\overline{V}$		$\overline{CTS_2}$ / $\overline{RTS_2}$ / TxD$_1$		
25		P7$_2$		TA1$_{OUT}$ / V		CLK$_2$ / RxD$_1$		
26		P7$_1$		TA0$_{IN}$		RxD$_2$ / SCL$_2$ / CLK$_1$		
27		P7$_0$		TA0$_{OUT}$		TxD$_2$ / SDA$_2$ / $\overline{RTS_1}$ / $\overline{CTS_1}$ / $\overline{CTS_0}$ / CLKS$_1$		
28		P6$_7$				TxD$_1$		
29		P6$_6$				RxD$_1$		
30		P6$_5$				CLK$_1$		
31		P6$_4$				$\overline{RTS_1}$ / $\overline{CTS_1}$/ $\overline{CTS_0}$ / CLKS$_1$		
32		P3$_7$						
33		P3$_6$						
34		P3$_5$						
35		P3$_4$						
36		P3$_3$						
37		P3$_2$				S$_{OUT3}$		
38		P3$_1$				S$_{IN3}$		
39		P3$_0$				CLK$_3$		
40		P6$_3$				TxD$_0$		

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Table 10　Pin Characteristics for 64-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I^{2}C bus Pin	Analog Pin
41		P2_3			OUTC1_3 / INPC1_3			
42		P2_2			OUTC1_2 / INPC1_2			
43		P2_1			OUTC1_1 / INPC1_1		SCL$_{MM}$	
44		P2_0			OUTC1_0 / INPC1_0		SDA$_{MM}$	
45		P1_7	$\overline{INT_5}$	IDU	INPC1_7			
46		P1_6	$\overline{INT_4}$	IDW				
47		P1_5	$\overline{INT_3}$	IDV				$\overline{AD_{TRG}}$
48		P0_3						AN0_3
49		P0_2						AN0_2
50		P0_1						AN0_1
51		P0_0						AN0_0
52		P10_7	$\overline{KI_3}$					AN$_7$
53		P10_6	$\overline{KI_2}$					AN$_6$
54		P10_5	$\overline{KI_1}$					AN$_5$
55		P10_4	$\overline{KI_0}$					AN$_4$
56		P10_3						AN$_3$
57		P10_2						AN$_2$
58		P10_1						AN$_1$
59	AV$_{SS}$							
60		P10_0						AN$_0$
61	V$_{REF}$							
62	AV$_{CC}$							
63		P9_3						AN2_4
64		P9_2		TB2_{IN}				

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3. Memory

Figure 3.1 is a memory map of the M16C/28 Group (M16C/28, M16C/28B). M16C/28 Group provides 1-Mbyte address space from addresses 00000_{16} to $FFFFF_{16}$. The internal ROM is allocated lower addresses beginning with address $FFFFF_{16}$. For example, 64 Kbytes internal ROM is allocated addresses $F0000_{16}$ to $FFFFF_{16}$.

Two 2-Kbyte internal ROM areas, block A and block B, are available in the flash memory version. The blocks are allocated addresses $F000_{16}$ to $FFFF_{16}$.

The fixed interrupt vector tables are allocated addresses $FFFDC_{16}$ to $FFFFF_{16}$. It stores the starting address of each interrupt routine. See the section on interrupts for details.

The internal RAM is allocated higher addresses beginning with address 00400_{16}. For example, 4-Kbytes internal RAM is allocated addresses 00400_{16} to $013FF_{16}$. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowledged.

SFR, consisting of control registers for peripheral functions such as I/O port, A/D converter, serial I/O, timers is allocated addresses 00000_{16} to $003FF_{16}$. All blank spaces within SFR are reserved and cannot be accessed by users.

The special page vector table is allocated to the addresses $FFE00_{16}$ to $FFFDB_{16}$. This vector is used by the JMPS or JSRS instruction. For details, refer to the ***M16C/60 and M16C/20 Series Software Manual***.
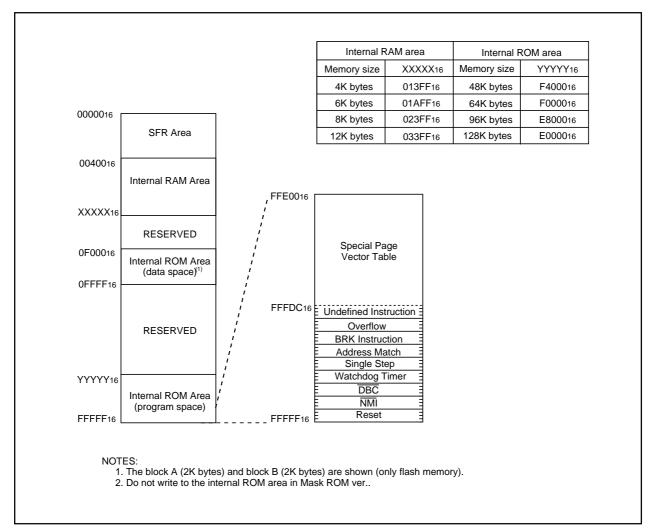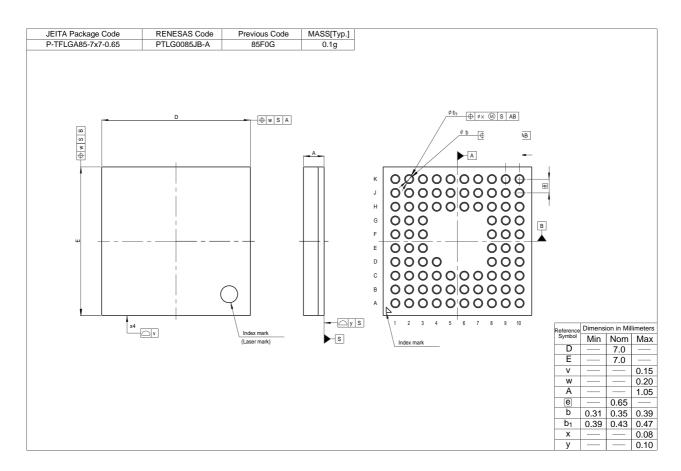
Internal RAM area		Internal ROM area	
Memory size	$XXXXX_{16}$	Memory size	$YYYYY_{16}$
4K bytes	$013FF_{16}$	48K bytes	$F4000_{16}$
6K bytes	$01AFF_{16}$	64K bytes	$F0000_{16}$
8K bytes	$023FF_{16}$	96K bytes	$E8000_{16}$
12K bytes	$033FF_{16}$	128K bytes	$E0000_{16}$

00000_{16} SFR Area
00400_{16} Internal RAM Area
$XXXXX_{16}$ RESERVED
$0F000_{16}$ Internal ROM Area (data space)[1]
$0FFFF_{16}$ RESERVED
$YYYYY_{16}$ Internal ROM Area (program space)
$FFFFF_{16}$

$FFE00_{16}$ Special Page Vector Table
$FFFDC_{16}$ Undefined Instruction
Overflow
BRK Instruction
Address Match
Single Step
Watchdog Timer
$\overline{DBC}$
$\overline{NMI}$
Reset
$FFFFF_{16}$

NOTES:
1. The block A (2K bytes) and block B (2K bytes) are shown (only flash memory).
2. Do not write to the internal ROM area in Mask ROM ver..

Figure 3.1 Memory Map

Table 4.3 SFR Information(3)[1]

Address	Register	Symbol	After Reset
≈			≈
$01B0_{16}$			
$01B1_{16}$			
$01B2_{16}$			
$01B3_{16}$	Flash memory control register 4 [2]	FMR4	01000000_2
$01B4_{16}$			
$01B5_{16}$	Flash memory control register 1 [2]	FMR1	$000XXX0X_2$
$01B6_{16}$			
$01B7_{16}$	Flash memory control register 0 [2]	FMR0	00000001_2
$01B8_{16}$			
$01B9_{16}$			
≈			≈
0210_{16}	Low-power Consumption Control 0	LPCC0	$X0000001_2$
0211_{16}			
0212_{16}			
0213_{16}			
0214_{16}			
0215_{16}			
0216_{16}			
0217_{16}			
0218_{16}			
0219_{16}			
≈			≈
0250_{16}			
0251_{16}			
0252_{16}			
0253_{16}			
0254_{16}			
0255_{16}			
0256_{16}			
0257_{16}			
0258_{16}			
0259_{16}			
$025A_{16}$			
$025B_{16}$			
$025C_{16}$	On-chip oscillator control register	ROCR	$X0000101_2$
$025D_{16}$	Pin assignment control register	PACR	00_{16}
$025E_{16}$	Peripheral clock select register	PCLKR	00000011_2
$025F_{16}$	Low-power Consumption Control 1	LPCC1	00_{16}
≈			≈
$02E0_{16}$	I^{2}C0 data shift register	S00	XX_{16}
$02E1_{16}$			
$02E2_{16}$	I^{2}C0 address register	S0D0	00_{16}
$02E3_{16}$	I^{2}C0 control register 0	S1D0	00_{16}
$02E4_{16}$	I^{2}C0 clock control register	S20	00_{16}
$02E5_{16}$	I^{2}C0 start/stop condition control register	S2D0	00011010_2
$02E6_{16}$	I^{2}C0 control register 1	S3D0	00110000_2
$02E7_{16}$	I^{2}C0 control register 2	S4D0	00_{16}
$02E8_{16}$	I^{2}C0 status register	S10	$0001000X_2$
$02E9_{16}$			
$02EA_{16}$			
≈			≈
$02FE_{16}$			
$02FF_{16}$			

Note 1:The blank spaces are reserved. No access is allowed.
Note 2:This register is included in the flash memory version.

X : Undefined

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA85-7x7-0.65	PTLG0085JB-A	85F0G	0.1g

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.65	—
b	0.31	0.35	0.39
b₁	0.39	0.43	0.47
x	—	—	0.08
y	—	—	0.10

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REVISION HISTORY	M16C/28 Group (M16C/28, M16C/28B) Shortsheet		

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		Page	Summary
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