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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Not For New Designs
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, IEBus, SIO, UART/USART
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	71
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30280fahp-u5b

1. Overview

The M16C/28 Group (M16C/28 and M16C/28B) MCU are single-chip control MCU, fabricated using high-performance silicon gate CMOS technology with the M16C/60 series CPU core. The M16C/28 Group (M16C/28 and M16C/28B) are housed in 64-pin and 80-pin plastic molded LQFP packages and also in 85-pin plastic molded TFLGA (Thin Fine Pitch Land Grid Array) package. With a 1-Mbyte address space, this MCU combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed. It includes a multiplier and DMAC adequate for office automation, communication devices and other high-speed processing applications.

The M16C/28 has Normal-ver., T-ver., and V-ver.. The M16C/28B has Normal-ver. only.

This hardware manual describes the Normal-ver. only. Please contact Renesas Technology Corp. for T-ver./V-ver. information.

1.1 Applications

Audio, cameras, office equipment, communication equipment, portable equipment, home appliances (inverter solution), motor control, industrial equipment, etc.

1.3 Block Diagram

Figure 1.1 is a block diagram of the M16C/28 Group (M16C/28, M16C/28B), 80-pin and 85-pin package.

Figure 1.2 is a block diagram of the M16C/28 Group (M16C/28, M16C/28B), 64-pin package.

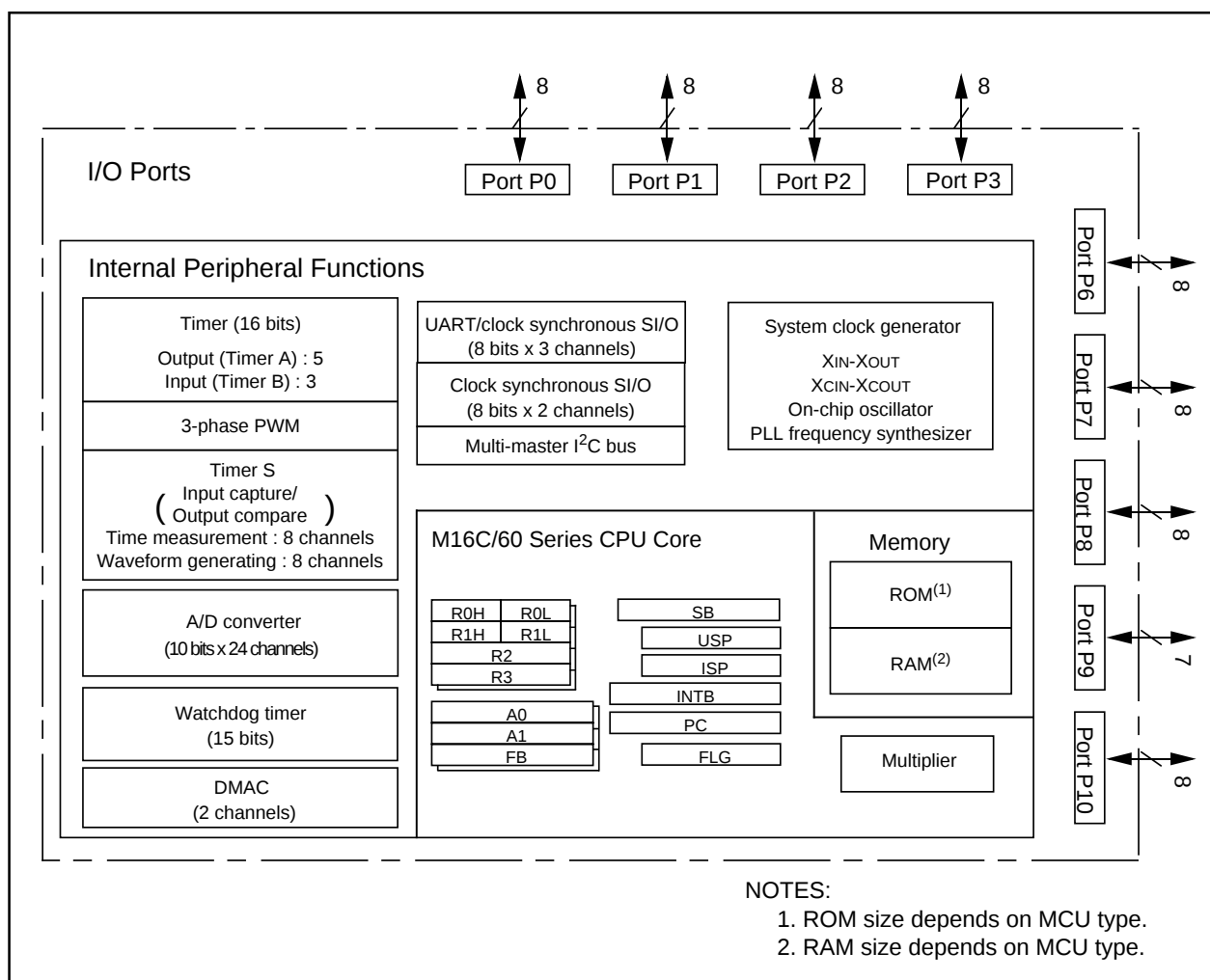


Figure 1.1 M16C/28 Group (M16C/28, M16C/28B), 80-Pin/85-Pin Block Diagram

1.4 Product Information

Tables 1.3 and 1.4 list the M16C/28 Group product information and Figure 1.3 shows the product numbering system. The specifications are partially different between normal-ver. and T/ V-ver..

Table 1.3 M16C/28 Product List -Normal-ver.

As of September, 2006

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30280F6WG (N)	48 K + 4 K	4 K	PTLG0085JB-A (85F0G)	Flash Memory	U3, U5, U7, U9
M30280F8WG (N)	64 K + 4 K	4 K			
M30280FAWG (N)	96 K + 4 K	8 K			
M30280F6HP (N)	48 K + 4 K	4 K	PLQP0080KB-A (80P6Q-A)		
M30280F8HP (N)	64 K + 4 K	4 K			
M30280FAHP (N)	96 K + 4 K	8 K			
M30280FCHP (N)	128 K + 4 K	12 K			
M30281F6HP (N)	48 K + 4 K	4 K	PLQP0064KB-A (64P6Q-A)		
M30281F8HP (N)	64 K + 4 K	4 K			
M30281FAHP (N)	96 K + 4 K	8 K			
M30281FCHP (N)	128 K + 4 K	12 K			
M30280M8-XXXHP (N)	64 K	4 K	PLQP0080KB-A (80P6Q-A)	Mask ROM	U3, U5
M30280MA-XXXHP (N)	96 K	8 K			
M30280MC-XXXHP (N)	128 K	12 K			
M30281M8-XXXHP (N)	64 K	4 K	PLQP0064KB-A (64P6Q-A)		
M30281MA-XXXHP (N)	96 K	8 K			
M30281MC-XXXHP (N)	128 K	12 K			

(N): New

Table 1.4 M16C/28B Product List -Normal-ver.

As of September, 2006

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30280FCBHP (D)	128 K + 4 K	12 K	PLQP0080KB-A (80P6Q-A)	Flash memory	U7
M30281FCBHP (D)	128 K + 4 K	12 K	PLQP0064KB-A (64P6Q-A)		

(D): Under development

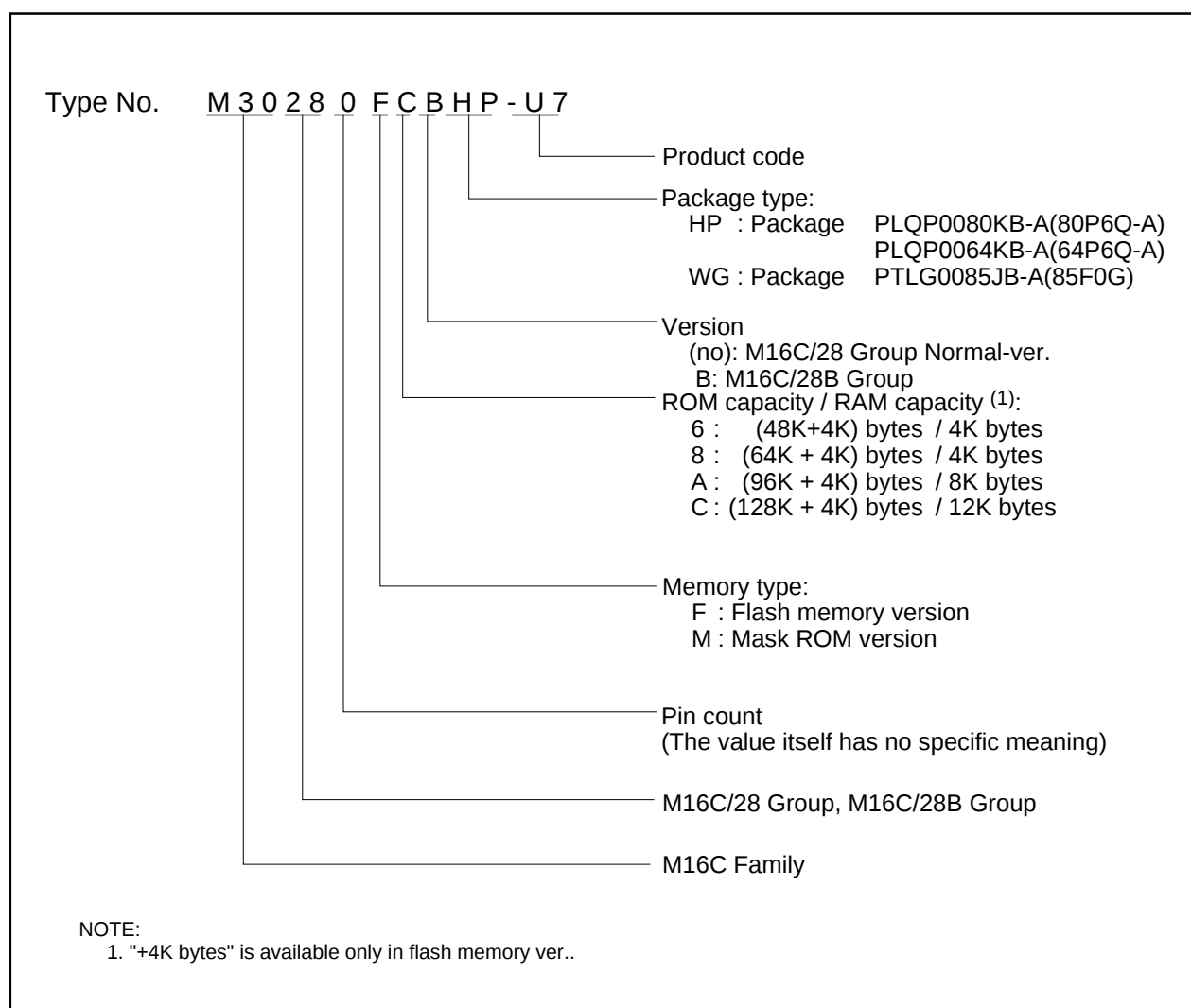


Figure 1.3 Product Numbering System

Table 1.5 Product Code (Flash Memory-ver.) - M16C/28 Normal-ver., 64-Pin⁽¹⁾/80-Pin⁽¹⁾/85-Pin Package

Product Code	Package	Internal ROM (User Program Space)		Internal ROM (Data Space)		Operating Ambient Temperature
		Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
U3	Lead free	100	0 to 60°C	100	0 to 60°C	-40 to 85°C
U5					-20 to 85°C	
U7		1,000		10,000	-40 to 85°C	-40 to 85°C
U9					-20 to 85°C	-20 to 85°C

NOTE:

1. The lead contained products, D3, D5, D7 and D9, are put together with U3, U5, U7 and U9 respectively. Lead-free (Sn-Ag-Cu plating) products can be mounted by both conventional Sn-Pb paste and Lead-free paste.

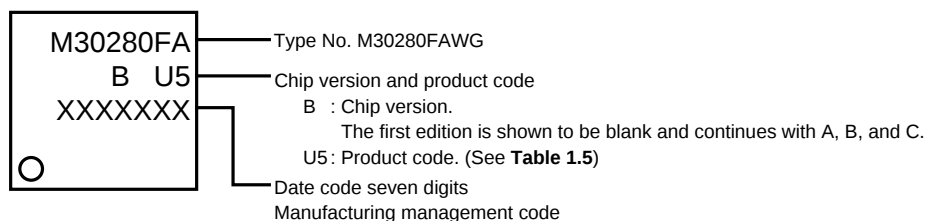
Table 1.6 Product Code (Flash Memory-ver.) - M16C/28B Normal-ver., 64-Pin/85-Pin Package

Product Code	Package	Internal ROM (User Program Space)		Internal ROM (Data Space)		Operating Ambient Temperature
		Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
U7	Lead-free	1,000	0 to 60°C	10,000	-40 to 85°C	-40 to 85°C

Table 1.7 Product Code (Mask ROM ver.) - M16C/28B Normal-ver., 64-Pin/80-Pin/85-Pin Package

Product Code	Package	Operating Ambient Temperature
U3	Lead-free	-40 to 85°C
U5		-20 to 85°C

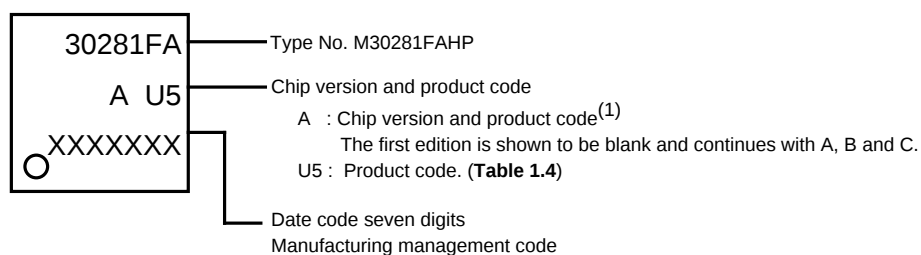
(1) Flash Memory Version, PTLG0085JB-A (85F0G), Normal-ver.



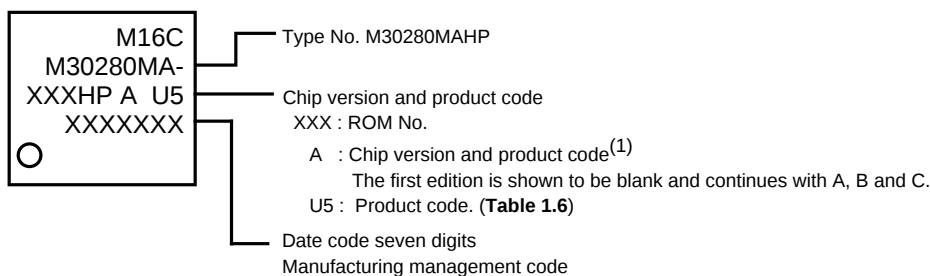
(2) Flash Memory Version, PLQP0080KB-A (80P6Q-A), Normal-ver.



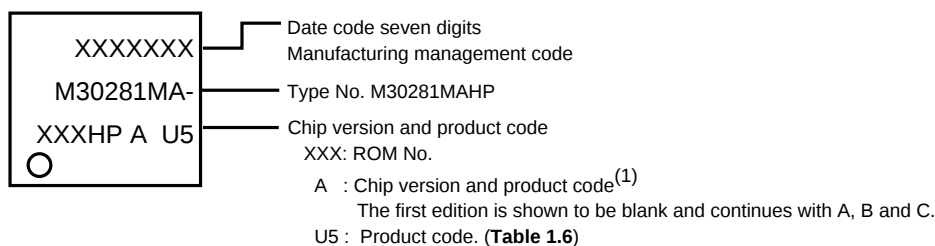
(3) Flash Memory Version, PLQP0064KB-A (64P6Q-A), Normal-ver.



(4) Mask ROM Version, PLQP0080KB-A (80P6Q-A), Normal-ver.



(5) Mask ROM Version, PLQP0064-KB-A (64P6Q-A), Normal-ver.



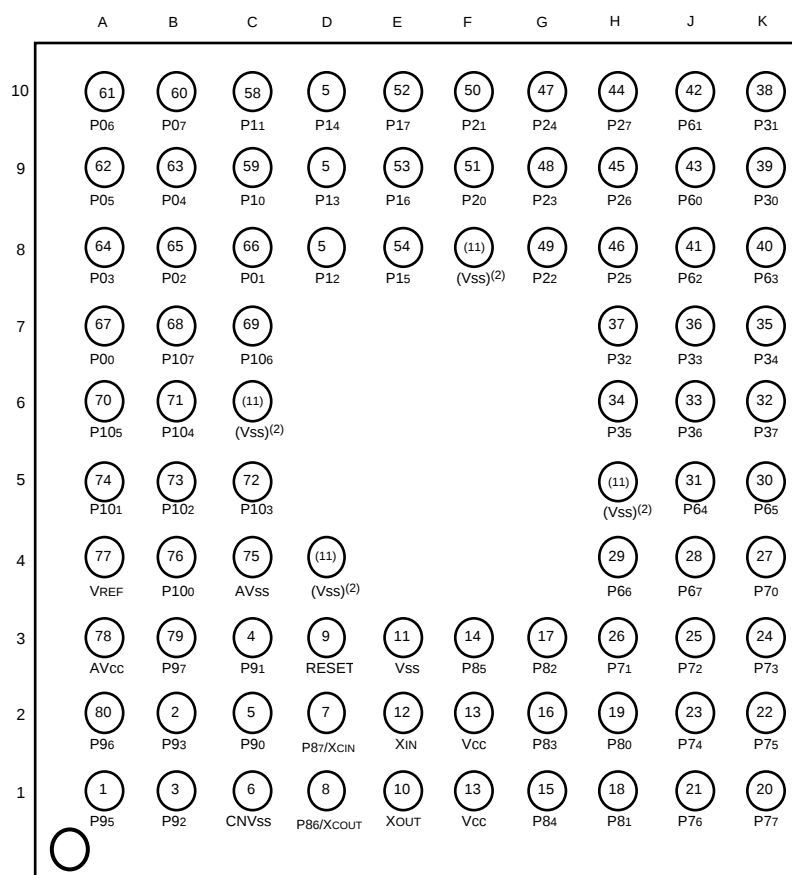
NOTES:

- The following functions are not available in the first version and version A products.
 - Delay trigger mode 0 of A/D conversion
 - Delay trigger mode 1 of A/D conversion

Figure 1.4 Marking Diagram-M16C/28 Normal-ver.

1.5 Pin Assignment

Figures 1.5 to 1.7 show the pin Assignments (top view).



NOTES :

1. The numbers in each grid (circle) show the pin numbers of the M30280FAHP (80P6Q-A package)
2. Connect grids written as (Vss) to Vss(GND) or leave them open.
3. Set PACR2 to PACR0 bits in the PACR register to "0112" before you input and output it after resetting to each pin. When the PACR register is not set, the input and output function of some pins are disabled.

Package: PTLG0085JB-A(85F0G)

Figure 1.5 Pin Assignment (Top View) of 85-pin Package

Table 1.8 Pin Characteristics for 85-pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I ² C bus Pin	Analog Pin	PLQP0080KB-A Pin Number
A1		P95				CLK4		AN25	1
A2		P96				SOUT4		AN26	80
A3	AVcc								78
A4	VREF								77
A5		P101						AN1	74
A6		P105	$\overline{\text{KI1}}$					AN5	70
A7		P00						AN00	67
A8		P03						AN03	64
A9		P05						AN05	62
A10		P06						AN06	61
B1		P92		TB2IN					3
B2		P93						AN24	2
B3		P97				SIN4		AN27	79
B4		P100						AN0	76
B5		P102						AN2	73
B6		P104	$\overline{\text{KI0}}$					AN4	71
B7		P107	$\overline{\text{KI3}}$					AN7	68
B8		P02						AN02	65
B9		P04						AN04	63
B10		P07						AN07	60
C1	CNVss								6
C2		P90		TB0IN					5
C3		P91		TB1IN					4
C4	AVss								75
C5		P103						AN3	72
C6	Vss ⁽¹⁾								(11)
C7		P106	$\overline{\text{KI2}}$					AN6	69
C8		P01						AN01	66
C9		P10						AN20	59
C10		P11						AN21	58
D1	XCOUT	P86							8
D2	XCIN	P87							7
D3	RESET								9
D4	Vss ⁽¹⁾								(11)
D8		P12						AN22	57
D9		P13						AN23	56
D10		P14							55
E1	XOUT								10
E2	XIN								12
E3	Vss								11

Table 1.9 Pin Characteristics for 80-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I ² C bus Pin	Analog Pin
41		P62				RxD0		
42		P61				CLK0		
43		P60				$\overline{\text{RTS}}_0 / \overline{\text{CTS}}_0$		
44		P27			OUTC17 / INPC17			
45		P26			OUTC16 / INPC16			
46		P25			OUTC15 / INPC15			
47		P24			OUTC14 / INPC14			
48		P23			OUTC13 / INPC13			
49		P22			OUTC12 / INPC12			
50		P21			OUTC11 / INPC11		SCLMM	
51		P20			OUTC10 / INPC10		SDAMM	
52		P17	$\overline{\text{INT}}_5$	IDU	INPC17			
53		P16	$\overline{\text{INT}}_4$	IDW				
54		P15	$\overline{\text{INT}}_3$	IDV				$\overline{\text{ADTRG}}$
55		P14						
56		P13						AN23
57		P12						AN22
58		P11						AN21
59		P10						AN20
60		P07						AN07
61		P06						AN06
62		P05						AN05
63		P04						AN04
64		P03						AN03
65		P02						AN02
66		P01						AN01
67		P00						AN00
68		P107	$\overline{\text{KI}}_3$					AN7
69		P106	$\overline{\text{KI}}_2$					AN6
70		P105	$\overline{\text{KI}}_1$					AN5
71		P104	$\overline{\text{KI}}_0$					AN4
72		P103						AN3
73		P102						AN2
74		P101						AN1
75	AVss							
76		P100						AN0
77	VREF							
78	AVcc							
79		P97				SIN4		AN27
80		P96				SOUT4		AN26

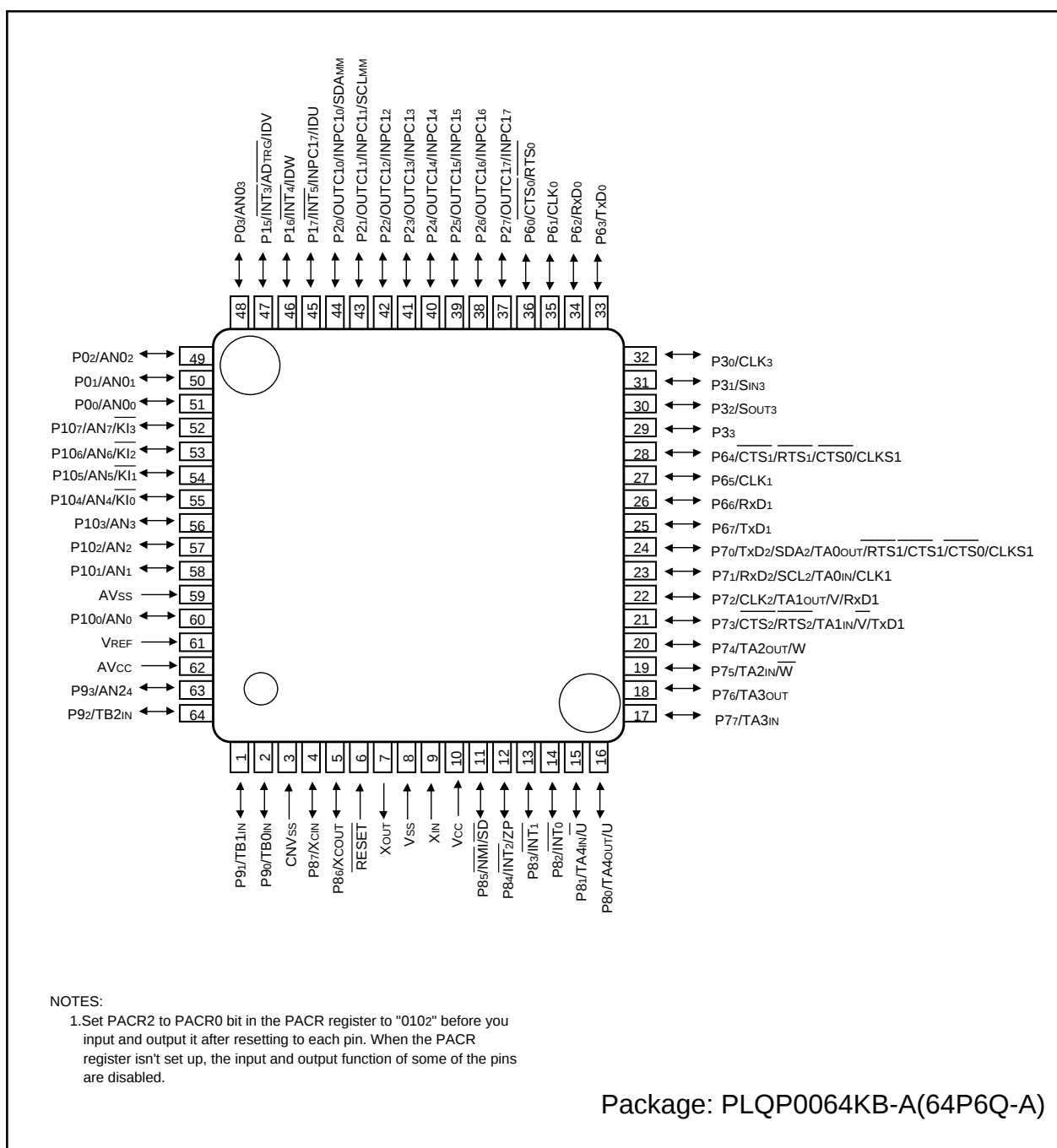


Figure 1.6 Pin Assignment (Top View) of 64-Pin Package

Table 10 Pin Characteristics for 64-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I ² C bus Pin	Analog Pin
41		P23			OUTC13 / INPC13			
42		P22			OUTC12 / INPC12			
43		P21			OUTC11 / INPC11		SCLMM	
44		P20			OUTC10 / INPC10		SDAMM	
45		P17	$\overline{\text{INT}}_5$	IDU	INPC17			
46		P16	$\overline{\text{INT}}_4$	IDW				
47		P15	$\overline{\text{INT}}_3$	IDV				$\overline{\text{ADTRG}}$
48		P03						AN03
49		P02						AN02
50		P01						AN01
51		P00						AN00
52		P107	$\overline{\text{KI}}_3$					AN7
53		P106	$\overline{\text{KI}}_2$					AN6
54		P105	$\overline{\text{KI}}_1$					AN5
55		P104	$\overline{\text{KI}}_0$					AN4
56		P103						AN3
57		P102						AN2
58		P101						AN1
59	AVss							
60		P100						AN0
61	VREF							
62	AVcc							
63		P93						AN24
64		P92		TB2IN				

1.6 Pin Description

Table 1.10 Pin Description (64-Pin, 80-Pin and 85-Pin Packages)

Classification	Symbol	I/O Type	Function
Power Supply	VCC, VSS	I	Apply 2.7 to 5.5V to the VCC pin. Apply 0V to the VSS pin.
Analog Power Supply	AVCC AVSS	I	Supplies power to the A/D converter. Connect the AVCC pin to VCC and the AVSS pin to VSS.
Reset Input	RESET	I	The MCU is in a reset state when "L" is applied to the RESET pin
CNVSS	CNVSS	I	Connect the CNVSS pin to VSS.
Main Clock Input	XIN	I	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, apply it to XIN and leave XOUT open. If XIN is not used (for external oscillator or external clock) connect XIN pin to VCC and leave XOUT open.
Main Clock Output	XOUT	O	
Sub Clock Input	XCIN	I	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT.
Sub Clock Output	XCOUT	O	
INT Interrupt Input	INT0 to INT5	I	Input pins for the INT interrupt. INT2 can be used for Timer A Z-phase function.
NMI Interrupt Input	NMI	I	Input pin for the NMI interrupt. NMI cannot be used as I/O port while the three-phase motor control is enabled. Apply a stable "H" to NMI after setting it's direction register to "0" when the three-phase motor control is enabled.
Key Input Interrupt	KI0 to KI3	I	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	I/O pins for the timer A0 to A4
	TA0IN to TA4IN	I	Input pins for the timer A0 to A4
	ZP	I	Input pin for Z-phase
Timer B	TB0IN to TB2IN	I	Input pins for the timer B0 to B2
Three-phase Motor Control Timer Output	U, $\bar{U}$, V, $\bar{V}$, W, $\bar{W}$	O	Output pins for the three-phase motor control timer
	IDU, IDW, IDV, $\bar{S}$	I/O	Input and output pins for the three-phase motor control timer
Serial I/O	CTS0 to CTS2	I	Input pins for data transmission control
	RTS0 to RTS2	O	Output pins for data reception control
	CLK0 to CLK3	I/O	Inputs and outputs the transfer clock
	RxD0 to RxD2	I	Inputs serial data
	TxD0 to TxD2	O	Outputs serial data
	CLKS1	O	Output pin for transfer clock
I ² C Mode	SDA2	I/O	Inputs and outputs serial data
	SCL2		Inputs and outputs the transfer clock
Multi-master I ² C bus	SDAMM	I/O	Inputs and outputs serial data
	SCLMM		Inputs and outputs the transfer clock
Reference Voltage Input	VREF	I	Applies reference voltage to the A/D converter
A/D Converter	AN0 to AN7 AN00 to AN03 AN24	I	Analog input pins for the A/D converter
	ADTRG		Input pin for an external A/D trigger

I : Input O : Output I/O : Input and output

Table 1.10 Pin Description (64-Pin, 80-Pin and 85-Pin Packages) (Continued)

Classification	Symbol	I/O Type	Function
Timer S	INPC1 ₀ to INPC1 ₇	I	Input pins for the time measurement function
	OUTC1 ₀ to OUTC1 ₇	O	Output pins for the waveform generating function
I/O Ports	P0 ₀ to P0 ₃ P1 ₅ to P1 ₇ P2 ₀ to P2 ₇ P3 ₀ to P3 ₃ P6 ₀ to P6 ₇ P7 ₀ to P7 ₇ P8 ₀ to P8 ₇ P10 ₀ to P10 ₇	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resistor available in 4-bit units
	P9 ₀ to P9 ₃	I/O	I/O ports having equivalent functions to P0

I : Input O : Output I/O : Input and output

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to 0.

2.8.3 Zero Flag (Z Flag)

This flag is set to 1 when an arithmetic operation resulted in 0; otherwise, it is 0.

2.8.4 Sign Flag (S Flag)

This flag is set to 1 when an arithmetic operation resulted in a negative value; otherwise, it is 0.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is 0 ; register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O Flag)

This flag is set to 1 when the operation resulted in an overflow; otherwise, it is 0.

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1. The I flag is cleared to 0 when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is 0; USP is selected when the U flag is 1.

The U flag is cleared to 0 when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write 0. When read, its content is indeterminate.

Table 4.2 SFR Information(2)⁽¹⁾

Address	Register	Symbol	After Reset
0040 ₁₆			
0041 ₁₆			
0042 ₁₆			
0043 ₁₆			
0044 ₁₆	INT3 interrupt control register	INT3IC	XX00X0002
0045 ₁₆	IC/OC 0 interrupt control register	ICOC0IC	XXXXX0002
0046 ₁₆	IC/OC 1 interrupt control register, I ² C bus interface interrupt control register	ICOC1IC, IICIC	XXXXX0002
0047 ₁₆	IC/OC base timer interrupt control register, SCLSDA interrupt control register	BTIC, SCLDAIC	XXXXX0002
0048 ₁₆	SI/O4 interrupt control register, INT5 interrupt control register	S4IC, INT5IC	XX00X0002
0049 ₁₆	SI/O3 interrupt control register, INT4 interrupt control register	S3IC, INT4IC	XX00X0002
004A ₁₆	UART2 Bus collision detection interrupt control register	BCNIC	XXXXX0002
004B ₁₆	DMA0 interrupt control register	DM0IC	XXXXX0002
004C ₁₆	DMA1 interrupt control register	DM1IC	XXXXX0002
004D ₁₆	Key input interrupt control register	KUPIC	XXXXX0002
004E ₁₆	A/D conversion interrupt control register	ADIC	XXXXX0002
004F ₁₆	UART2 transmit interrupt control register	S2TIC	XXXXX0002
0050 ₁₆	UART2 receive interrupt control register	S2RIC	XXXXX0002
0051 ₁₆	UART0 transmit interrupt control register	S0TIC	XXXXX0002
0052 ₁₆	UART0 receive interrupt control register	S0RIC	XXXXX0002
0053 ₁₆	UART1 transmit interrupt control register	S1TIC	XXXXX0002
0054 ₁₆	UART1 receive interrupt control register	S1RIC	XXXXX0002
0055 ₁₆	Timer A0 interrupt control register	TA0IC	XXXXX0002
0056 ₁₆	Timer A1 interrupt control register	TA1IC	XXXXX0002
0057 ₁₆	Timer A2 interrupt control register	TA2IC	XXXXX0002
0058 ₁₆	Timer A3 interrupt control register	TA3IC	XXXXX0002
0059 ₁₆	Timer A4 interrupt control register	TA4IC	XXXXX0002
005A ₁₆	Timer B0 interrupt control register	TB0IC	XXXXX0002
005B ₁₆	Timer B1 interrupt control register	TB1IC	XXXXX0002
005C ₁₆	Timer B2 interrupt control register	TB2IC	XXXXX0002
005D ₁₆	INT0 interrupt control register	INT0IC	XX00X0002
005E ₁₆	INT1 interrupt control register	INT1IC	XX00X0002
005F ₁₆	INT2 interrupt control register	INT2IC	XX00X0002
0060 ₁₆			
0061 ₁₆			
0062 ₁₆			
0063 ₁₆			
0064 ₁₆			
0065 ₁₆			
0066 ₁₆			
0067 ₁₆			
0068 ₁₆			
0069 ₁₆			
006A ₁₆			
006B ₁₆			
006C ₁₆			
006D ₁₆			
006E ₁₆			
006F ₁₆			
0070 ₁₆			
0071 ₁₆			
0072 ₁₆			
0073 ₁₆			
0074 ₁₆			
0075 ₁₆			
0076 ₁₆			
0077 ₁₆			
0078 ₁₆			
0079 ₁₆			
007A ₁₆			
007B ₁₆			
007C ₁₆			
007D ₁₆			
007E ₁₆			
007F ₁₆			

Note 1: The blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.4 SFR Information(4)(1)

Address	Register	Symbol	After Reset
0300 ₁₆ 0301 ₁₆	TM, WG register 0	G1TM0, G1PO0	XX ₁₆ XX ₁₆
0302 ₁₆ 0303 ₁₆	TM, WG register 1	G1TM1, G1PO1	XX ₁₆ XX ₁₆
0304 ₁₆ 0305 ₁₆	TM, WG register 2	G1TM2, G1PO2	XX ₁₆ XX ₁₆
0306 ₁₆ 0307 ₁₆	TM, WG register 3	G1TM3, G1PO3	XX ₁₆ XX ₁₆
0308 ₁₆ 0309 ₁₆	TM, WG register 4	G1TM4, G1PO4	XX ₁₆ XX ₁₆
030A ₁₆ 030B ₁₆	TM, WG register 5	G1TM5, G1PO5	XX ₁₆ XX ₁₆
030C ₁₆ 030D ₁₆	TM, WG register 6	G1TM6, G1PO6	XX ₁₆ XX ₁₆
030E ₁₆ 030F ₁₆	TM, WG register 7	G1TM7, G1PO7	XX ₁₆ XX ₁₆
0310 ₁₆	WG control register 0	G1POCR0	0X00XX002
0311 ₁₆	WG control register 1	G1POCR1	0X00XX002
0312 ₁₆	WG control register 2	G1POCR2	0X00XX002
0313 ₁₆	WG control register 3	G1POCR3	0X00XX002
0314 ₁₆	WG control register 4	G1POCR4	0X00XX002
0315 ₁₆	WG control register 5	G1POCR5	0X00XX002
0316 ₁₆	WG control register 6	G1POCR6	0X00XX002
0317 ₁₆	WG control register 7	G1POCR7	0X00XX002
0318 ₁₆	TM control register 0	G1TMCR0	00 ₁₆
0319 ₁₆	TM control register 1	G1TMCR1	00 ₁₆
031A ₁₆	TM control register 2	G1TMCR2	00 ₁₆
031B ₁₆	TM control register 3	G1TMCR3	00 ₁₆
031C ₁₆	TM control register 4	G1TMCR4	00 ₁₆
031D ₁₆	TM control register 5	G1TMCR5	00 ₁₆
031E ₁₆	TM control register 6	G1TMCR6	00 ₁₆
031F ₁₆	TM control register 7	G1TMCR7	00 ₁₆
0320 ₁₆ 0321 ₁₆	Base timer register	G1BT	XX ₁₆ XX ₁₆
0322 ₁₆	Base timer control register 0	G1BCR0	00 ₁₆
0323 ₁₆	Base timer control register 1	G1BCR1	00 ₁₆
0324 ₁₆	TM prescale register 6	G1TPR6	00 ₁₆
0325 ₁₆	TM prescale register 7	G1TPR7	00 ₁₆
0326 ₁₆	Function enable register	G1FE	00 ₁₆
0327 ₁₆	Function select register	G1FS	00 ₁₆
0328 ₁₆ 0329 ₁₆	Base timer reset register	G1BTRR	XX ₁₆ XX ₁₆
032A ₁₆ 032B ₁₆	Divider register	G1DV	00 ₁₆
032C ₁₆			
032D ₁₆			
032E ₁₆			
032F ₁₆			
0330 ₁₆	Interrupt request register	G1IR	XX ₁₆
0331 ₁₆	Interrupt enable register 0	G1IE0	00 ₁₆
0332 ₁₆	Interrupt enable register 1	G1IE1	00 ₁₆
0333 ₁₆			
0334 ₁₆			
0335 ₁₆			
0336 ₁₆			
0337 ₁₆			
0338 ₁₆			
0339 ₁₆			
033A ₁₆			
033B ₁₆			
033C ₁₆			
033D ₁₆			
033E ₁₆	NMI digital debounce register	NDDR	FF ₁₆
033F ₁₆	P17 digital debounce register	P17DDR	FF ₁₆

Note 1: The blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.5 SFR Information(5)(1)

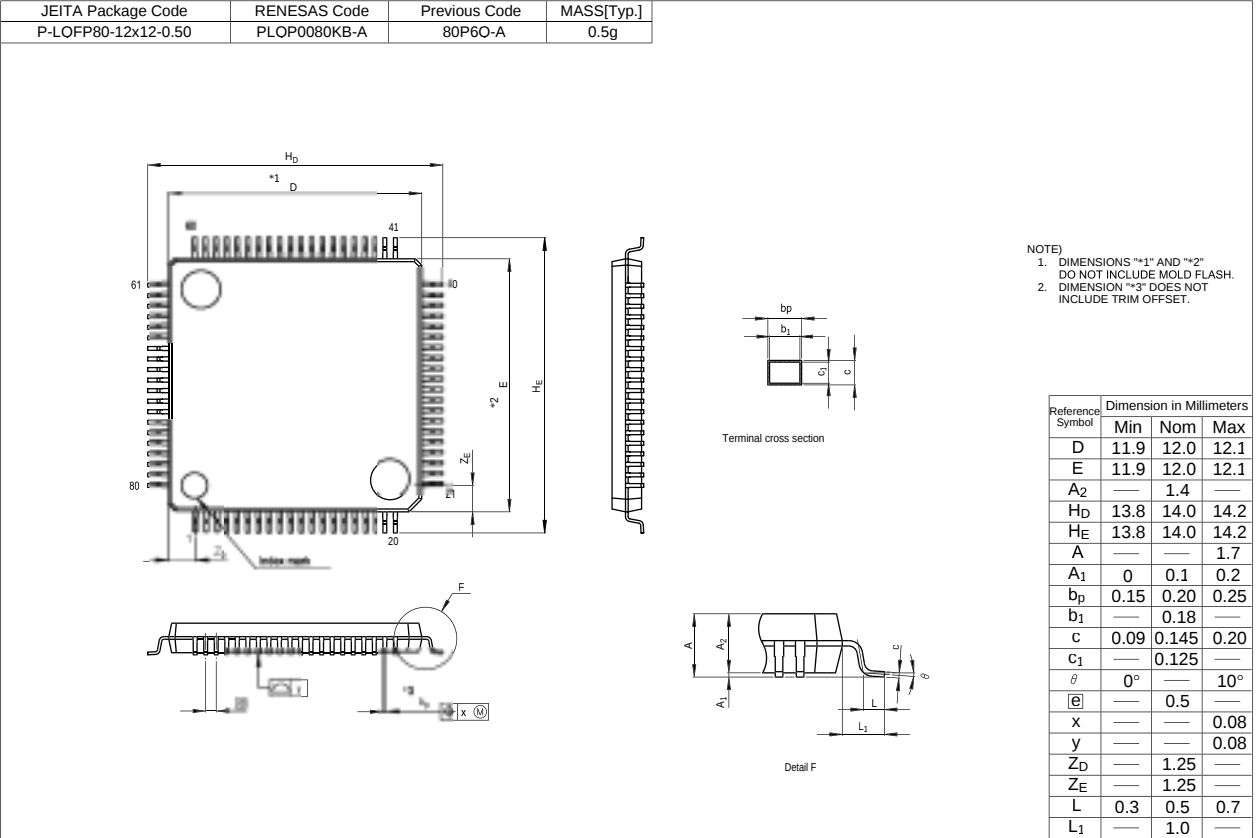
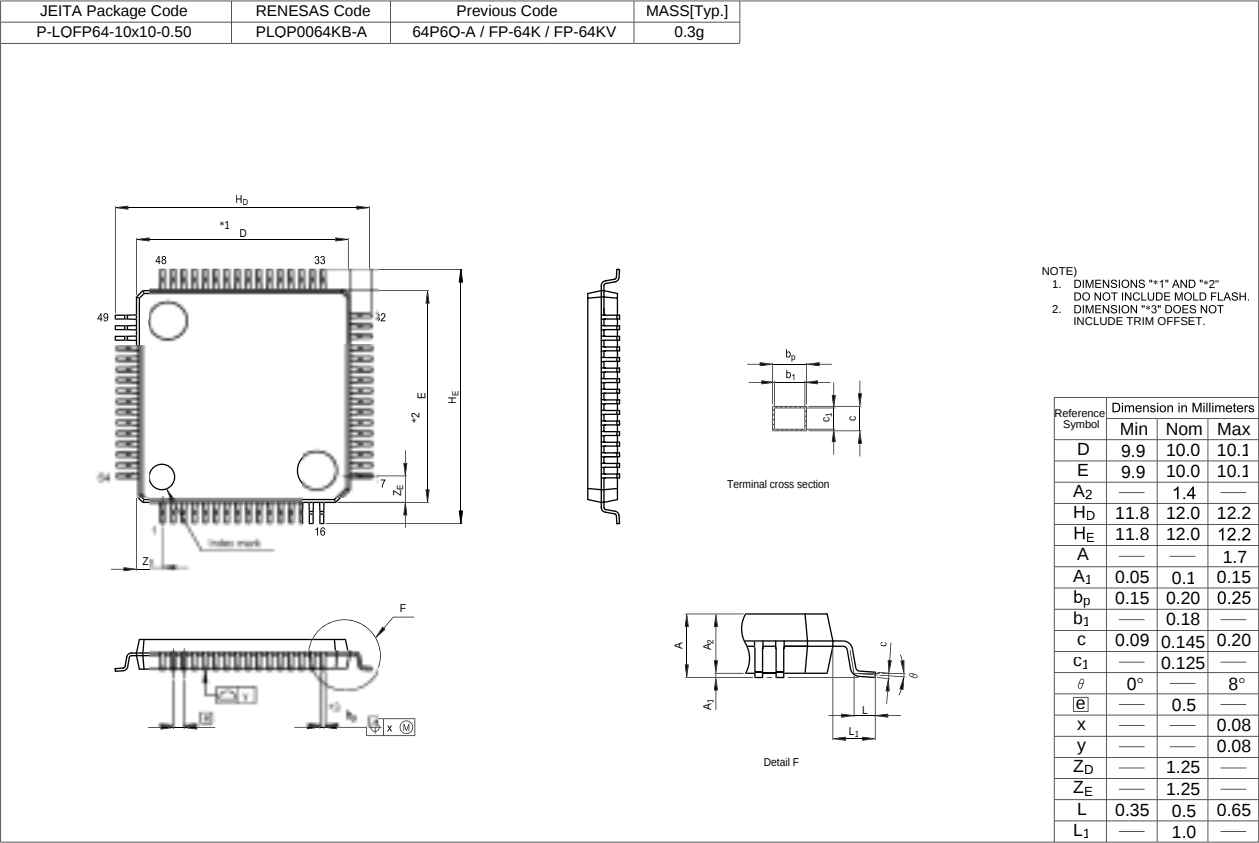
Address	Register	Symbol	After Reset
0340 ₁₆			
0341 ₁₆			
0342 ₁₆	Timer A1-1 register	TA11	XX16
0343 ₁₆			XX16
0344 ₁₆	Timer A2-1 register	TA21	XX16
0345 ₁₆			XX16
0346 ₁₆	Timer A4-1 register	TA41	XX16
0347 ₁₆			XX16
0348 ₁₆	Three-phase PWM control register 0	INVC0	0016
0349 ₁₆	Three-phase PWM control register 1	INVC1	0016
034A ₁₆	Three-phase output buffer register 0	IDB0	001111112
034B ₁₆	Three-phase output buffer register 1	IDB1	001111112
034C ₁₆	Dead time timer	DTT	XX16
034D ₁₆	Timer B2 interrupt occurrence frequency set counter	ICTB2	XX16
034E ₁₆	Position-data-retain function control register	PDRF	XXXX00002
034F ₁₆			
0350 ₁₆			
0351 ₁₆			
0352 ₁₆			
0353 ₁₆			
0354 ₁₆			
0355 ₁₆			
0356 ₁₆			
0357 ₁₆			
0358 ₁₆			
0359 ₁₆			
035A ₁₆			
035B ₁₆			
035C ₁₆			
035D ₁₆			
035E ₁₆	Interrupt request cause select register 2	IFSR2A	00XXXXX02(2)
035F ₁₆	Interrupt request cause select register	IFSR	0016
0360 ₁₆	SI/O3 transmit/receive register	S3TRR	XX16
0361 ₁₆			
0362 ₁₆	SI/O3 control register	S3C	010000002
0363 ₁₆	SI/O3 bit rate generator	S3BRG	XX16
0364 ₁₆	SI/O4 transmit/receive register	S4TRR	XX16
0365 ₁₆			
0366 ₁₆	SI/O4 control register	S4C	010000002
0367 ₁₆	SI/O4 bit rate generator	S4BRG	XX16
0368 ₁₆			
0369 ₁₆			
036A ₁₆			
036B ₁₆			
036C ₁₆			
036D ₁₆			
036E ₁₆			
036F ₁₆			
0370 ₁₆			
0371 ₁₆			
0372 ₁₆			
0373 ₁₆			
0374 ₁₆	UART2 special mode register 4	U2SMR4	0016
0375 ₁₆	UART2 special mode register 3	U2SMR3	000X0X0X2
0376 ₁₆	UART2 special mode register 2	U2SMR2	X00000002
0377 ₁₆	UART2 special mode register	U2SMR	X00000002
0378 ₁₆	UART2 transmit/receive mode register	U2MR	0016
0379 ₁₆	UART2 bit rate generator	U2BRG	XX16
037A ₁₆	UART2 transmit buffer register	U2TB	XX16
037B ₁₆			XX16
037C ₁₆	UART2 transmit/receive control register 0	U2C0	000010002
037D ₁₆	UART2 transmit/receive control register 1	U2C1	000000102
037E ₁₆	UART2 receive buffer register	U2RB	XX16
037F ₁₆			XX16

Note 1: The blank spaces are reserved. No access is allowed.

Note 2: Write 1 to bit 0 after reset.

X : Undefined

Appendix 1. Package Dimensions



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