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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	M16C/60
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, IEBus, SIO, UART/USART
Peripherals	DMA, POR, PWM, Voltage Detect, WDT
Number of I/O	71
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	85-TFLGA
Supplier Device Package	85-TFLGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/m30280fawg-u5b

1.3 Block Diagram

Figure 1.1 is a block diagram of the M16C/28 Group (M16C/28, M16C/28B), 80-pin and 85-pin package.
Figure 1.2 is a block diagram of the M16C/28 Group (M16C/28, M16C/28B), 64-pin package.
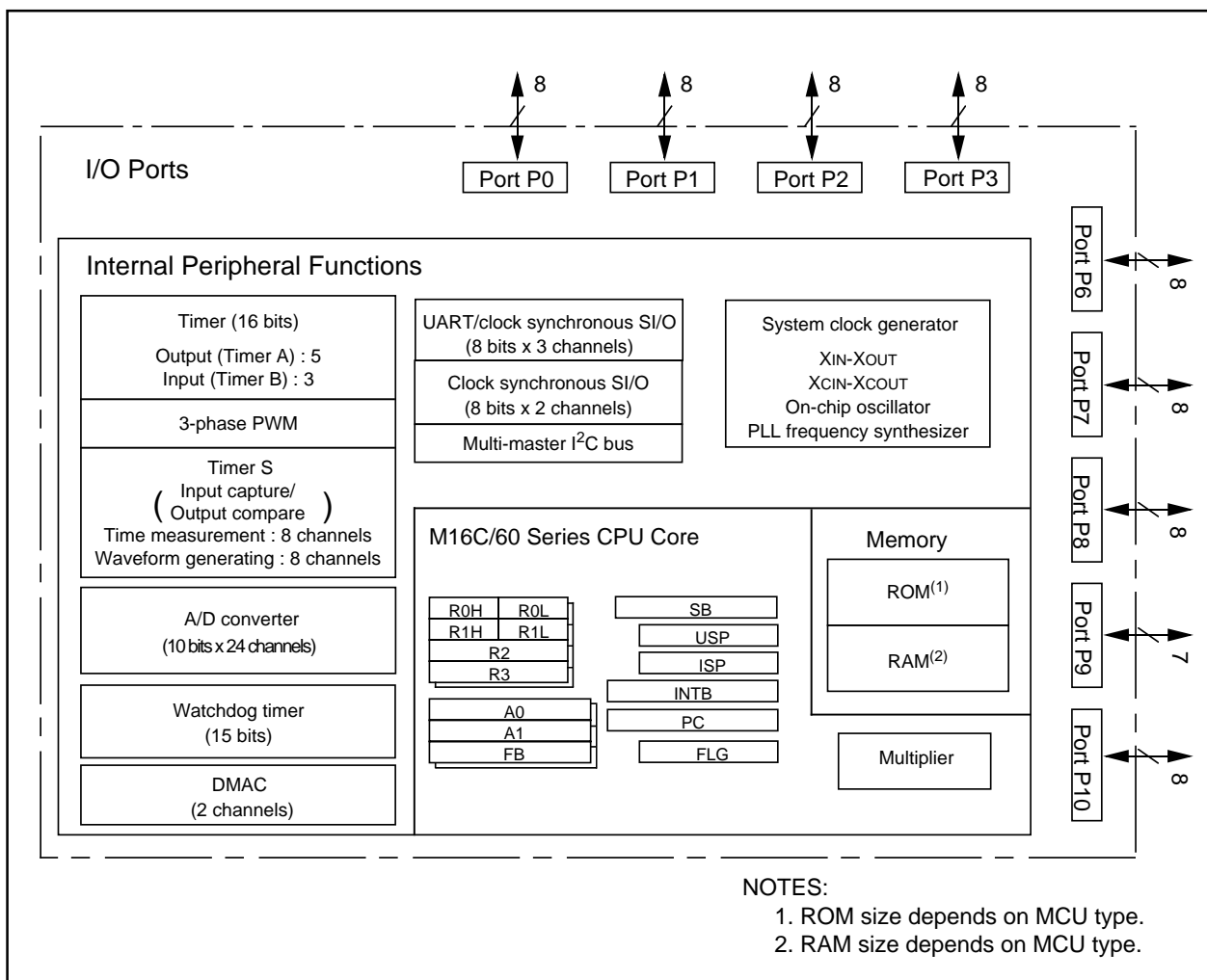
Figure 1.1 M16C/28 Group (M16C/28, M16C/28B), 80-Pin/85-Pin Block Diagram
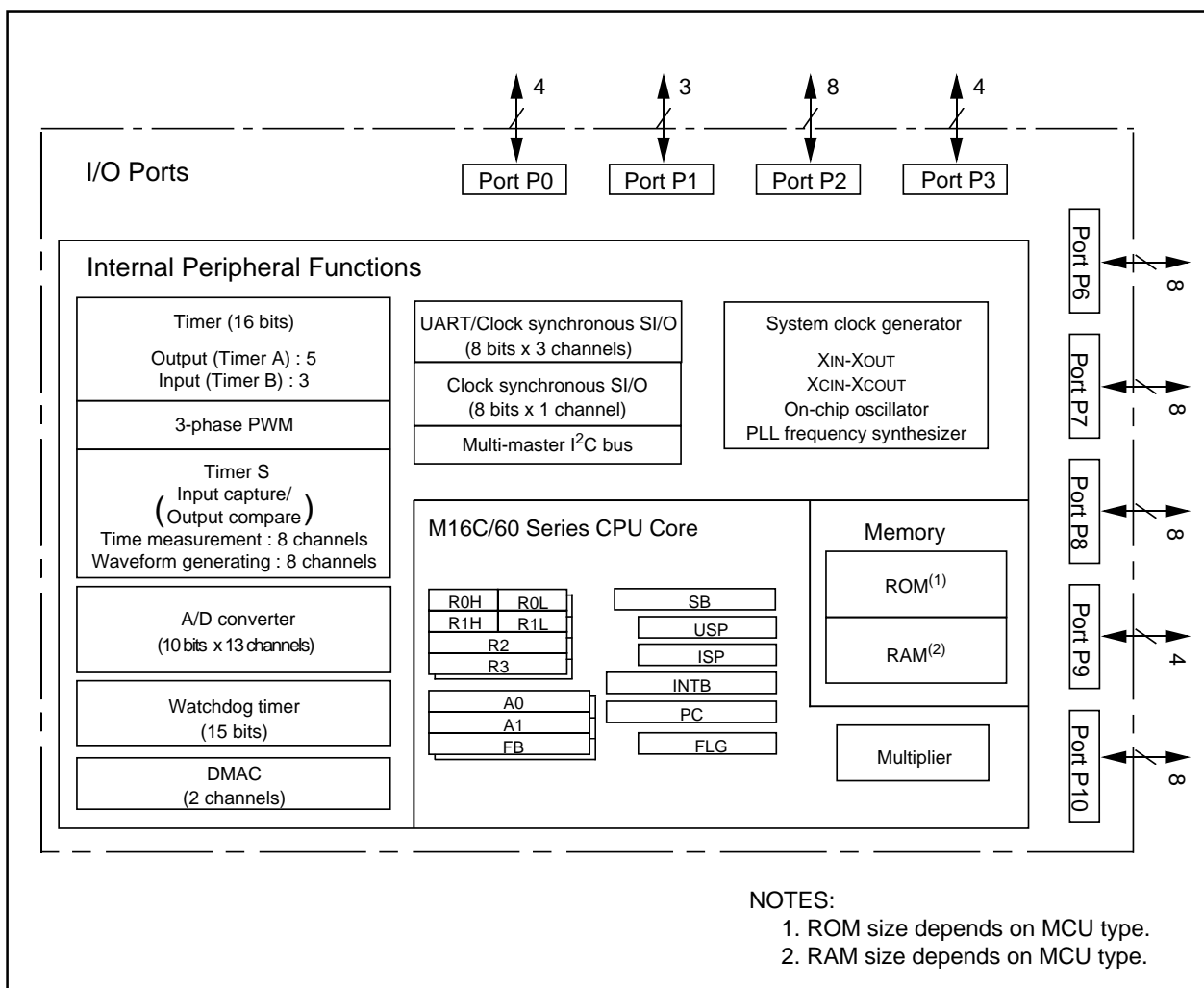
Figure 1.2 M16C/28 Group (M16C/28, M16C/28B), 64-Pin Block Diagram

I/O Ports

Port P0   Port P1   Port P2   Port P3

4   3   8   4

Port P6   8
Port P7   8
Port P8   8
Port P9   4
Port P10   8

Internal Peripheral Functions

Timer (16 bits)
Output (Timer A) : 5
Input (Timer B) : 3

3-phase PWM

Timer S
(Input capture/
Output compare)
Time measurement : 8 channels
Waveform generating : 8 channels

A/D converter
(10 bits x 13 channels)

Watchdog timer
(15 bits)

DMAC
(2 channels)

UART/Clock synchronous SI/O
(8 bits x 3 channels)

Clock synchronous SI/O
(8 bits x 1 channel)

Multi-master I^2C bus

System clock generator
X_{IN}-X_{OUT}
X_{CIN}-X_{COUT}
On-chip oscillator
PLL frequency synthesizer

M16C/60 Series CPU Core

R0H | R0L
R1H | R1L
R2
R3
A0
A1
FB

SB
USP
ISP
INTB
PC
FLG

Memory

ROM[1]

RAM[2]

Multiplier

NOTES:
1. ROM size depends on MCU type.
2. RAM size depends on MCU type.

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1.4 Product Information

Tables 1.3 and **1.4** list the M16C/28 Group product information and **Figure 1.3** shows the product numbering system. The specifications are partially different between normal-ver.and T/ V-ver..

Table 1.3 M16C/28 Product List -Normal-ver.　　　　　　　　　**As of September, 2006**

Type Number		ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30280F6WG	(N)	48 K + 4 K	4 K	PTLG0085JB-A (85F0G)	Flash Memory	U3, U5, U7, U9
M30280F8WG	(N)	64 K + 4 K	4 K			
M30280FAWG	(N)	96 K + 4 K	8 K			
M30280F6HP	(N)	48 K + 4 K	4 K	PLQP0080KB-A (80P6Q-A)		
M30280F8HP	(N)	64 K + 4 K	4 K			
M30280FAHP	(N)	96 K + 4 K	8 K			
M30280FCHP	(N)	128 K + 4 K	12 K			
M30281F6HP	(N)	48 K + 4 K	4 K	PLQP0064KB-A (64P6Q-A)		
M30281F8HP	(N)	64 K + 4 K	4 K			
M30281FAHP	(N)	96 K + 4 K	8 K			
M30281FCHP	(N)	128 K + 4 K	12 K			
M30280M8-XXXHP	(N)	64 K	4 K	PLQP0080KB-A (80P6Q-A)	Mask ROM	U3, U5
M30280MA-XXXHP	(N)	96 K	8 K			
M30280MC-XXXHP	(N)	128 K	12 K			
M30281M8-XXXHP	(N)	64 K	4 K	PLQP0064KB-A (64P6Q-A)		
M30281MA-XXXHP	(N)	96 K	8 K			
M30281MC-XXXHP	(N)	128 K	12 K			

(N): New

Table 1.4 M16C/28B Product List -Normal-ver.　　　　　　　　　**As of September, 2006**

Type Number		ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30280FCBHP	(D)	128 K + 4 K	12 K	PLQP0080KB-A (80P6Q-A)	Flash memory	U7
M30281FCBHP	(D)	128 K + 4 K	12 K	PLQP0064KB-A (64P6Q-A)		

(D): Under development

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Type No.   M 3 0 2 8 0 F C B H P - U 7

—— Product code

Package type:
  HP : Package   PLQP0080KB-A(80P6Q-A)
                  PLQP0064KB-A(64P6Q-A)
  WG : Package   PTLG0085JB-A(85F0G)

Version
  (no): M16C/28 Group Normal-ver.
  B: M16C/28B Group

ROM capacity / RAM capacity [1]:
  6 :   (48K+4K) bytes / 4K bytes
  8 :   (64K + 4K) bytes / 4K bytes
  A :   (96K + 4K) bytes / 8K bytes
  C : (128K + 4K) bytes / 12K bytes

Memory type:
  F : Flash memory version
  M : Mask ROM version

Pin count
(The value itself has no specific meaning)

M16C/28 Group, M16C/28B Group

M16C Family

NOTE:
    1. "+4K bytes" is available only in flash memory ver..

Figure 1.3 Product Numbering System

1.5 Pin Assignment

Figures 1.5 to 1.7 show the pin Assignments (top view).
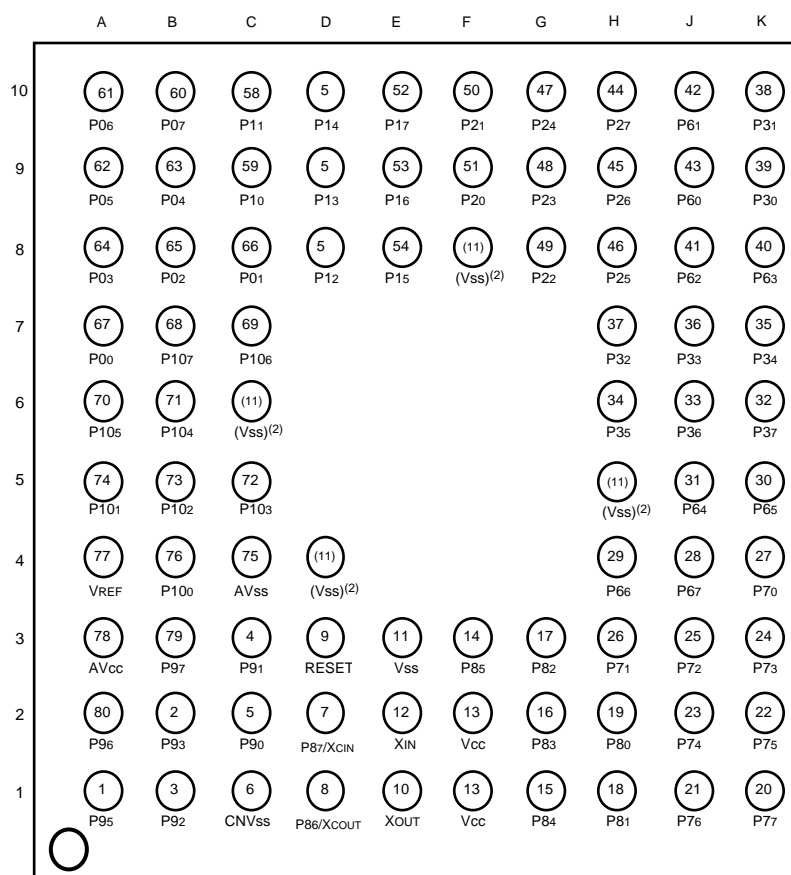
NOTES :
1. The numbers in each grid (circle) show the pin numbers of the M30280FAHP (80P6Q-A package)
2. Connect grids written as (Vss) to Vss(GND) or leave them open.
3. Set PACR2 to PACR0 bits in the PACR register to "0112" before you input and output it after resetting to each pin. When the PACR register is not set, the input and output function of some pins are disabled.

Package: PTLG0085JB-A(85F0G)

Figure 1.5 Pin Assignment (Top View) of 85-pin Package

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Table 1.8 Pin Characteristics for 85-pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I²C bus Pin	Analog Pin	PLQP0080KB-A Pin Number
A1		$P9_5$				CLK_4		$AN2_5$	1
A2		$P9_6$				S_{OUT4}		$AN2_6$	80
A3	AV_{CC}								78
A4	V_{REF}								77
A5		$P10_1$						AN_1	74
A6		$P10_5$	$\overline{KI_1}$					AN_5	70
A7		$P0_0$						$AN0_0$	67
A8		$P0_3$						$AN0_3$	64
A9		$P0_5$						$AN0_5$	62
A10		$P0_6$						$AN0_6$	61
B1		$P9_2$		$TB2_{IN}$					3
B2		$P9_3$						$AN2_4$	2
B3		$P9_7$				S_{IN4}		$AN2_7$	79
B4		$P10_0$						AN_0	76
B5		$P10_2$						AN_2	73
B6		$P10_4$	$\overline{KI_0}$					AN_4	71
B7		$P10_7$	$\overline{KI_3}$					AN_7	68
B8		$P0_2$						$AN0_2$	65
B9		$P0_4$						$AN0_4$	63
B10		$P0_7$						$AN0_7$	60
C1	CNV_{SS}								6
C2		$P9_0$		$TB0_{IN}$					5
C3		$P9_1$		$TB1_{IN}$					4
C4	AV_{SS}								75
C5		$P10_3$						AN_3	72
C6	$V_{SS}^{(1)}$								(11)
C7		$P10_6$	$\overline{KI_2}$					AN_6	69
C8		$P0_1$						$AN0_1$	66
C9		$P1_0$						$AN2_0$	59
C10		$P1_1$						$AN2_1$	58
D1	X_{COUT}	$P8_6$							8
D2	X_{CIN}	$P8_7$							7
D3	$\overline{RESET}$								9
D4	$V_{SS}^{(1)}$								(11)
D8		$P1_2$						$AN2_2$	57
D9		$P1_3$						$AN2_3$	56
D10		$P1_4$							55
E1	X_{OUT}								10
E2	X_{IN}								12
E3	V_{SS}								11

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Table 1.8 Pin Characteristics for 85-pin Package (continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I²C bus Pin	Analog Pin	PLQP0080KB-A Pin Number
E8		P1_5	$\overline{INT_3}$	IDV				$\overline{AD}_{TRG}$	54
E9		P1_6	$\overline{INT_4}$	IDW					53
E10		P1_7	$\overline{INT_5}$	IDU	INPC1_7				52
F1	Vcc								13
F2	Vcc								13
F3		P8_5	$\overline{NMI}$	$\overline{SD}$					14
F8	Vss(1)								(11)
F9		P2_0			OUTC1_0 / INPC1_0		SDA_MM		51
F10		P2_1			OUTC1_1 / INPC1_1		SCL_MM		50
G1		P8_4	$\overline{INT_2}$	ZP					15
G2		P8_3	$\overline{INT_1}$						16
G3		P8_2	$\overline{INT_0}$						17
G8		P2_2			OUTC1_2 / INPC1_2				49
G9		P2_3			OUTC1_3 / INPC1_3				48
G10		P2_4			OUTC1_4 / INPC1_4				47
H1		P8_1		TA4_IN / $\overline{U}$					18
H2		P8_0		TA4_OUT / U					19
H3		P7_1		TA0_IN		RxD_2 / SCL_2 / CLK_1			26
H4		P6_6				RxD_1			29
H5	Vss(1)								(11)
H6		P3_5							34
H7		P3_2				S_OUT3			37
H8		P2_5			OUTC1_5 / INPC1_5				46
H9		P2_6			OUTC1_6 / INPC1_6				45
H10		P2_7			OUTC1_7 / INPC1_7				44
J1		P7_6		TA3_OUT					21
J2		P7_4		TA2_OUT / W					23
J3		P7_2		TA1_OUT / V		CLK_2 / RxD_1			25
J4		P6_7				TxD_1			28
J5		P6_4				$\overline{RTS_1}$ / $\overline{CTS_1}$ / $\overline{CTS_0}$ / CLKS_1			31
J6		P3_6							33
J7		P3_3							36
J8		P6_2				RxD_0			41
J9		P6_0				$\overline{RTS_0}$ / $\overline{CTS_0}$			43
J10		P6_1				CLK_0			42
K1		P7_7		TA3_IN					20
K2		P7_5		TA2_IN / $\overline{W}$					22
K3		P7_3		TA1_IN / $\overline{V}$		$\overline{CTS_2}$ / $\overline{RTS_2}$ / $\overline{TXD_1}$			24
K4		P7_0		TA0_OUT		TxD_2 / SDA_2 / $\overline{RTS_1}$ / $\overline{CTS_1}$ / $\overline{CTS_0}$ / CLKS_1			27
K5		P6_5				CLK_1			30
K6		P3_7							32
K7		P3_4							35
K8		P6_3				TxD_0			40
K9		P3_0				CLK_3			39
K10		P3_1				S_IN3			38

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Table 1.9 Pin Characteristics for 80-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I^{2}C bus Pin	Analog Pin
1		P9$_5$				CLK$_4$		AN2$_5$
2		P9$_3$						AN2$_4$
3		P9$_2$		TB2$_{IN}$				
4		P9$_1$		TB1$_{IN}$				
5		P9$_0$		TB0$_{IN}$				
6	CNV$_{SS}$							
7	X$_{CIN}$	P8$_7$						
8	X$_{COUT}$	P8$_6$						
9	$\overline{RESET}$							
10	X$_{OUT}$							
11	V$_{SS}$							
12	X$_{IN}$							
13	V$_{CC}$							
14		P8$_5$	$\overline{NMI}$	$\overline{SD}$				
15		P8$_4$	$\overline{INT_2}$	ZP				
16		P8$_3$	$\overline{INT_1}$					
17		P8$_2$	$\overline{INT_0}$					
18		P8$_1$		TA4$_{IN}$ / $\overline{U}$				
19		P8$_0$		TA4$_{OUT}$ / U				
20		P7$_7$		TA3$_{IN}$				
21		P7$_6$		TA3$_{OUT}$				
22		P7$_5$		TA2$_{IN}$ / $\overline{W}$				
23		P7$_4$		TA2$_{OUT}$ / W				
24		P7$_3$		TA1$_{IN}$ / $\overline{V}$		$\overline{CTS_2}$ / $\overline{RTS_2}$ / TxD$_1$		
25		P7$_2$		TA1$_{OUT}$ / V		CLK$_2$ / RxD$_1$		
26		P7$_1$		TA0$_{IN}$		RxD$_2$ / SCL$_2$ / CLK$_1$		
27		P7$_0$		TA0$_{OUT}$		TxD$_2$ / SDA$_2$ / $\overline{RTS_1}$ / $\overline{CTS_1}$ / $\overline{CTS_0}$ / CLKS$_1$		
28		P6$_7$				TxD$_1$		
29		P6$_6$				RxD$_1$		
30		P6$_5$				CLK$_1$		
31		P6$_4$				RTS$_1$ / $\overline{CTS_1}$ / $\overline{CTS_0}$ / CLKS$_1$		
32		P3$_7$						
33		P3$_6$						
34		P3$_5$						
35		P3$_4$						
36		P3$_3$						
37		P3$_2$				S$_{OUT3}$		
38		P3$_1$				S$_{IN3}$		
39		P3$_0$				CLK$_3$		
40		P6$_3$				TxD$_0$		

Table 1.9 Pin Characteristics for 80-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I^{2}C bus Pin	Analog Pin
41		P6$_2$				R$_X$D$_0$		
42		P6$_1$				CLK$_0$		
43		P6$_0$				$\overline{RTS_0}$ / $\overline{CTS_0}$		
44		P2$_7$			OUTC1$_7$ / INPC1$_7$			
45		P2$_6$			OUTC1$_6$ / INPC1$_6$			
46		P2$_5$			OUTC1$_5$ / INPC1$_5$			
47		P2$_4$			OUTC1$_4$ / INPC1$_4$			
48		P2$_3$			OUTC1$_3$ / INPC1$_3$			
49		P2$_2$			OUTC1$_2$ / INPC1$_2$			
50		P2$_1$			OUTC1$_1$ / INPC1$_1$		SCL$_{MM}$	
51		P2$_0$			OUTC1$_0$ / INPC1$_0$		SDA$_{MM}$	
52		P1$_7$	$\overline{INT_5}$	IDU	INPC1$_7$			
53		P1$_6$	$\overline{INT_4}$	IDW				
54		P1$_5$	$\overline{INT_3}$	IDV				$\overline{ADTRG}$
55		P1$_4$						
56		P1$_3$						AN2$_3$
57		P1$_2$						AN2$_2$
58		P1$_1$						AN2$_1$
59		P1$_0$						AN2$_0$
60		P0$_7$						AN0$_7$
61		P0$_6$						AN0$_6$
62		P0$_5$						AN0$_5$
63		P0$_4$						AN0$_4$
64		P0$_3$						AN0$_3$
65		P0$_2$						AN0$_2$
66		P0$_1$						AN0$_1$
67		P0$_0$						AN0$_0$
68		P10$_7$	$\overline{KI_3}$					AN$_7$
69		P10$_6$	$\overline{KI_2}$					AN$_6$
70		P10$_5$	$\overline{KI_1}$					AN$_5$
71		P10$_4$	$\overline{KI_0}$					AN$_4$
72		P10$_3$						AN$_3$
73		P10$_2$						AN$_2$
74		P10$_1$						AN$_1$
75	AV$_{SS}$							
76		P10$_0$						AN$_0$
77	V$_{REF}$							
78	AV$_{CC}$							
79		P9$_7$				S$_{IN4}$		AN2$_7$
80		P9$_6$				S$_{OUT4}$		AN2$_6$

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Table 1.10 Pin Characteristics for 64-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Mult-master I^{2}C bus Pin	Analog Pin
1		P9$_1$		TA$_1$IN				
2		P9$_0$		TB$_0$IN				
3	CNVss							
4	X$_{CIN}$	P8$_7$						
5	X$_{COUT}$	P8$_6$						
6	$\overline{\text{RESET}}$							
7	X$_{OUT}$							
8	Vss							
9	X$_{IN}$							
10	Vcc							
11		P8$_5$	$\overline{\text{NMI}}$	$\overline{\text{SD}}$				
12		P8$_4$	$\overline{\text{INT}_2}$	ZP				
13		P8$_3$	$\overline{\text{INT}_1}$					
14		P8$_2$	$\overline{\text{INT}_0}$					
15		P8$_1$		TA$_4$IN / $\overline{\text{U}}$				
16		P8$_0$		TA$_4$OUT / U				
17		P7$_7$		TA$_3$IN				
18		P7$_6$		TA$_3$OUT				
19		P7$_5$		TA$_2$IN / $\overline{\text{W}}$				
20		P7$_4$		TA$_2$OUT / W				
21		P7$_3$		TA$_1$IN / $\overline{\text{V}}$		$\overline{\text{CTS}_2}$ / $\overline{\text{RTS}_2}$ / TxD$_1$		
22		P7$_2$		TA$_1$OUT / V		CLK$_2$ / RxD$_1$		
23		P7$_1$		TA$_0$IN		RxD$_2$ / SCL$_2$ / CLK$_1$		
24		P7$_0$		TA$_0$OUT		TxD$_2$ / SDA$_2$ / $\overline{\text{RTS}_1}$ / $\overline{\text{CTS}_1}$ / $\overline{\text{CTS}_0}$ / CLKS$_1$		
25		P6$_7$				TxD$_1$		
26		P6$_6$				RxD$_1$		
27		P6$_5$				CLK$_1$		
28		P6$_4$				RTS$_1$ / $\overline{\text{CTS}_1}$/ $\overline{\text{CTS}_0}$ / CLKS$_1$		
29		P3$_3$						
30		P3$_2$				S$_{OUT3}$		
31		P3$_1$				S$_{IN3}$		
32		P3$_0$				CLK$_3$		
33		P6$_3$				TxD$_0$		
34		P6$_2$				RxD$_0$		
35		P6$_1$				CLK$_0$		
36		P6$_0$				$\overline{\text{RTS}_0}$ / $\overline{\text{CTS}_0}$		
37		P2$_7$			OUTC1$_7$ / INPC1$_7$			
38		P2$_6$			OUTC1$_6$ / INPC1$_6$			
39		P2$_5$			OUTC1$_5$ / INPC1$_5$			
40		P2$_4$			OUTC1$_4$ / INPC1$_4$			

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Table 10 Pin Characteristics for 64-Pin Package (Continued)

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	Timer S Pin	UART Pin	Multi-master I²C bus Pin	Analog Pin
41		P2$_3$			OUTC1$_3$ / INPC1$_3$			
42		P2$_2$			OUTC1$_2$ / INPC1$_2$			
43		P2$_1$			OUTC1$_1$ / INPC1$_1$		SCL$_{MM}$	
44		P2$_0$			OUTC1$_0$ / INPC1$_0$		SDA$_{MM}$	
45		P1$_7$	$\overline{INT_5}$	IDU	INPC1$_7$			
46		P1$_6$	$\overline{INT_4}$	IDW				
47		P1$_5$	$\overline{INT_3}$	IDV				$\overline{AD_{TRG}}$
48		P0$_3$						AN0$_3$
49		P0$_2$						AN0$_2$
50		P0$_1$						AN0$_1$
51		P0$_0$						AN0$_0$
52		P10$_7$	$\overline{KI_3}$					AN$_7$
53		P10$_6$	$\overline{KI_2}$					AN$_6$
54		P10$_5$	$\overline{KI_1}$					AN$_5$
55		P10$_4$	$\overline{KI_0}$					AN$_4$
56		P10$_3$						AN$_3$
57		P10$_2$						AN$_2$
58		P10$_1$						AN$_1$
59	AV$_{SS}$							
60		P10$_0$						AN$_0$
61	V$_{REF}$							
62	AV$_{CC}$							
63		P9$_3$						AN2$_4$
64		P9$_2$		TB2$_{IN}$				

1.6 Pin Description

Table 1.10 Pin Description (64-Pin, 80-Pin and 85-Pin Packages)

Classification	Symbol	I/O Type	Function
Power Supply	V_{CC}, V_{SS}	I	Apply 2.7 to 5.5V to the V_{CC} pin. Apply 0V to the V_{SS} pin.
Analog Power Supply	AV_{CC} AV_{SS}	I	Supplies power to the A/D converter. Connect the AV_{CC} pin to V_{CC} and the AV_{SS} pin to V_{SS}.
Reset Input	$\overline{RESET}$	I	The MCU is in a reset state when "L" is applied to the $\overline{RESET}$ pin
CNV_{SS}	CNV_{SS}	I	Connect the CNV_{SS} pin to V_{SS}.
Main Clock Input	X_{IN}	I	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between X_{IN} and X_{OUT}. To apply external clock, apply it to X_{IN} and leave X_{OUT} open. If X_{IN} is not used (for external oscillator or external clock) connect X_{IN} pin to V_{CC} and leave X_{OUT} open.
Main Clock Output	X_{OUT}	O	
Sub Clock Input	X_{CIN}	I	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between X_{CIN} and X_{COUT}.
Sub Clock Output	X_{COUT}	O	
$\overline{INT}$ Interrupt Input	$\overline{INT0}$ to $\overline{INT5}$	I	Input pins for the $\overline{INT}$ interrupt. $\overline{INT2}$ can be used for Timer A Z-phase function.
$\overline{NMI}$ Interrupt Input	$\overline{NMI}$	I	Input pin for the $\overline{NMI}$ interrupt. $\overline{NMI}$ cannot be used as I/O port while the three-phase motor control is enabled. Apply a stable "H" to $\overline{NMI}$ after setting it's direction register to "0" when the three-phase motor control is enabled.
Key Input Interrupt	$\overline{KI0}$ to $\overline{KI3}$	I	Input pins for the key input interrupt
Timer A	$TA0_{OUT}$ to $TA4_{OUT}$	I/O	I/O pins for the timer A0 to A4
	$TA0_{IN}$ to $TA4_{IN}$	I	Input pins for the timer A0 to A4
	ZP	I	Input pin for Z-phase
Timer B	$TB0_{IN}$ to $TB2_{IN}$	I	Input pins for the timer B0 to B2
Three-phase Motor Control Timer Output	U, $\overline{U}$, V, $\overline{V}$, W, $\overline{W}$	O	Output pins for the three-phase motor control timer
	IDU, IDW, IDV, $\overline{SD}$	I/O	Input and output pins for the three-phase motor control timer
Serial I/O	$\overline{CTS0}$ to $\overline{CTS2}$	I	Input pins for data transmission control
	$\overline{RTS0}$ to $\overline{RTS2}$	O	Output pins for data reception control
	CLK0 to CLK3	I/O	Inputs and outputs the transfer clock
	RxD0 to RxD2	I	Inputs serial data
	TxD0 to TxD2	O	Outputs serial data
	CLKS1	O	Output pin for transfer clock
I^{2}C Mode	SDA2	I/O	Inputs and outputs serial data
	SCL2		Inputs and outputs the transfer clock
Multi-master I^{2}C bus	SDA_{MM}	I/O	Inputs and outputs serial data
	SCL_{MM}		Inputs and outputs the transfer clock
Reference Voltage Input	V_{REF}	I	Applies reference voltage to the A/D converter
A/D Converter	AN0 to AN7 AN00 to AN03 AN24	I	Analog input pins for the A/D converter
	$\overline{AD_{TRG}}$		Input pin for an external A/D trigger

I : Input   O : Output   I/O : Input and output

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Table 1.10 Pin Description (64-Pin, 80-Pin and 85-Pin Packages) (Continued)

Classification	Symbol	I/O Type	Function
Timer S	INPC1_0 to INPC1_7	I	Input pins for the time measurement function
	OUTC1_0 to OUTC1_7	O	Output pins for the waveform generating function
I/O Ports	P0$_0$ to P0$_3$ P1$_5$ to P1$_7$ P2$_0$ to P2$_7$ P3$_0$ to P3$_3$ P6$_0$ to P6$_7$ P7$_0$ to P7$_7$ P8$_0$ to P8$_7$ P10$_0$ to P10$_7$	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resister available in 4-bit units
	P9$_0$ to P9$_3$	I/O	I/O ports having equivalent functions to P0

I : Input   O : Output   I/O : Input and output

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2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to 0.

2.8.3 Zero Flag (Z Flag)

This flag is set to 1 when an arithmetic operation resulted in 0; otherwise, it is 0.

2.8.4 Sign Flag (S Flag)

This flag is set to 1 when an arithmetic operation resulted in a negative value; otherwise, it is 0.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is 0 ; register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O Flag)

This flag is set to 1 when the operation resulted in an overflow; otherwise, it is 0.

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1. The I flag is cleared to 0 when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is 0; USP is selected when the U flag is 1.

The U flag is cleared to 0 when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write 0. When read, its content is indeterminate.

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4. Special Function Register (SFR)

SFR (Special Function Register) is the control register of peripheral functions. **Tables 4.1** to **4.7** list the SFR information.

Table 4.1 SFR Information(1)[1]

Address	Register	Symbol	After Reset
0000_{16}			
0001_{16}			
0002_{16}			
0003_{16}			
0004_{16}	Processor mode register 0	PM0	00_{16}
0005_{16}	Processor mode register 1	PM1	00000100_2
0006_{16}	System clock control register 0	CM0	01001000_2
0007_{16}	System clock control register 1	CM1	00100000_2
0008_{16}			
0009_{16}	Address match interrupt enable register	AIER	$XXXXXX00_2$
$000A_{16}$	Protect register	PRCR	$XX000000_2$
$000B_{16}$			
$000C_{16}$	Oscillation stop detection register [2]	CM2	$0X000010_2$
$000D_{16}$			
$000E_{16}$	Watchdog timer start register	WDTS	XX_{16}
$000F_{16}$	Watchdog timer control register	WDC	$00XXXXXX_2$
0010_{16}	Address match interrupt register 0	RMAD0	00_{16}
0011_{16}			00_{16}
0012_{16}			$X0_{16}$
0013_{16}			
0014_{16}	Address match interrupt register 1	RMAD1	00_{16}
0015_{16}			00_{16}
0016_{16}			$X0_{16}$
0017_{16}			
0018_{16}			
0019_{16}	Voltage detection register 1 [3]	VCR1	00001000_2
$001A_{16}$	Voltage detection register 2 [3]	VCR2	00_{16}
$001B_{16}$			
$001C_{16}$	PLL control register 0	PLC0	$0001X010_2$
$001D_{16}$			
$001E_{16}$	Processor mode register 2	PM2	$XXX00000_2$
$001F_{16}$	Low voltage detection interrupt register	D4INT	00_{16}
0020_{16}	DMA0 source pointer	SAR0	XX_{16}
0021_{16}			XX_{16}
0022_{16}			XX_{16}
0023_{16}			
0024_{16}	DMA0 destination pointer	DAR0	XX_{16}
0025_{16}			XX_{16}
0026_{16}			XX_{16}
0027_{16}			
0028_{16}	DMA0 transfer counter	TCR0	XX_{16}
0029_{16}			XX_{16}
$002A_{16}$			
$002B_{16}$			
$002C_{16}$	DMA0 control register	DM0CON	$00000X00_2$
$002D_{16}$			
$002E_{16}$			
$002F_{16}$			
0030_{16}	DMA1 source pointer	SAR1	XX_{16}
0031_{16}			XX_{16}
0032_{16}			XX_{16}
0033_{16}			
0034_{16}	DMA1 destination pointer	DAR1	XX_{16}
0035_{16}			XX_{16}
0036_{16}			XX_{16}
0037_{16}			
0038_{16}	DMA1 transfer counter	TCR1	XX_{16}
0039_{16}			XX_{16}
$003A_{16}$			
$003B_{16}$			
$003C_{16}$	DMA1 control register	DM1CON	$00000X00_2$
$003D_{16}$			
$003E_{16}$			
$003F_{16}$			

NOTES:
　　1. The blank spaces are reserved. No access is allowed.
　　2. The CM20, CM21, and CM27 bits do not change at oscillation stop detection reset.
　　3. This register does not change at software reset, watchdog timer reset and oscillation stop detection reset.

　X : Undefined

Table 4.6 SFR Information(6)[1]

Address	Register	Symbol	After Reset
0380_{16}	Count start flag	TABSR	00_{16}
0381_{16}	Clock prescaler reset flag	CPSRF	$0XXXXXXX_2$
0382_{16}	One-shot start flag	ONSF	00_{16}
0383_{16}	Trigger select register	TRGSR	00_{16}
0384_{16}	Up-down flag	UDF	00_{16}
0385_{16}			
0386_{16}	Timer A0 register	TA0	XX_{16}
0387_{16}			XX_{16}
0388_{16}	Timer A1 register	TA1	XX_{16}
0389_{16}			XX_{16}
$038A_{16}$	Timer A2 register	TA2	XX_{16}
$038B_{16}$			XX_{16}
$038C_{16}$	Timer A3 register	TA3	XX_{16}
$038D_{16}$			XX_{16}
$038E_{16}$	Timer A4 register	TA4	XX_{16}
$038F_{16}$			XX_{16}
0390_{16}	Timer B0 register	TB0	XX_{16}
0391_{16}			XX_{16}
0392_{16}	Timer B1 register	TB1	XX_{16}
0393_{16}			XX_{16}
0394_{16}	Timer B2 register	TB2	XX_{16}
0395_{16}			XX_{16}
0396_{16}	Timer A0 mode register	TA0MR	00_{16}
0397_{16}	Timer A1 mode register	TA1MR	00_{16}
0398_{16}	Timer A2 mode register	TA2MR	00_{16}
0399_{16}	Timer A3 mode register	TA3MR	00_{16}
$039A_{16}$	Timer A4 mode register	TA4MR	00_{16}
$039B_{16}$	Timer B0 mode register	TB0MR	$00XX0000_2$
$039C_{16}$	Timer B1 mode register	TB1MR	$00XX0000_2$
$039D_{16}$	Timer B2 mode register	TB2MR	$00XX0000_2$
$039E_{16}$	Timer B2 special mode register	TB2SC	$X0000000_2$
$039F_{16}$			
$03A0_{16}$	UART0 transmit/receive mode register	U0MR	00_{16}
$03A1_{16}$	UART0 bit rate generator	U0BRG	XX_{16}
$03A2_{16}$	UART0 transmit buffer register	U0TB	XX_{16}
$03A3_{16}$			XX_{16}
$03A4_{16}$	UART0 transmit/receive control register 0	U0C0	00001000_2
$03A5_{16}$	UART0 transmit/receive control register 1	U0C1	00000010_2
$03A6_{16}$	UART0 receive buffer register	U0RB	XX_{16}
$03A7_{16}$			XX_{16}
$03A8_{16}$	UART1 transmit/receive mode register	U1MR	00_{16}
$03A9_{16}$	UART1 bit rate generator	U1BRG	XX_{16}
$03AA_{16}$	UART1 transmit buffer register	U1TB	XX_{16}
$03AB_{16}$			XX_{16}
$03AC_{16}$	UART1 transmit/receive control register 0	U1C0	00001000_2
$03AD_{16}$	UART1 transmit/receive control register 1	U1C1	00000010_2
$03AE_{16}$	UART1 receive buffer register	U1RB	XX_{16}
$03AF_{16}$			XX_{16}
$03B0_{16}$	UART transmit/receive control register 2	UCON	$X0000000_2$
$03B1_{16}$			
$03B2_{16}$			
$03B3_{16}$			
$03B4_{16}$			
$03B5_{16}$			
$03B6_{16}$			
$03B7_{16}$			
$03B8_{16}$	DMA0 request cause select register	DM0SL	00_{16}
$03B9_{16}$			
$03BA_{16}$	DMA1 request cause select register	DM1SL	00_{16}
$03BB_{16}$			
$03BC_{16}$			
$03BD_{16}$			
$03BE_{16}$			
$03BF_{16}$			

Note 1:The blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.7 SFR Information(7)[1]

Address	Register	Symbol	After Reset
03C0₁₆	A/D register 0	AD0	XX₁₆
03C1₁₆			XX₁₆
03C2₁₆	A/D register 1	AD1	XX₁₆
03C3₁₆			XX₁₆
03C4₁₆	A/D register 2	AD2	XX₁₆
03C5₁₆			XX₁₆
03C6₁₆	A/D register 3	AD3	XX₁₆
03C7₁₆			XX₁₆
03C8₁₆	A/D register 4	AD4	XX₁₆
03C9₁₆			XX₁₆
03CA₁₆	A/D register 5	AD5	XX₁₆
03CB₁₆			XX₁₆
03CC₁₆	A/D register 6	AD6	XX₁₆
03CD₁₆			XX₁₆
03CE₁₆	A/D register 7	AD7	XX₁₆
03CF₁₆			XX₁₆
03D0₁₆			
03D1₁₆			
03D2₁₆	A/D trigger control register	ADTRGCON	00₁₆
03D3₁₆	A/D convert status register 0	ADSTAT0	00000X00₂
03D4₁₆	A/D control register 2	ADCON2	00₁₆
03D5₁₆			
03D6₁₆	A/D control register 0	ADCON0	00000XXX₂
03D7₁₆	A/D control register 1	ADCON1	00₁₆
03D8₁₆			
03D9₁₆			
03DA₁₆			
03DB₁₆			
03DC₁₆			
03DD₁₆			
03DE₁₆			
03DF₁₆			
03E0₁₆	Port P0 register	P0	XX₁₆
03E1₁₆	Port P1 register	P1	XX₁₆
03E2₁₆	Port P0 direction register	PD0	00₁₆
03E3₁₆	Port P1 direction register	PD1	00₁₆
03E4₁₆	Port P2 register	P2	XX₁₆
03E5₁₆	Port P3 register	P3	XX₁₆
03E6₁₆	Port P2 direction register	PD2	00₁₆
03E7₁₆	Port P3 direction register	PD3	00₁₆
03E8₁₆			
03E9₁₆			
03EA₁₆			
03EB₁₆			
03EC₁₆	Port P6 register	P6	XX₁₆
03ED₁₆	Port P7 register	P7	XX₁₆
03EE₁₆	Port P6 direction register	PD6	00₁₆
03EF₁₆	Port P7 direction register	PD7	00₁₆
03F0₁₆	Port P8 register	P8	XX₁₆
03F1₁₆	Port P9 register	P9	XX₁₆
03F2₁₆	Port P8 direction register	PD8	00₁₆
03F3₁₆	Port P9 direction register	PD9	000X0000₂
03F4₁₆	Port P10 register	P10	XX₁₆
03F5₁₆			
03F6₁₆	Port P10 direction register	PD10	00₁₆
03F7₁₆			
03F8₁₆			
03F9₁₆			
03FA₁₆			
03FB₁₆			
03FC₁₆	Pull-up control register 0	PUR0	00₁₆
03FD₁₆	Pull-up control register 1	PUR1	00₁₆
03FE₁₆	Pull-up control register 2	PUR2	00₁₆
03FF₁₆	Port control register	PCR	00₁₆

Note 1:The blank spaces are reserved. No access is allowed.

X : Undefined

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA85-7x7-0.65	PTLG0085JB-A	85F0G	0.1g

Index mark (Laser mark)

Index mark

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.65	—
b	0.31	0.35	0.39
b₁	0.39	0.43	0.47
x	—	—	0.08
y	—	—	0.10
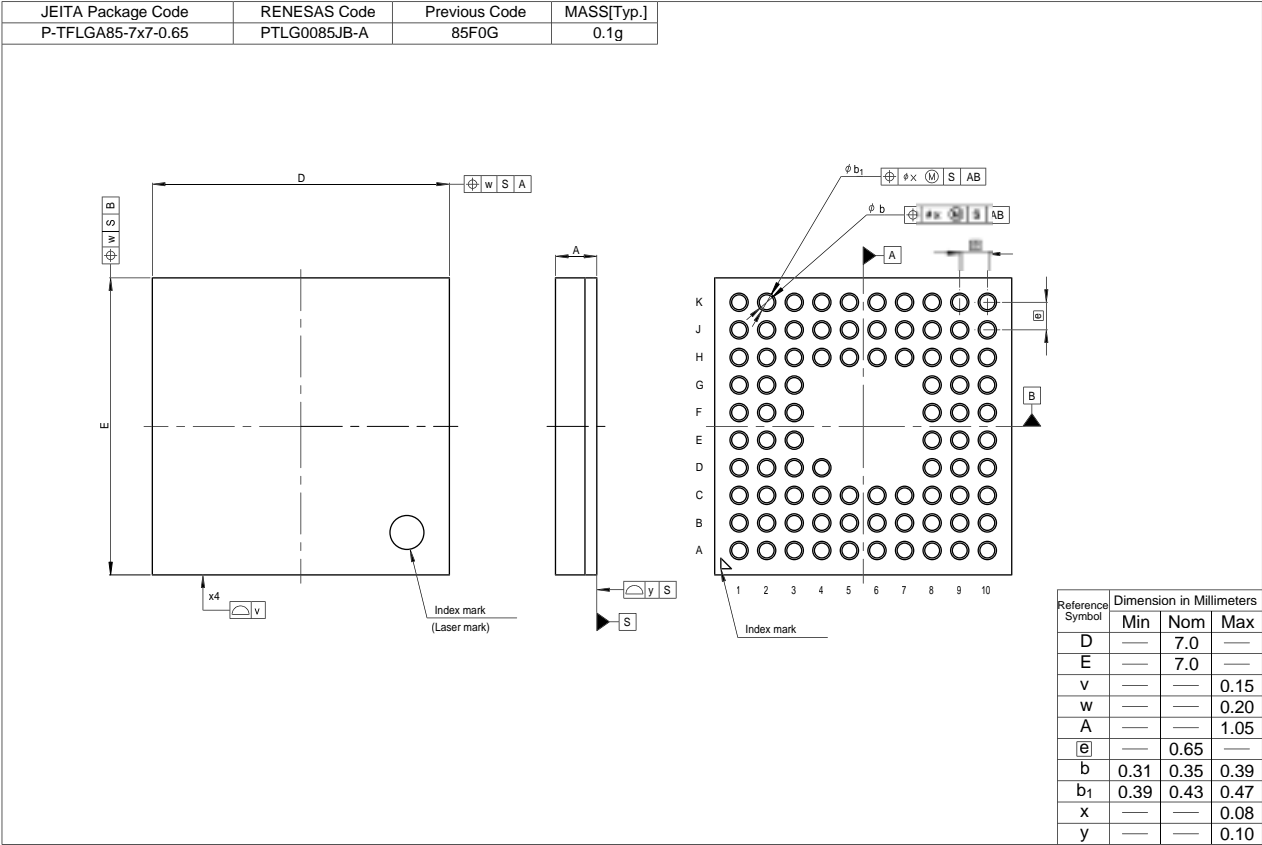
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